



OEM HARD DISK DRIVE SPECIFICATIONS

for

DPLA-24480/25120 (4480/5120 MB)

2.5-Inch Hard Disk Drive with ATA Interface

Revision (3.0)



OEM HARD DISK DRIVE SPECIFICATIONS

for

DPLA-24480/25120 (4480/5120 MB)

2.5-Inch Hard Disk Drive with ATA Interface

Revision (3.0)

1st Edition (0.1) S82H-9141-00 (May 08, 1997) Preliminary
2nd Edition (0.2) S82H-9141-01 (May 15, 1997) Preliminary
3rd Edition (1.0) S82H-9141-02 (June 27, 1997)
4th Edition (1.1) S82H-9141-03 (July 16, 1997)
5th Edition (2.0) S82H-9141-04 (September 5, 1997)
6th Edition (3.0) S82H-9141-05 (October 01, 1997)

The following paragraph does not apply to the United Kingdom or any country where such provisions are inconsistent with local law: INTERNATIONAL BUSINESS MACHINES CORPORATION PROVIDES THIS PUBLICATION "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Some states do not allow disclaimer or express or implied warranties in certain transactions, therefore, this statement may not apply to you.

This publication could include technical inaccuracies or typographical errors. Changes are periodically made to the information herein; these changes will be incorporated in new editions of the publication. IBM may make improvements and/or changes in the product(s) and/or the program(s) described in this publication at any time.

It is possible that this publication may contain reference to, or information about, IBM products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that IBM intends to announce such IBM products, programming, or services in your country.

Technical information about this product is available by contacting with local IBM representative or the following.

Tel:+1-507-253-4110 / Fax:+1-507-253-4111 ----- U.S.A
Tel:+81-466-45-1441 / Fax:+81-466-45-1045 ----- Japan
Tel:+44-1705-561567 / Fax:+44-1705-210266 ----- England
Tel:+49-6131-845050 / Fax:+49-6131-846442 ----- Germany
Internet: <http://www.storage.ibm.com/oem>

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Armonk, NY 10577.

© Copyright International Business Machines Corporation 1997. All rights reserved.

Note to U.S. Government Users — Documentation related to restricted rights — Use, duplication or disclosure is subject to restrictions set forth in GSA ADP Schedule Contract with IBM Corp.

Contents

1.0 General	1
1.1 Glossary	1
1.2 General Caution	1
1.2.1 Caution of usage	2
2.0 General Features	5
<hr/>	
Part 1. Functional Specification	7
3.0 Drive Characteristics	9
3.1 Logical Drive Format	9
3.2 Data Sheet	9
3.3 Performance Characteristics	10
3.3.1 Command Processing	10
3.3.2 Average Seek Time (Including Settling)	10
3.3.3 Single Track Seek Time	11
3.3.4 Full Stroke Seek	12
3.3.5 Average Latency	12
3.3.6 Drive Ready Time	12
3.3.7 Operating Modes.	13
4.0 Data Integrity	15
4.1 Data Loss by Power Off	15
4.2 Write Cache	15
4.3 Equipment Status	15
4.4 WRITE Safety	16
4.5 Data buffer test	16
4.6 Error Recovery	16
4.7 Automatic Reallocation	16
4.7.1 Non Recovered Write Errors	16
4.7.2 Non Recovered Read Errors	16
4.7.3 Recovered Read Errors	17
5.0 Specification	19
5.1 Environment	19
5.1.1 Temperature and Humidity	19
5.1.2 Magnetic Fields	20
5.2 DC Power Requirements	21
5.2.1 Start Up Current	22
5.3 Reliability	23
5.3.1 Data Reliability	23
5.3.2 Failure Prediction (S.M.A.R.T.)	23
5.3.3 Cable Noise Interference	23
5.3.4 Drive Usage Condition	23
5.3.5 Preventive Maintenance	23
5.3.6 Load/Unload	24
5.4 Mechanical Specifications	26
5.4.1 Mechanical Dimensions and Weight	26
5.4.2 Hole Locations	26
5.4.3 Mounting Orientation	27

5.5	Vibration and Shock	28
5.5.1	Operating Vibration	28
5.5.2	Non-Operating Vibration	28
5.5.3	Operating Shock	29
5.5.4	Non-Operating Shock	29
5.6	Acoustics	30
5.6.1	Sound Power Level	30
5.6.2	Discrete Tone Penalty	31
5.7	Identification	32
5.7.1	Labels	32
5.8	Electromagnetic Compatibility	32
5.8.1	CE Mark	32
5.8.2	C-Tick Mark	32
5.9	Safety	33
5.9.1	Underwriters Lab(UL) Approval	33
5.9.2	Canadian Standards Authority(CSA) Approval	33
5.9.3	IEC Compliance	33
5.9.4	German Safety Mark	33
5.9.5	Flammability	33
5.9.6	Secondary Circuit Protection	33
5.10	Packaging	33
6.0	Electrical Interface Specifications	35
6.1	Cabling	35
6.2	Interface Connector	35
6.2.1	Signal Definition	36
6.3	Interface Logic Signal Levels	39
6.4	Reset timings	40
6.5	PIO Timings	41
6.5.1	DMA Timings (Single Word)	42
6.5.2	DMA Timings (Multiword)	43
6.5.3	Ultra DMA Timings	44
6.6	Drive Address Setting	52
6.6.1	Default Setting	52
6.7	Addressing of drive Registers	53
<hr/>		
Part 2.	ATA Interface Specification	55
7.0	General	57
7.1	Introduction	57
7.2	Terminology	57
8.0	Deviations From Standard	59
9.0	Registers	61
9.1	Alternate Status Register	62
9.2	Command Register	62
9.3	Cylinder High Register	62
9.4	Cylinder Low Register	62
9.5	Data Register	63
9.6	Device Control Register	63
9.7	Drive Address Register	63
9.8	Device/Head Register	64
9.9	Error Register	64

9.10	Features Register	65
9.11	Sector Count Register	65
9.12	Sector Number Register	65
9.13	Status Register	65
10.0	General Operation Descriptions	67
10.1	Reset Response	67
10.1.1	Register Initialization	69
10.2	Diagnostic and Reset considerations	70
10.3	Sector Addressing Mode	71
10.3.1	Logical CHS Addressing Mode	71
10.3.2	LBA Addressing Mode	71
10.4	Power Management Feature	72
10.4.1	Power Mode	72
10.4.2	Power Management Commands	72
10.4.3	Standby/Sleep command completion timing	72
10.4.4	Standby timer	73
10.4.5	Status	73
10.4.6	Interface Capability for Power Modes	73
10.4.7	Initial Power Mode at Power On	73
10.5	Adaptive Battery Life Extender (ABLE-2) Feature	74
10.5.1	Performance Idle mode	74
10.5.2	Active Idle mode	74
10.5.3	Low Power Idle mode	74
10.5.4	Transition Time	74
10.6	S.M.A.R.T. Function	76
10.6.1	Attributes	76
10.6.2	Attribute values	76
10.6.3	Attribute thresholds	76
10.6.4	Threshold exceeded condition	76
10.6.5	S.M.A.R.T. commands	76
10.6.6	S.M.A.R.T. operation with power management modes	77
10.7	Security Mode Feature Set	78
10.7.1	Security mode	78
10.7.2	Security level	78
10.7.3	Password	78
10.7.4	Operation example	79
10.7.5	Command Table	82
10.8	Protected Area Function (Vendor Specific)	84
10.8.1	Example for operation (In LBA mode)	84
10.9	Write Cache Function	86
10.10	Reassign Function	87
10.10.1	Auto Reassign Function	87
11.0	Command Protocol	89
11.1	Data In Commands	89
11.2	Data Out Commands	90
11.3	Non-Data Commands	92
11.4	DMA Data Transfer Commands	93
12.0	Command Descriptions	95
12.1	Check Power Mode (E5h/98h)	99
12.2	Execute Device Diagnostic (90h)	100
12.3	Flush Cache (E7h)	101
12.4	Format Track (50h: Vendor Specific)	102

12.5	Format Unit (F7h: Vendor Specific)	104
12.6	Identify Device (ECh)	106
12.7	Identify Device DMA (EEh)	110
12.8	Idle (E3h/97h)	111
12.9	Idle Immediate (E1h/95h)	112
12.10	Initialize Device Parameters (91h)	113
12.11	Read Buffer (E4h)	114
12.12	Read DMA (C8h/C9h)	115
12.13	Read Long (22h/23h)	117
12.14	Read Multiple (C4h)	119
12.15	Read Native Max LBA/CYL (F8h: Vendor Specific)	121
12.16	Read Sectors (20h/21h)	123
12.17	Read Verify Sectors (40h/41h)	125
12.18	Recalibrate (1xh)	127
12.19	Security Disable Password (F6h)	128
12.20	Security Erase Prepare (F3h)	129
12.21	Security Erase Unit (F4h)	130
12.22	Security Freeze Lock (F5h)	132
12.23	Security Set Password (F1h)	133
12.24	Security Unlock (F2h)	135
12.25	Seek (7xh)	137
12.26	Set Features (EFh)	138
12.27	Set Max LBA/CYL (F9h: Vendor Specific)	140
12.28	Set Multiple (C6h)	142
12.29	Sleep (E6h/99h)	143
12.30	S.M.A.R.T. Function Set (B0h)	144
12.30.2	Device Attributes Data Structure	147
12.30.3	Device Attribute Thresholds Data Structure	153
12.30.4	Error Reporting	155
12.31	Standby (E2h/96h)	157
12.32	Standby Immediate (E0h/94h)	158
12.33	Write Buffer (E8h)	159
12.34	Write DMA (CAh/CBh)	160
12.35	Write Long (32h/33h)	162
12.36	Write Multiple (C5h)	164
12.37	Write Sectors (30h/31h)	166
12.38	Write Verify (3Ch: Vendor Specific)	168
13.0	Timings	171
14.0	Appendix	175
14.1	Commands Support Coverage	175
14.2	SET FEATURES Command Support Coverage	178
Index		179

1.0 General

This document describes the specifications of the following IBM 2.5-inch, ATA interface hard disk drives:

- DPLA-24480 (4480 MB)
- DPLA-25120 (5120 MB)

Note: The specifications are subject to change without notice.

1.1 Glossary

<i>Word</i>	<i>Meaning</i>
Kbpi	1 000 Bit Per Inch
Mbps	1 000 000 Bit per second
MB	1 000 000 bytes
KB	1 000 bytes
32 KB	32 x 1 024 bytes
64 KB	64 x 1 024 bytes
Mb/sq.in	1 000 000 bits per square inch
MLC	Machine Level Control
TBD	To Be Defined

1.2 General Caution

- Do not apply pressing force on the top cover (See Figure 1 on page 2).
- Do not cover the breathing hole on the top cover (See Figure 2 on page 3).
- Do not touch the interface connector pins and the surface of printed circuit board.
- The drive can be easily damaged by shocks or ESD (Electric Static Discharge), so any damages applied to the drive after taking out from shipping package and opening ESD protective bag are user's responsibilities.

1.2.1 Caution of usage

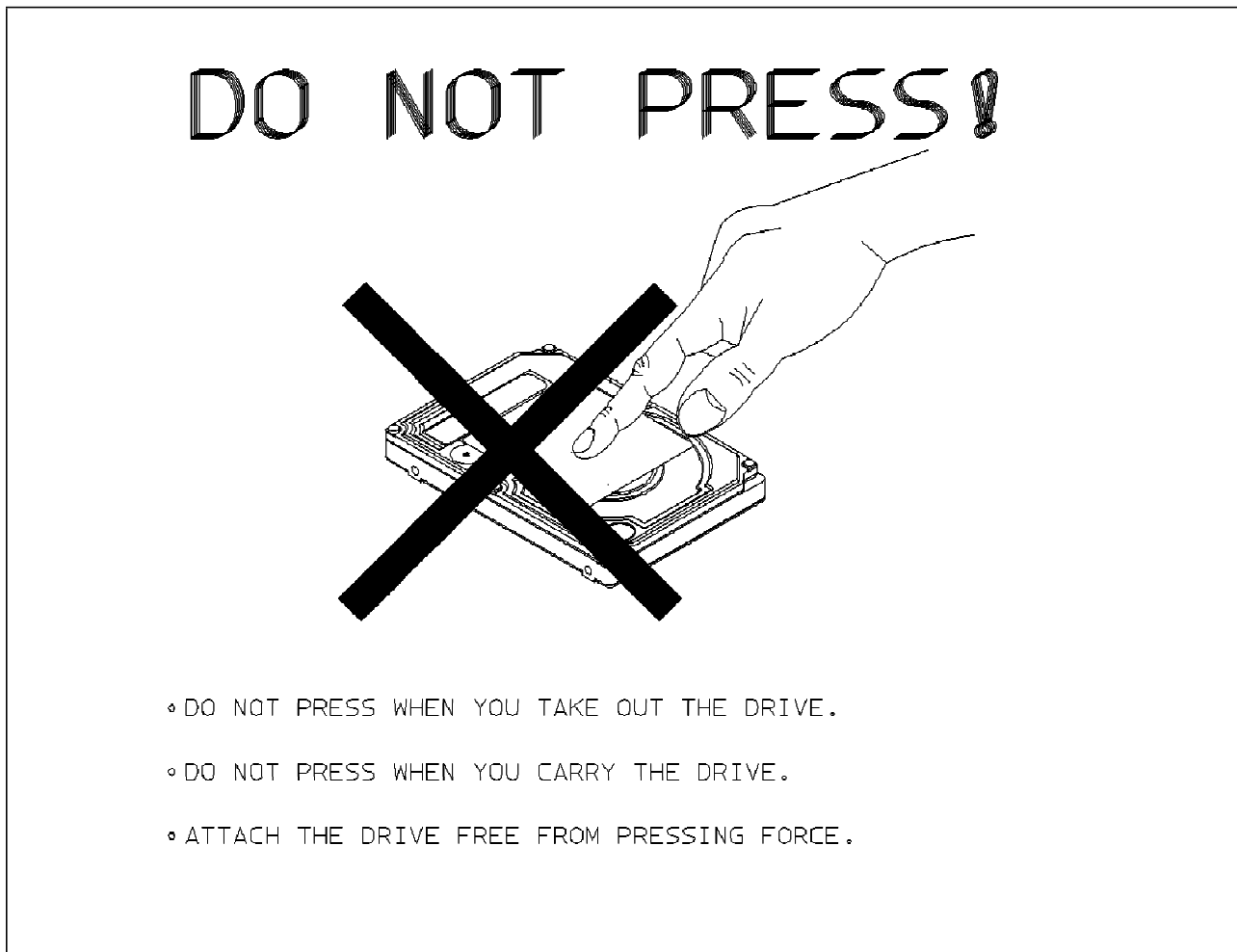
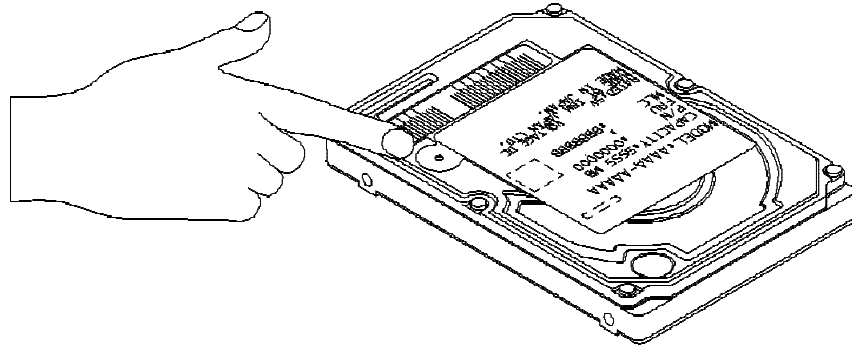


Figure 1. Handling caution of DPLA-24480/25120

DO NOT COVER THIS HOLE



COVERING THIS HOLE WILL RESULT LOSS OF DATA.

Figure 2. Breathing hole caution of DPLA-24480/25120

2.0 General Features

- 2.5-inch, 17mm Height MCC Compliance
- 5120MB / 4480MB formatted capacity
- 512 bytes/sector
- AT Interface (Enhanced IDE) conforming to ATA-3
- Integrated controller
- No-ID recording format
- PRML
- Multi Zone Recording
- Enhanced ECC
 - On The Fly correction : 9 Bytes/sector
 - Offline correction : 12 Bytes/sector
- 468KB Buffer for Read and Write
- Host data transfer speed.
 - 16.6 MB/sec : PIO Mode-4
 - 33.3 MB/sec : Ultra DMA Mode-2
- Media data transfer rate 98.5 (outer zone) - 60.2 (inner zone) Mbit/sec
- Average seek time 12 milliseconds for read
- Closed-loop actuator servo (Embedded Sector Servo)
- Rotary voice coil motor actuator
- Load / Unload mechanism
- Mechanical Latch
- Adaptive power save control (0.85 Watt at low-power idle state)
- 3.6 sec Power on to ready
- Shock
 - Non-operation : 400G/2ms
 - Operation : 100G/2ms

Note: Mounting screw position is

- Compatible with DLGA-2xxxx, DTNA-2xxxx, DDLA-2xxxx, DTCA-2xxxx.
- Incompatible with DMCA-2xxxx, DCRA-2xxxx, DSOA-2xxxx, DPRA-2xxxx, DBOA-2xxx.

Part 1. Functional Specification

3.0 Drive Characteristics

This chapter provides the characteristics of the drives.

3.1 Logical Drive Format

The customer usable data capacity is as shown below.

Figure 3. Drive Parameter		
Descriptions	DPLA-24480	DPLA-25120
Logical Head Number	15	15
Logical Sectors/Track	63	63
Logical Cylinder Number	9264	10592
Logical Sector Size	512	512
Total Customer Usable Data Sectors	8 754 480	10 009 440
Total Customer Usable Data Bytes	4480 MB (4,482,293,760)	5120 MB (5,124,833,280)

3.2 Data Sheet

Figure 4. Data Sheet	
Media transfer rate [Mb/sec]	60.2 - 98.5
Interface transfer rate [MB/sec]	33.3 MB/sec Max (Ultra DMA Mode-2) 16.6 MB/sec Max (PIO-4)
Data buffer size [KB]	512 KB (Read / Write)
Rotational speed [RPM]	4900
Average latency [msec]	6.1
Recording density [Kbpi]	201 Maximum
Track density [TPI]	12,500
Areal density [Gb/sq.in.]	2.51 Maximum
Number of zone	12
Number of disks	4
Number of heads	7 / 8
Servo design method	Embedded sector servo

3.3 Performance Characteristics

File performance is characterized by the following parameters:

- Command Overhead
- Mechanical Positioning
 - Seek Time
 - Latency
- Data Transfer Speed
- Buffering Operation

Note: All the above parameters contribute to a file performance. There are other parameters which contribute to the performance on the actual system. This specification tries to define the essential file characteristics, not the system throughput which is dependent on the system and the application.

The following table gives a **typical value** of each parameter. The detail descriptions are followed in the next sections.

Function	Typical
Average Random Seek Time For Read	12 msec
Average Random Seek Time For Write	13 msec
Rotational Speed	4900 rpm
Power On To Ready	3.6 sec
Command Overhead	1.0 msec
Disk-Buffer Data Transfer	98.5 - 60.2 Mbit/sec
Buffer-Host Data Transfer	16.6 MB/sec (PIO Mode-4) 33.3 MB/sec (Ultra DMA Mode-2)

Figure 5. Performance Parameter

3.3.1 Command Processing

Command overhead time is defined as the total time from when the command is received by the drive to the start of motion of the actuator.

3.3.2 Average Seek Time (Including Settling)

Command Type	Typical	Max
Read	12 msec	16 msec
Write	13 msec	17 msec

Figure 6. Mechanical Positioning Performance

'Typical' and 'Max' are given throughout the performance specification by;

Typical Average of the drive population tested at nominal environmental and voltage conditions.

Max Maximum value measured on any one drive over the full range of the environmental and voltage conditions. (See section on Environment and D.C. Power Requirements.)

The seek time is measured from the start of motion of the actuator to the start of a **reliable read or write operation**. Reliable read or write implies that error correction/recovery is not employed to correct for arrival problems. The Average Seek Time is measured as the weighted average of all possible seek combinations.

$$\text{Weighted Average} = \frac{\sum_{n=1}^{\text{max}} (\text{max} + 1 - n) (T_{n.in} + T_{n.out})}{(\text{max} + 1) (\text{max})}$$

Where:

- max = Maximum Seek Length
- n = Seek Length (1 to max)
- Tn.in = Inward measured seek time for a n track seek
- Tn.out = Outward measured seek time for a n track seek

3.3.3 Single Track Seek Time

Function	Typical	Max
READ	4 msec	5.5 msec
Write	4 msec	6.5 msec

Figure 7. Single Track Seek Time

Single track seek is measured as the average of one (1) single track seek from every track in both directions (inward and outward).

3.3.4 Full Stroke Seek

Function	Typical	Max
Read	23.0 msec	30.0 msec
Write	24.0 msec	31.0 msec

Figure 8. Full Stroke Seek Time

Full stroke seek is measured as the average of 1000 full stroke seeks.

3.3.5 Average Latency

RPM	Time for a revolution	Average Latency
4900	12.2 msec	6.1 msec

Figure 9. Latency Time

3.3.6 Drive Ready Time

Condition	Typical	Max
Power On To Ready	3.6 sec	9.5 sec

Figure 10. Drive Ready Time

Ready The condition in which the drive is able to perform a media access command (e.g. read, write) immediately.

Power On This includes the time required for the internal self diagnostics.

3.3.7 Operating Modes.

Operating mode	Description
Spin-Up	: Start up time period from spindle stop or power down.
Seek	: Seek operation mode
Write	: Write operation mode
Read	: Read operation mode
Performance idle	: The device is capable of responding immediately to media access requests. All electronic components remain powered and full frequency servo remains operational.
Active idle	: The device is capable of responding immediately to media access requests. Some circuitry including servo system and R/W electronics are in power saving mode. The head is parked near the mid-diameter of disk without servoing. A device in Active idle mode may take longer to complete the execution of a command because it has to activate that circuitry.
Low power idle	: Head is unloaded on the ramp position. Spindle motor is rotating at full speed.
Standby	: The device interface is capable of accepting commands. Spindle motor is stopped. All circuitry except host interface are in power saving mode. The execution of commands is delayed until spindle becomes ready.
Sleep	: The device requires a soft reset or a hard reset to be activated. All electronics including spindle motor and host interface are shut off.

Figure 11. Operating Mode

3.3.7.1 Mode Transition Time.

From	To	Transition Time
Standby	Idle	2.5 sec typ, 9.5 sec max.

Figure 12. Mode Transition Time

3.3.7.2 Operating mode at power on

The device goes to Idle mode after power on or hard reset as an initial state. Initial state may be changed to Standby mode using pin 49 on the interface connector. Refer to 6.6, “ Drive Address Setting” on page 52 for detail.

3.3.7.3 Adaptive power save control

The transient timing from active mode to Idle mode is adaptively controlled to the access pattern of the host system.

4.0 Data Integrity

4.1 Data Loss by Power Off

- The drive retains recorded data under all non-write operations.
- No more than one sector can be lost by power down during write operation while write cache is disabled.
- Power off during write operation may make an incomplete sector which will report hard data error when read. The sector can be recovered by a re-write operation.
- Hard reset does not cause any data loss.

4.2 Write Cache

- Power off while write cache is enabled may cause loss of data which are remaining in the cache and have not been flushed onto the disk media.
This means that there is a possibility that power off even after write command completion may cause loss of data.
- There are ways to check if all data in the write cache have been flushed onto the disk. Checking just before power off is recommended to prevent data loss.
 - To confirm successful completion of Software Reset.
 - To confirm successful completion of Flush Cache command.
 - To confirm successful completion of Check Power Mode command.
 - To confirm successful completion of Standby command.
 - To confirm successful completion of Standby Immediate command.
 - To confirm successful completion of Sleep command.

Note: For **Power Off Sequence**, refer to 5.3.6, “Load/Unload” on page 24.

4.3 Equipment Status

Equipment status is available to the host system any time the drive is not ready to read, write, or seek. This status normally exists at power-on time and will be maintained until the following conditions are satisfied:

- Access recalibration/tuning is complete.
- Spindle speed meets requirements for reliable operation.
- Self-check of drive is complete.

Appropriate error status is made available to the host system if any of the following conditions occur after the drive has once become ready:

- Spindle speed outside requirements for reliable operation.
- Occurrence of a WRITE FAULT condition.

4.4 WRITE Safety

The drive ensures that the data is written into the disk media properly. Following conditions are monitored during a write operation. When one of those conditions exceeds the criteria, the write operation is terminated and automatic retry sequence will be invoked.

- Head off track
- External shock
- Low supply voltage
- Spindle speed tolerance

4.5 Data buffer test

The data buffer is tested at Power-on-reset and when a drive self-test is requested by the host. The tests are consisted of write/read '00'x and 'ff'x pattern on all buffer.

4.6 Error Recovery

Errors occurring on the drive are handled by the error recovery procedure.

Errors that are uncorrectable after application of the error recovery procedures are reported to the host system as non-recoverable errors.

4.7 Automatic Reallocation

The sectors those show some errors may be reallocated automatically when specific conditions are met. The spare sectors for reallocation are located at the end of drive. As a result of reallocation, the physical location of logically sequenced sectors will be dispersed. The drive does not report for auto-reallocation to the host system. The conditions for auto-reallocation are described below.

4.7.1 Non Recovered Write Errors

When a write operation can not be completed after the Error Recovery Procedure (ERP) is fully carried out, the sector(s) are reallocated to the spare location. An error is reported to the host system only when the write cache is disabled and the auto reallocation is failed.

4.7.2 Non Recovered Read Errors

When a read operation is failed after defined ERP is fully carried out, a hard error is reported to the host system. This location is registered internally as a candidate for the reallocation. When a registered location is specified as a target of a write operation, a sequence of media verification is performed automatically. When the result of this verification meets the criteria, this sector is reallocated.

4.7.3 Recovered Read Errors

When a read operation for a sector failed once then recovered at the specific ERP step, this sector is reallocated automatically. A media verification sequence may be run prior to the reallocation according to the pre-defined conditions.

5.0 Specification

5.1 Environment

5.1.1 Temperature and Humidity

Figure 13. Environmental Condition	
Operating Conditions	
Temperature	5 to 55[°C] (See note)
Relative Humidity	8 to 90 [% RH] non-condensing
Maximum Wet Bulb Temperature	29.4[°C] non-condensing
Maximum Temperature Gradient	20[°C / Hour]
Altitude	- 300 to 3000 [m]
Non-Operating Conditions	
Temperature	- 40 to 65[°C]
Relative Humidity	5 to 95 [% RH] non-condensing
Maximum Wet Bulb Temperature	40[°C] non-condensing
Maximum Temperature Gradient	20[°C / Hour]
Altitude	- 300 to 12,000 [m]
Note:	
The system has to provide sufficient ventilation to maintain a surface temperature below 60[°C] at the center of the top cover of the drive.	
Non-operating condition should not continue beyond one year.	

5.1.2 Magnetic Fields

The disk drive will withstand radiation & conductive noise within the limits shown below.

5.1.2.1 Radiation Noise

The disk drive shall work without degradation of the soft error rate under the following Magnetic Flux Density Limits at the enclosure surface.

Frequency (KHz)	Limits (Gauss rms)
0 - 60	5.0
61 - 100	2.5
101 - 200	1.0
201 - 400	0.5

Figure 14. Magnetic Flux Density Limits

5.1.2.2 Conductive Noise

The disk drive shall work without degradation of the soft error rate, with an AC current of up to 45 mA(p-p), in the frequency range from DC to 20 MHz, injected through any two of the mounting screw holes of the drive via 50ohm resistor.

5.2 DC Power Requirements

Connection to the product should be made in isolated secondary circuits (SELV). The voltage specifications are applied at the power connector of the drive.

Item	Requirements	Notes
Nominal Supply	+ 5 Volt	
Power Supply Ripple (0- 20Mhz)	100 mv p-p max	*1
Tolerance	+/- 5 %	*2
Supply Current	Pop.Mean (Nominal Condition)	
Low-power Idle Average	0.17 A RMS max (0.85 W)	
Active Idle Average	0.26 A RMS max (1.3 W)	
Performance Idle Average	0.40 A RMS max (2.0 W)	*3
Read average	0.50 A RMS max (2.5 W)	*4
Write average	0.54 A RMS max (2.7 W)	
Seek average	0.52 A RMS max (2.6 W)	*5
Standby	0.06 A RMS max (0.3 W)	
Sleep	0.02 A RMS max (0.1 W)	
Start up(maximum peak)	1.00 A RMS max (5.0 W)	*6
(average from power on to ready)	0.76 A RMS max (3.8 W)	
Supply Rise Time	7 - 100 ms	

Figure 15. Power Requirement

Notes (*):

- (*1) The maximum fixed disk ripple is measured at 5V input of the drive.
- (*2) The disk drive shall not incur damage for an over voltage condition of +25 % (maximum duration of 20 ms) on the 5-volt nominal supply.
- (*3) The idle current is specified at an inner track.
- (*4) The read/write current is specified based on three operations of 63 sector read/write per 100 msec.
- (*5) The seek average current is specified based on three operations per 100 msec.
- (*6) The typical current wave form at start up is shown in Figure 16 on page 22.

5.2.1 Start Up Current

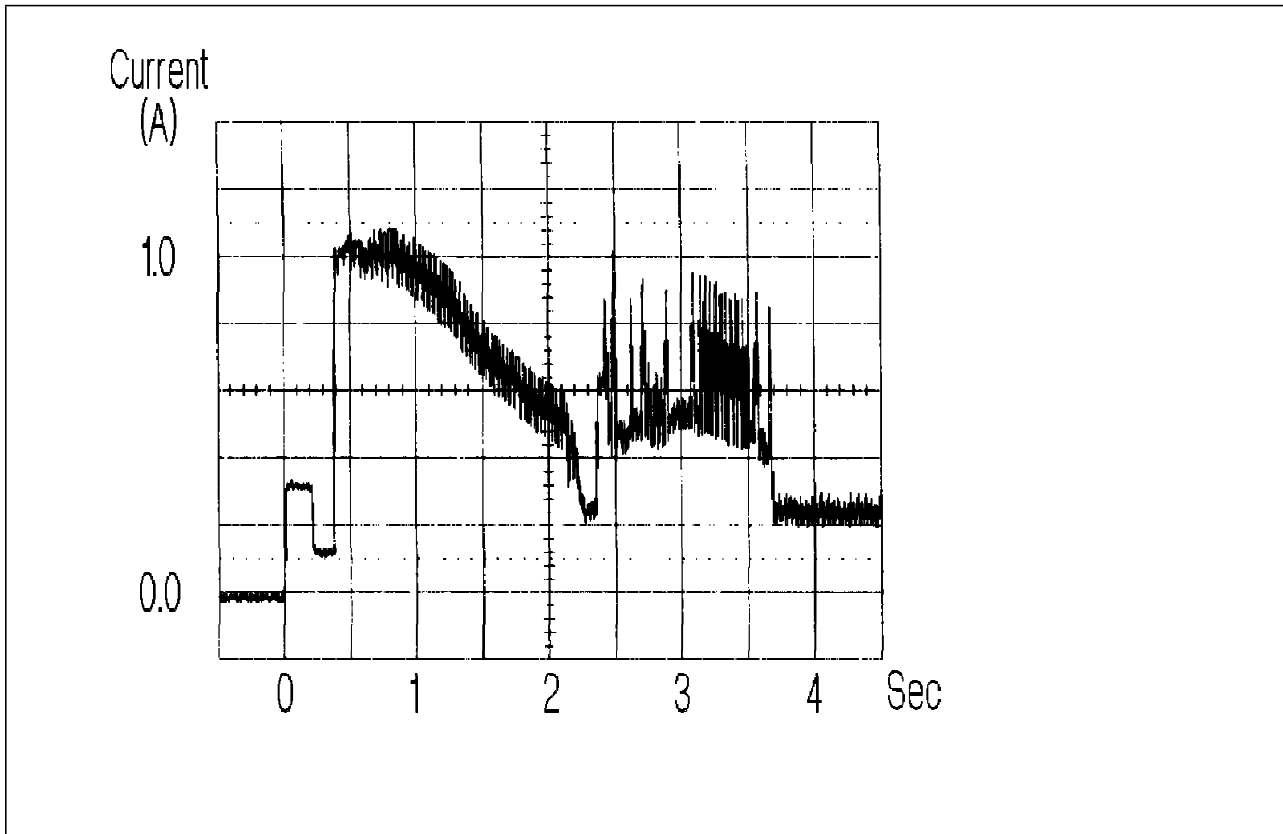


Figure 16. Typical current wave form at start up.

5.3 Reliability

5.3.1 Data Reliability

- Probability of not recovering data 1 in 10¹³ bits read
- ECC implementation
 - On-The-Fly correction, performed as a part of read channel function, recovers up to 9 symbols of error in 1 sector. (1 symbol is 8 bits.)
 - Off-line correction, performed as a part of retry procedure in the drive, recovers up to 12 symbols of error in 1 sector.

5.3.2 Failure Prediction (S.M.A.R.T.)

DPLA-2xxxx supports S.M.A.R.T. function. The details are described in 10.6, “S.M.A.R.T. Function” on page 76 and 12.30, “S.M.A.R.T. Function Set (B0h)” on page 144.

5.3.3 Cable Noise Interference

To avoid any degradation of performance throughput or error when the interface cable is routed on top or comes in contact with the HDA assembly, the drive must be grounded electrically to the system frame by four screws. The common mode noise or voltage level difference between the system frame and power cable ground or AT interface cable ground should be in the allowable level specified in the power requirement section.

5.3.4 Drive Usage Condition

The drive is designed to be used under the following conditions.

- Within specifications of Shock, Vibration, Temperature, Humidity, Altitude, and Magnetic Field.
- ESD protective handling.
- Without covering breathing hole on top cover.
- Without pressing top cover.
- Less than 140 power-on hours per month.
- Seeking/Writing/Reading operation be less than 20% of power-on hours.
- The power requirements be satisfied.
- Drive frame be grounded electrically to the system through four screws.
- Mounting with recommended screw depth and torque.
- Interface physical and electrical requirements be satisfied per ATA-3.
- Power off sequence according to 5.3.6.2, “ Required Power-Off Sequence” on page 24.

Actual product life and failure rate depend on duty cycle and environmental conditions. Consult your IBM representative for reliability estimate if atypical operating conditions are anticipated.

5.3.5 Preventive Maintenance

None.

5.3.6 Load/Unload

The product supports a minimum of 300,000 normal load/unloads.

Load/unload is a functional mechanism of the HDD. It is controlled by the drive microcode. Specifically, unloading of the heads is invoked by the commands:

- Soft Reset
- Standby
- Standby Immediate
- Sleep

Load/unload is also invoked as one of the idle modes of the drive.

The specified start/stop life of the product assumes that load/unload is operated normally, **not in emergency mode**.

5.3.6.1 Emergency Unload

When HDD power is interrupted while the heads are still loaded, the microcode cannot operate and the normal 5v power is unavailable to unload the heads. In this case, normal unload is not possible, so the heads are unloaded by routing the back-EMF of the spinning motor to the voice coil. The actuator velocity is greater than the normal case, and the unload process is inherently less controllable without a normal seek current profile.

Emergency unload is intended to be invoked in rare situations. Because this operation is inherently uncontrolled, it is more mechanically stressful than a normal unload.

A single emergency unload operation is more stressful than 100 normal unloads. Use of emergency unload reduces the start/stop life of the HDD at a rate at least 100x faster than that of normal unload, and may damage the HDD.

Warranty is void on a drive that has experienced 3000 or more emergency unloads.

5.3.6.2 Required Power-Off Sequence

The required BIOS sequence for removing power from DPLA-2xxxx is:

- Step 1: Issue one of the following commands.
 - Soft Reset
 - Standby
 - Standby Immediate
 - Sleep

Note: Do **not** use Flush Cache command for power off sequence, because the command does not invoke Unload.

- Step 2: **Wait** until **Command Complete** Status is returned.

In typical case, it takes 350ms for the command completion, however, BIOS time out value needs to be 30sec considering error recovery time. Refer to 13.0, “Timings” on page 171 for time out values.

- Step 3: Terminate power to HDD.

This power-down sequence should be followed for entry into any system power-down state, or system suspend state, or system hibernation state. In a robustly designed system, emergency unload is limited to rare scenarios such as battery removal during operation.

5.3.6.3 Power Switch Design Considerations

In systems that use DPLA-2xxxx consideration should be given to the design of the system power switch.

IBM recommends that the switch operate under control of the Bios, as opposed to being 'hard wired'. The same recommendation is made for 'cover-close' switches. When a hard wired switch is turned off, emergency unload occurs, as well as the problems cited in 4.1, "Data Loss by Power Off" on page 15 and 4.2, "Write Cache" on page 15.

5.3.6.4 Test Considerations

Start/stop testing is classically performed to verify head/disk durability. In the case of DPLA-2xxxx the heads do not land on the disk, so this type of test should be viewed as a test of the load/unload function.

Start/Stop testing should be done **by commands** through the interface, **Not by power cycling** the drive. Simple power cycling of DPLA-2xxxx invokes the emergency unload mechanism, and subjects the HDD to non-typical mechanical stress.

Power cycling testing may be required to test the boot-up function of the system. In this case IBM recommends that the power-off portion of the cycle contain the sequence specified in 5.3.6.2, "Required Power-Off Sequence" on page 24. Again, if this is not done, the emergency unload function is invoked and non-typical stress results.

5.4 Mechanical Specifications

5.4.1 Mechanical Dimensions and Weight

The following chart describes the dimensions for the 2.5" hard disk drive form factor.

	DPLA-24480 / DPLA-25120
Height (mm)	17.0 +0.0/-0.5
Width (mm)	69.85 ± 0.25
Length (mm)	100.2 ± 0.25
Weight (gram)	180 Typical

Figure 17. Physical Dimension and Weight

5.4.2 Hole Locations

The Figure 18 on page 26 shows the outline of DPLA-24480/25120 which includes the hole locations.

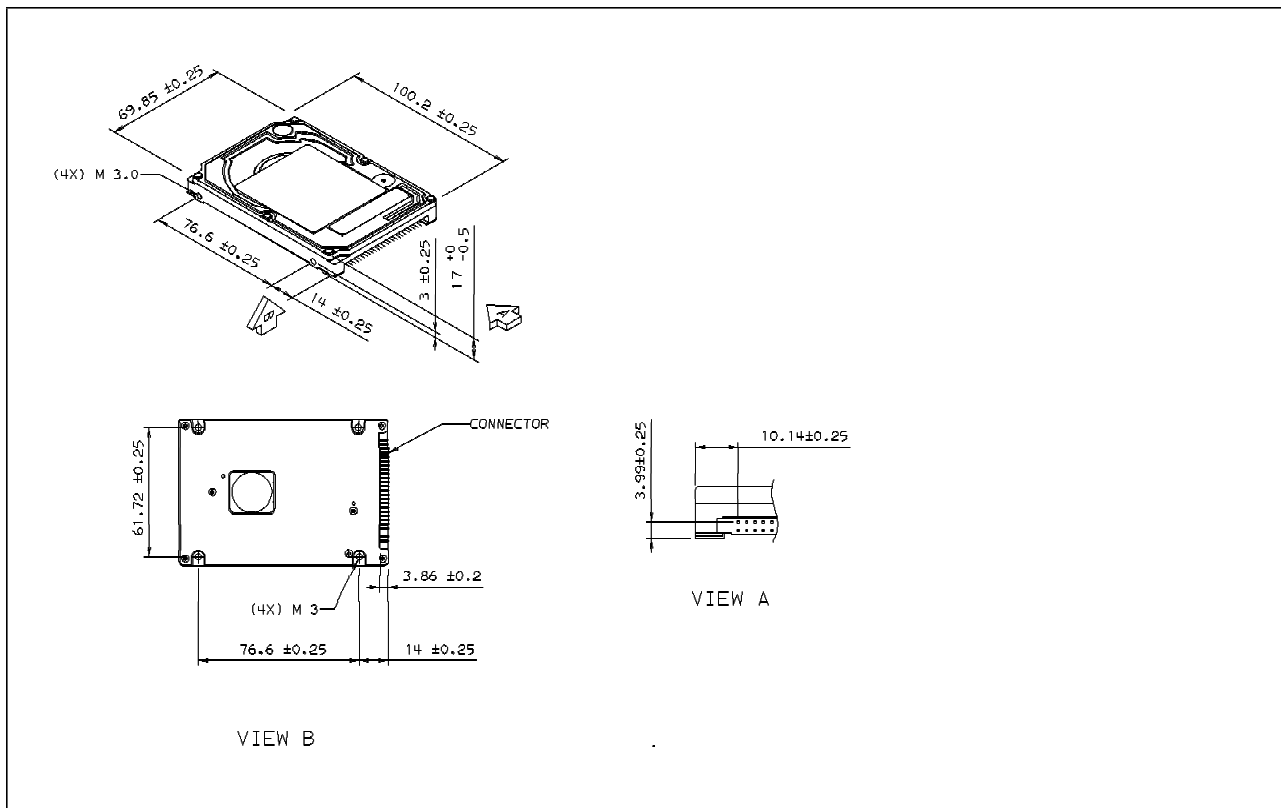


Figure 18. Outline of DPLA-24480/25120

5.4.3 Mounting Orientation

The drive will operate in all axes (6 directions). The drive will operate within the specified error rates when tilted ± 5 degree from these positions.

Performance and error rate will stay within specification limits if the drive is operated in the other permissible orientations from which it was formatted. Thus a drive formatted in a horizontal orientation will be able to run vertically and vice versa.

The recommended mounting screw torque is 3 ± 0.5 kgf.cm.

The recommended mounting screw depth is 3.0 ± 0.3 mm for bottom and 3.5 ± 0.5 mm for horizontal mounting.

The system is responsible for mounting the drive securely enough to prevent excessive motion or vibration of the drive at seek operation or spindle rotation, using appropriate screws or equivalent mounting hardware.

Vibration test and shock test are to be conducted by mounting the drive to the table using the bottom four screws.

5.5 Vibration and Shock

All vibration and shock measurements in this section shall be for the disk drive without the mounting attachments for the systems. The input level shall be applied to the normal drive mounting points.

5.5.1 Operating Vibration

The disk drive will operate without a hard error while being subjected to the following vibration levels.

5.5.1.1 Random Vibration

The measurements are carried out with vibration test level 0.67G RMS (Root Mean Square) during 30 minutes of random vibration using the power spectrum density (PSD) as follows.

Random vibration PSD profile Breakpoint

5 Hz	2.0 x E-5	g**2/Hz
17 Hz	1.1 x E-3	
45 Hz	1.1 x E-3	
48 Hz	8.0 x E-3	
62 Hz	8.0 x E-3	
65 Hz	1.0 x E-3	
150 Hz	1.0 x E-3	
200 Hz	5.0 x E-4	
500 Hz	5.0 x E-4	

The specified levels are measured at the mounting points.

5.5.1.2 Swept Sine Vibration

- 1 G (Zero to peak), 5 to 500 to 5 Hz sine wave
- 1.0 oct/min sweep rate

5.5.2 Non-Operating Vibration

5.5.2.1 Random Vibration

The test consists of a random vibration applied in each of three mutually perpendicular axes with the time duration of 15 minutes per axis. The PSD levels for the test simulates the shipping and relocation environment which is shown below.

Hz	Random Vibration PSD Profile Breakpoints (Non-Operating)			
Hz	2.5	5	40	500
G**2/Hz	0.001	0.03	0.018	0.018

Overall RMS level of vibration is 3.01G (RMS).

5.5.2.2 Swept Sine Vibration

- 25.4mm (peak to peak) displacement, 5 to 10 to 5 Hz
- 5 G (zero to peak), 10 to 500 to 10 Hz sine wave
- 0.5 oct/min sweep rate

5.5.3 Operating Shock

The hard disk drive meets the following criteria while operating in the conditions described below. The shock test consists of ten shock inputs in each axis and direction for a total of 60. There must be a minimum 3 seconds delay between shock pulses. Soft errors and automatic retries are allowed during the test.

No data loss or permanent damage : 100G/2msec half-sine shock pulse, 10G/11msec half-sine shock pulse

The input level shall be applied to the normal disk drive subsystem mounting points, as mounted in normal system use.

5.5.4 Non-Operating Shock

The disk drive must withstand with no damage or degradation of performance, a 120G half-sine wave shock pulse of 11 ms duration and a 400G half-sine wave shock pulse of 2 ms duration on six sides when heads are parked. (When the power is not applied to the unit, the heads are automatically located on the parked position.)

All shocks shall be applied in each direction of the drive's three mutually perpendicular axes, one axis at a time. Input levels shall be measured at the frame of the disk drive.

5.6 Acoustics

5.6.1 Sound Power Level

The criteria of A-weighted sound power level is described below.

Measurements are to be taken in accordance with ISO 7779. The mean of 40 drives is to be less than the typical value. Each drive is to be less than the maximum value. Drives are to meet this requirement in both board down orientations.

A-weighted Sound Power (Bels)	Typical	Maximum
Idle	3.7	4.0
Operating	4.0	4.3

Background power levels of the acoustic test chamber for each octave band are to be recorded.

Sound power tests are to be conducted with the drive supported by spacers so that the lower surface of the drive be located at 25 +/- 3mm height from the chamber floor. No sound absorbing material shall be used.

The acoustical characteristics of the disk drive are measured under the following conditions.

Idle mode :

Power on, disks spinning, track following, unit ready to receive and respond to control line commands.

Operating mode :

Continuous random cylinder selection and seek operation of actuator with a dwell time at each cylinder. Seek rate for the drive can be calculated as shown below.

$$N_s = 0.4 / (T_t + T_1)$$

where:

- N_s : Average seek rate in seeks/s.
 T_t : Published seek time from one random track to another without including rotational latency.
 T_1 : Equivalent time, in seconds, for the drive to rotate by half a revolution.

5.6.2 Discrete Tone Penalty

Discrete tone penalties are added to the A-weighted sound power (L_w) with following formula only when determining compliance.

$$L_{wt(spec)} = L_w + 0.1 * P_t + 0.3 < 4.0 \text{ (Bels)}$$

where:

L_w : A-weighted sound power level.

P_t : Value of discrete tone penalty = $dL_t - 6.0$ (dBA)

dL_t : Tone-to-noise ratio taken in accordance with ISO 7779. at each octave band.

5.7 Identification

5.7.1 Labels

The following labels are affixed to every disk drive .

1. A label placed on the top of the HDA containing the statement 'Made by IBM' or equivalent, Part No., EC No. and FRU No.
2. A bar code label placed on the disk drive based on user request. The location on the disk drive is to be designated in the drawing.
3. Labels containing the vendor's name, disk drive model number, serial number, place of manufacture and UL/CSA logos.

5.8 Electromagnetic Compatibility

The drive, when installed in a suitable enclosure and exercised with a random accessing routine at maximum data rate, shall meet the worldwide EMC requirements listed below.

IBM will provide technical support to assist users in complying with the EMC requirements.

- United States Federal Communications Commission (FCC) Rules and Regulations (Class B), Part 15.
- European Economic Community (EEC) directive number 76/889 related to the control of radio frequency interference and the Verband Deutscher Elektrotechniker (VDE) requirements of Germany (GOP).

5.8.1 CE Mark

The product is certified for compliance to EC directive 89/336/EEC. CE marking for the certification appears on the drive.

5.8.2 C-Tick Mark

The product complies with the following Australian EMC standard.

- Limits and methods of measurement of radio disturbance characteristics of information technology equipment, AS/NZS 3548:1995 Class B.

5.9 Safety

5.9.1 Underwriters Lab(UL) Approval

DPLA-24480/25120 complies with UL 1950.

5.9.2 Canadian Standards Authority(CSA) Approval

DPLA-24480/25120 complies with CSA C22.2, #950-M1993.

5.9.3 IEC Compliance

DPLA-24480/25120 complies with IEC 950.

5.9.4 German Safety Mark

DPLA-24480/25120 are approved by TUV on Test Requirement:

EN 60 950:1988/A1:1990/A2:1991.

5.9.5 Flammability

Printed Circuit boards used in this product are made of material with a UL recognized flammability rating of V-1 or better. The flammability rating is marked or etched on the board. All other parts not considered electrical components are made of material with a UL recognized flammability rating of V-1 or better except minor mechanical parts.

5.9.6 Secondary Circuit Protection

This product utilizes printed circuit wiring that must be protected against the possibility of sustained combustion due to circuit or component failure. Adequate secondary over current protection is the responsibility of the using system.

User must protect the drive from it's electrical short circuit problem. 10 A limit is required for safety purpose.

5.10 Packaging

Drives will be shipped in appropriate containers and placed on pallets.

Drives are shipped in ESD protective bags.

6.0 Electrical Interface Specifications

6.1 Cabling

The maximum cable length from the host system to the drive plus circuit pattern length in the host system shall not exceed 18 inches.

6.2 Interface Connector

The signal connector for AT Attachment is designed to mate with Dupont part number 69764-044 or equivalent.

Figure 20 and Figure 18 show the connector location and physical pin location.

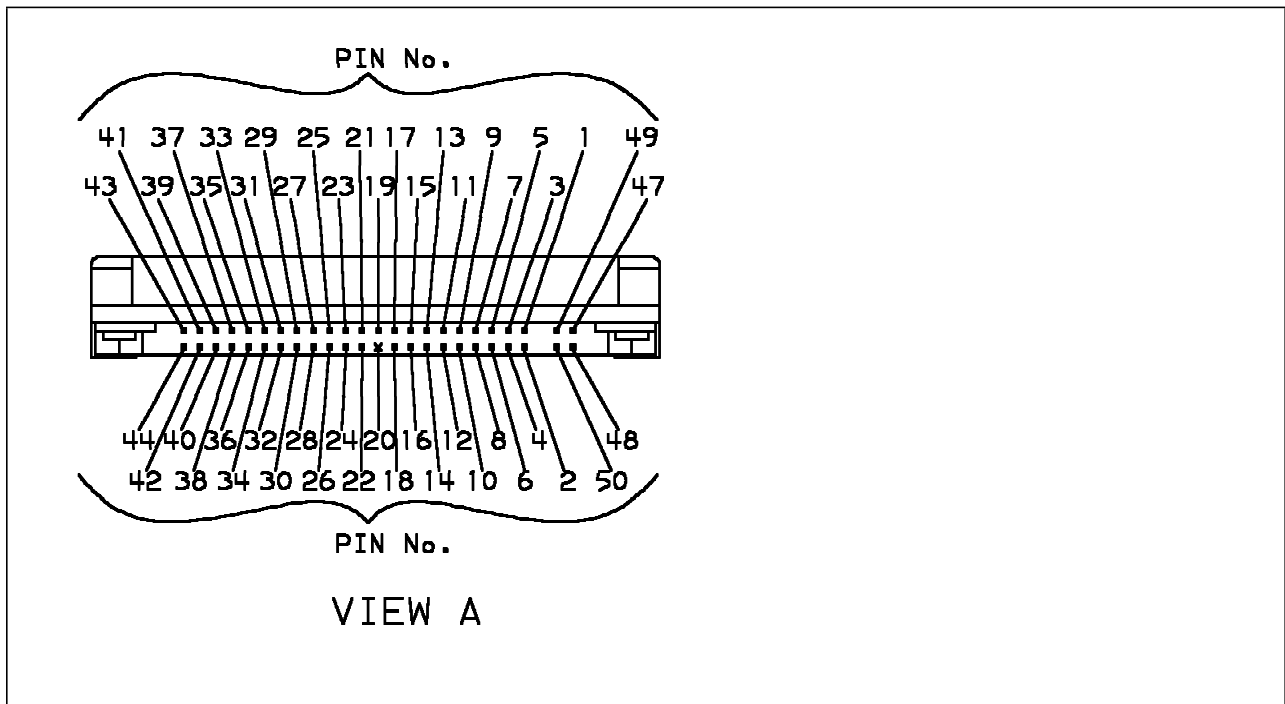


Figure 20. AT Attachment connector of DPLA-24480/25120

Note 1 : Pin position 20 is left blank for correct connector insertion.

Note 2 : Pin position 47 through 50 are used for drive address setting. (Refer to Figure 35 on page 52 for address setting.)

6.2.1 Signal Definition

The pin assignments of interface signals are listed as follows:

PIN	SIGNAL	I/O	Type	PIN	SIGNAL	I/O	Type
01	-RESET	I	TTL	02	GND		
03	DD07	I/O	3-state	04	DD08	I/O	3-state
05	DD06	I/O	3-state	06	DD09	I/O	3-state
07	DD05	I/O	3-state	08	DD10	I/O	3-state
09	DD04	I/O	3-state	10	DD11	I/O	3-state
11	DD03	I/O	3-state	12	DD12	I/O	3-state
13	DD02	I/O	3-state	14	DD13	I/O	3-state
15	DD01	I/O	3-state	16	DD14	I/O	3-state
17	DD00	I/O	3-state	18	DD15	I/O	3-state
19	GND			(20)	Key		
21	DMARQ	0	3-state	22	GND		
23	-DIOW(*)	I	TTL	24	GND		
25	-DIOR(*)	I	TTL	26	GND		
27	IORDY(*)	0	3-state	28	CSEL	I	TTL
29	-DMACK	I	TTL	30	GND		
31	INTRQ	0	3-state	32	-HIOCS16	0	OC
33	DA01	I	TTL	34	-PDIAG	I/O	OC
35	DA00	I	TTL	36	DA02	I	TTL
37	-CS0	I	TTL	38	-CS1	I	TTL
39	-DASP	I/O	OC	40	GND		
41	+5V Logic	PWR		42	+5V MOTOR	PWR	
43	GND			44	(Resv)		

Figure 21. Table of signals

Notes:

1. "O" designates an output from the Drive.
2. "I" designates an input to the Drive.
3. "I/O" designates an input/output common.
4. "OC" designates Open-Collector or Open-Drain output.
5. The signal lines marked with (*) are redefined during the Ultra DMA protocol to provide special functions. These lines change from the conventional to special definitions at the moment the Host decides to allow a DMA burst, if the Ultra DMA transfer mode was previously chosen via SetFeatures. The Drive becomes aware of this change upon assertion of the -DMACK line. These lines revert back to their original definitions upon the deassertion of -DMACK at the termination of the DMA burst.

	Special Definition (for Ultra DMA)	Conventional Definition
Write Operation	-DDMARDY HSTROBE STOP	IORDY -DIOR -DIOW
Read Operation	-HDMARDY DSTROBE STOP	-DIOR IORDY -DIOW

Figure 22. Signal Special Definitions for Ultra DMA

- DD00-DD15** 16-bit bi-directional data bus between the host and the HDD. The lower 8 lines, DD00-07, are used for Register and ECC access. All 16 lines, DD00-15, are used for data transfer. These are 3-State lines with 24 mA current sink capability.
- DA00-DA02** Address used to select the individual register in the HDD.
- CS0** Chip select signal generated from the Host address bus. When active, one of the Command Block Registers (Data, Error{Features when written}, Sector Count, Sector Number, Cylinder Low, Cylinder High, Drive/Head and Status{Command when written} register) can be selected.
(See Figure 36 on page 53.)
- CS1** Chip select signal generated from the Host address bus. When active, one of the Control Block Registers (Alternate Status{Device Control when written} and Drive Address register) can be selected.
(See Figure 36 on page 53.)
- RESET** This line is used to reset the HDD. It shall be kept Low logic state during power up and kept High thereafter.
- DIOW** Its rising edge holds data from the host data bus to a register or data register of the HDD.
- DIOR** When low, this signal enables data from a register or data register of the drive onto data bus. The data on the bus shall be latched on the rising edge of -DIOR.
- INTRQ** Interrupt is enabled only when the drive is selected, and the host activates the -IEN bit in the Device Control Reg. Otherwise, this signal is in high impedance state regardless of the state of the IRQ bit. The interrupt is set when the IRQ bit is set by the drive CPU. IRQ is reset to zero by a host read of the status register or a write to the Command Reg. This signal is a 3-State line with 24 mA sink capability.
- HIOCS16** Indication to the host that a 16-bit wide data register has been addressed and that the drive is prepared to send or receive a 16-bit wide data word. This signal is an Open-Drain output with 24 mA sink capability and an external resistor is needed to pull this line to 5 volts.
- DASP** This is a time-multiplexed signal which indicates that a drive is active, or that device 1 is present. This signal is driven by Open-Drain driver and internally pulled-up to 5 volts through a 10k Ω resistor.
During Power-On initialization or after -RESET is negated, -DASP shall be asserted by Device 1 within 400 msec to indicate that device 1 is present. Device 0 shall allow up to 450msec for device 1 to assert -DASP. If device 1 is not present, device 0 may assert -DASP to drive a LED indicator.
-DASP shall be negated following acceptance of the first valid command by device 1. Anytime after negation of -DASP, either drive may assert -DASP to indicate that a drive is active.
- PDIAG** This signal shall be asserted by device 1 to indicate to device 0 that it has completed diagnostics. This line is pulled-up to 5 volts in the HDD through a 10k Ω resistor.
Following a Power On Reset, software reset or -RESET, drive 1 shall negate -PDIAG within 1 msec (to indicate to device 0 that it is busy). Drive 1 shall then assert -PDIAG within 30 seconds to indicate that it is no longer busy, and is able to provide status.
Following the receipt of a valid Execute Drive Diagnostics command, device 1 shall negate -PDIAG within 1 msec to indicate to device 0 that it is busy and has not yet passed its drive diagnostics. If device 1 is present then device 0 shall wait up to 6 seconds from the receipt of a valid Execute Drive Diagnostics command for drive 1 to assert -PDIAG. Device 1 should clear BSY before asserting -PDIAG, as -PDIAG is used to indicate that device 1 has passed its diagnostics and is ready to post status.
If -DASP was not asserted by device 1 during reset initialization, device 0 shall post its own status immediately after it completes diagnostics, and clear the device 1 Status register to

00h. Device 0 may be unable to accept commands until it has finished its reset procedure and is ready (DRDY=1).

CSEL (Cable Select) (Optional)

The drive is configured as either Device 0 or 1 depending upon the value of CSEL.

- If CSEL is grounded then the device address is 0.
- If CSEL is open then the device address is 1.

KEY

Pin position 20 has no connection pin. It is recommended to close the respective position of the cable connector in order to avoid incorrect insertion by mistake.

IORDY

This signal is negated to extend the host transfer cycle when a drive is not ready to respond to a data transfer request, and may be negated when the host transfer cycle is less than 240 nsec for PIO data transfer. This signal is a 3-state line with 24 mA sink capability and an external resistor is needed to pull this line to 5 volts.

-DMACK

This signal shall be used by the host in response to DMARQ to either acknowledge that data has been accepted, or that data is available.

This signal is internally pulled-up to 5Volt through 15 K ohm resistor and the tolerance of the resistor value is -50% to +100% .

DMARQ

This signal, used for DMA data transfers between host and drive, shall be asserted by the drive when it is ready to transfer data to or from the host. The direction of data transfer is controlled by -HIOR and -HIOW. This signal is used on a handshake manner with -DMACK. This signal is a 3-state line with 24mA sink capability and internally pulled-down to GND through 10 kΩ resistor.

-HDMARDY (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive.

-HDMARDY is a flow control signal for Ultra DMA data in bursts. This signal is held asserted by the host to indicate to the device that the host is ready to receive Ultra DMA data in transfers. The host may negate -HDMARDY to pause an Ultra DMA data in transfer.

HSTROBE (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive.

HSTROBE is the data out strobe signal from the host for an Ultra DMA data out transfer. Both the rising and falling edge of HSTROBE latch the data from DD(15:0) into the device. The host may stop toggling HSTROBE to pause an Ultra DMA data out transfer.

STOP (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive.

STOP shall be asserted by the host prior to initiation of an Ultra DMA burst. STOP shall be negated by the host before data is transferred in an Ultra DMA burst. Assertion of STOP by the host during or after data transfer in an Ultra DMA mode signals the termination of the burst.

-DDMARDY (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive.

-DDMARDY is a flow control signal for Ultra DMA data out bursts. This signal is held asserted by the device to indicate to the host that the device is ready to receive Ultra DMA data out transfers. The device may negate -DDMARDY to pause an Uptra DMA data out transfer.

DSTROBE (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive.

DSTROBE is the data int strobe signal from the device for an Ultra DMA data in transfer. Both the rising and falling edge of DSTROBE latch the data from DD(15:0) into the host. The device may stop toggling DSTROBE to pause an Ultra DMA data in transfer.

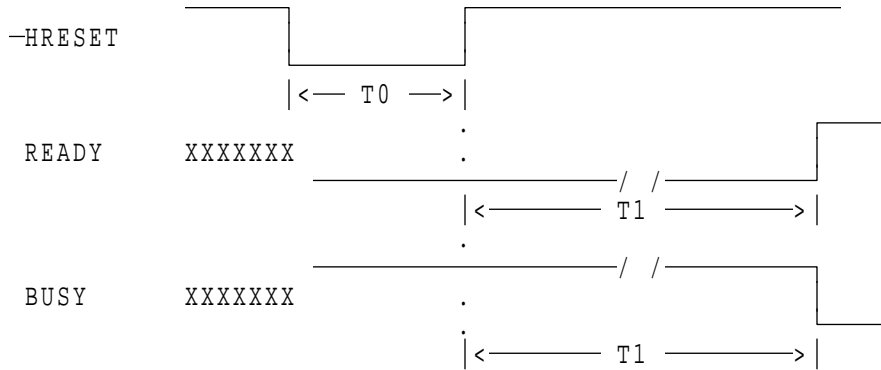
6.3 Interface Logic Signal Levels

The interface logic signal have the following electrical specifications:

Inputs :	Input High Voltage	–	2.0 V min./ Vcc+0.7 V max.
	Input Low Voltage	–	–0.5 V min./ 0.8 V max.
Outputs :	Output High Voltage	–	2.4 V min.
	Output Low Voltage	–	0.5 V max.
Current :	Driver Sink Current	–	24 mA min.
	Driver Source Current	–	–400 uA min.

6.4 Reset timings

HDD reset timing.

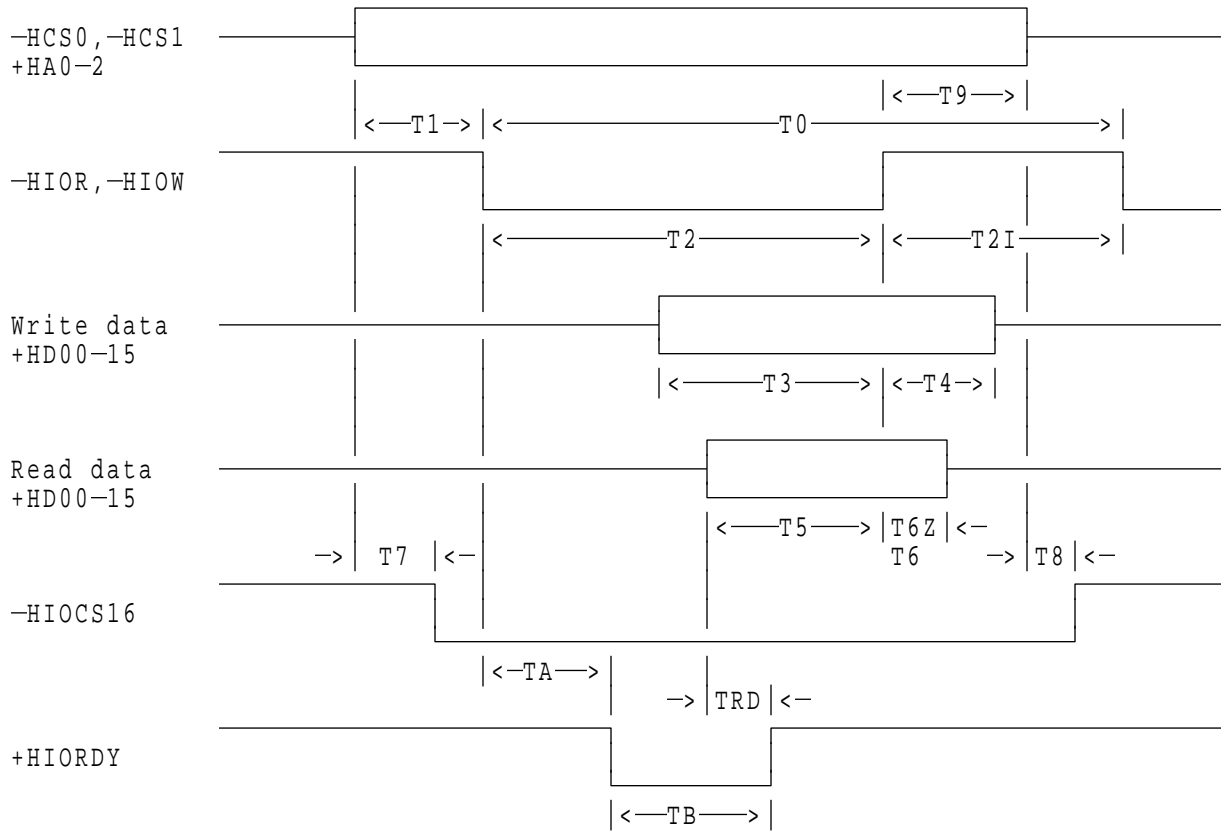


	PARAMETER DESCRIPTION	Min (usec)	Typ (sec)	Max (sec)
T0	-HRESET low width	25	—	—
T1	-HRESET high to READY/Not BUSY	—	2.3	9.5

Figure 23. System Reset timing

6.5 PIO Timings

The PIO cycle timings meet Mode 4 of the ATA-3 description.



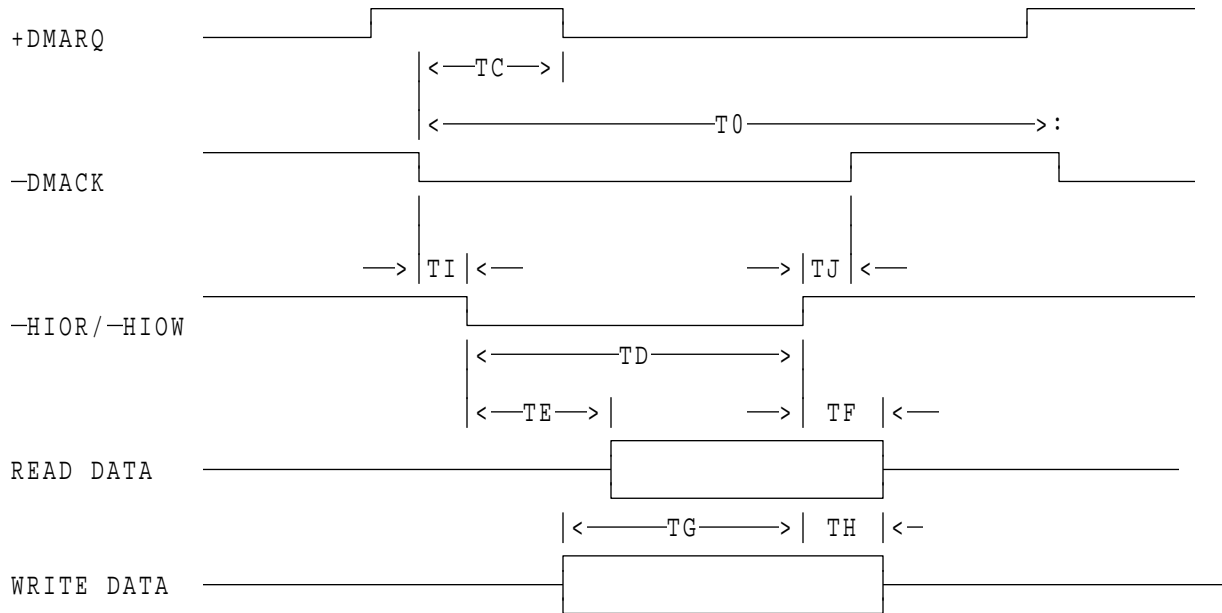
	PARAMETER DESCRIPTION	MIN (nsec)	MAX (nsec)	Note
T0	Cycle time	120	—	
T1	$\overline{\text{HCS0-1}}, +\text{HA00-02}$ valid to $\overline{\text{HIOR}}, \overline{\text{HIOW}}$ active	25	—	
T2	$\overline{\text{HIOR}}, \overline{\text{HIOW}}$ pulse width	70	—	
T2I	$\overline{\text{HIOR}}, \overline{\text{HIOW}}$ recovery	25	—	
T3	$+\text{HD00-15}$ setup to $\overline{\text{HIOW}}$ high	20	—	
T4	$\overline{\text{HIOW}}$ high to $+\text{HD00-15}$ hold	10	—	
T5	$+\text{HD00-15}$ setup to $\overline{\text{HIOR}}$ high	20	—	*1
T6	$\overline{\text{HIOR}}$ high to $+\text{HD00-15}$ hold	5	—	
T6Z	$\overline{\text{HIOR}}$ high to $+\text{HD00-15}$ tristate	—	30	
T7	$\overline{\text{HCS0-1}}, +\text{HA00-02}$ valid to $\overline{\text{HIOCS16}}$ assertion	—	30	
T8	$\overline{\text{HCS0-1}}, +\text{HA00-02}$ invalid to $\overline{\text{HIOCS16}}$ negation	—	30	
T9	$\overline{\text{HIOR}}, \overline{\text{HIOW}}$ high to $\overline{\text{HCS0-1}}, +\text{HA00-02}$ hold	10	—	
TRD	Read data valid to $+\text{HIORDY}$ active	0	—	
TA	$\overline{\text{HIOR}}, \overline{\text{HIOW}}$ low to $+\text{HIORDY}$ low	—	35	
TB	$+\text{HIORDY}$ pulse width	—	1250	

Note *1 : This value is applied only when $+\text{HIORDY}$ is not negated. When $+\text{HIORDY}$ is negated, TRD is applied.

Figure 24. PIO cycle timings

6.5.1 DMA Timings (Single Word)

The Single Word DMA timing meets Mode 2 of the ATA-3 description.

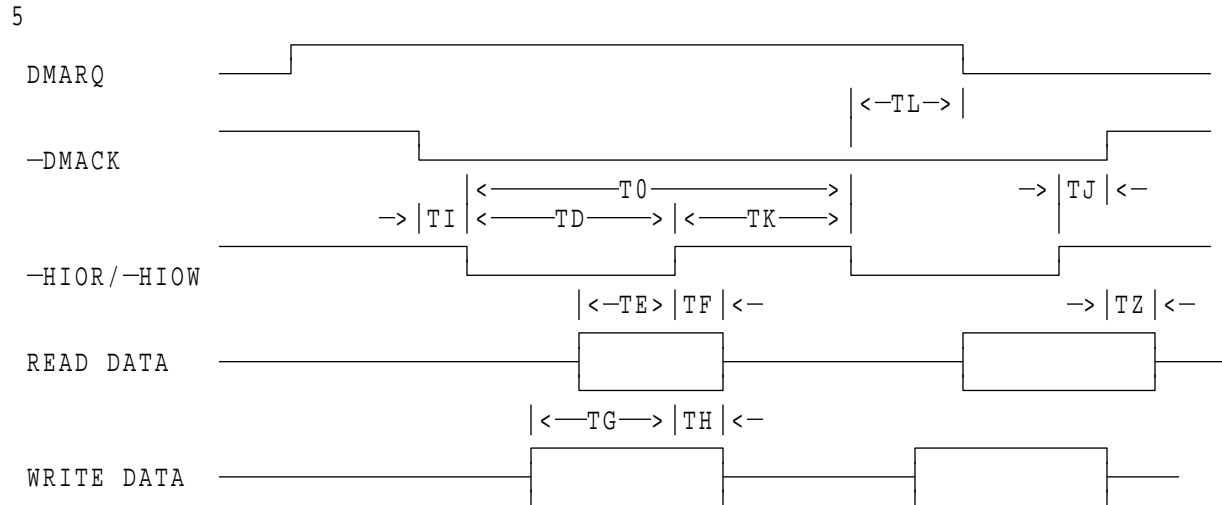


	PARAMETER DESCRIPTION	MIN (nsec)	MAX (nsec)	Note
T0	Cycle time	240	—	
TC	-DMA active to +DMARQ inactive	—	80	
TD	-HIOR, -HIOW pulse width	120	—	
TE	-HIOR data access	—	60	
TF	-HIOR data hold	5	—	
TG	-HIOW data setup	35	—	
TH	-HIOW data hold	20	—	
TI	-DMACK to -HIOR/-HIOW setup	0	—	
TJ	-HIOR/-HIOW to -DMACK hold	0	—	

Figure 25. DMA (Single Word) cycle timings

6.5.2 DMA Timings (Multiword)

The Multiword DMA timing meets Mode 2 of the ATA-3 description.



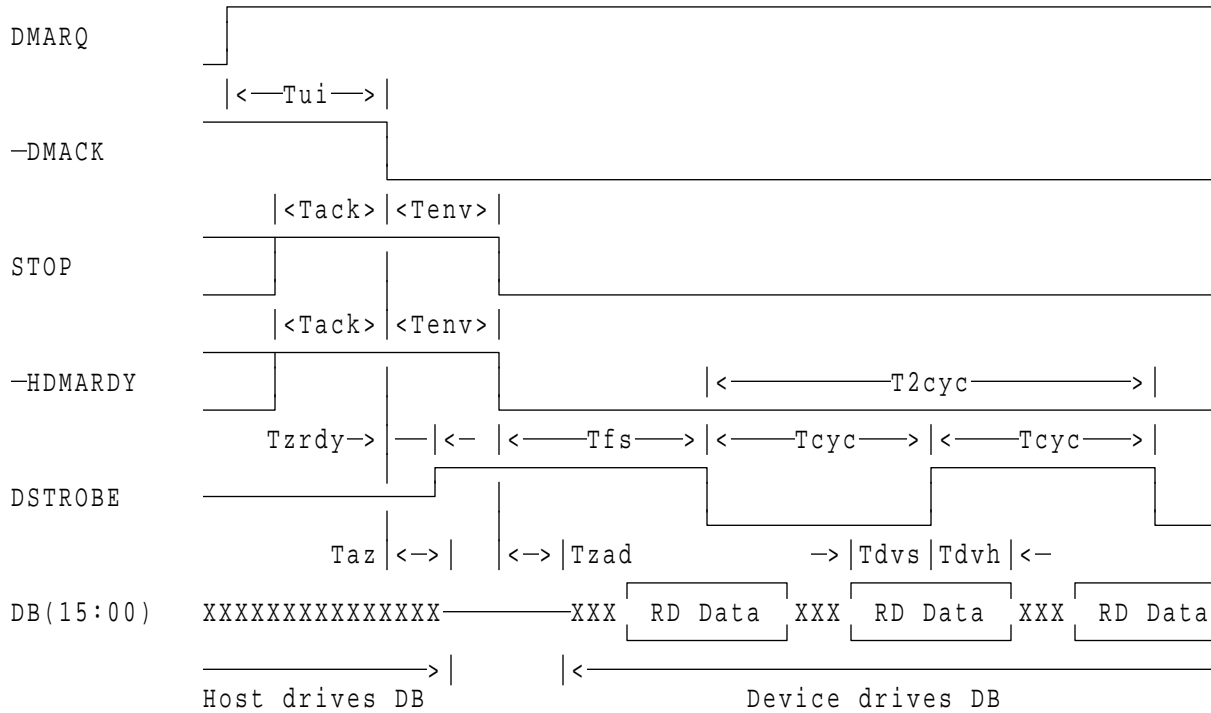
	PARAMETER DESCRIPTION	MIN (nsec)	MAX (nsec)	Note
T0	Cycle time	120	—	
TD	-HIOR,-HIOW pulse width	70	—	
TE	-HIOR data setup	20	—	
TF	-HIOR data hold	5	—	
TG	-HIOW data setup	20	—	
TH	-HIOW data hold	10	—	
TI	-DMACK to -HIOR/-HIOW setup	0	—	
TJ	-HIOR/-HIOW to -DMACK hold	5	—	
TK	-HIOR/-HIOW negated pulse width	25	—	
TL	-HIOR/-HIOW to -DMARQ delay	—	35	
TZ	-DMACK to tristate	—	25	

Figure 26. DMA (Multi Word) cycle timings

6.5.3 Ultra DMA Timings

The Ultra DMA timing meets Mode 0, 1 and 2 of the Ultra DMA/33 -- a Proposal for a New Protocol in ATA/ATAPI-4 (X3T13/D96153 Revision 1)

6.5.3.1 Initiating Read DMA

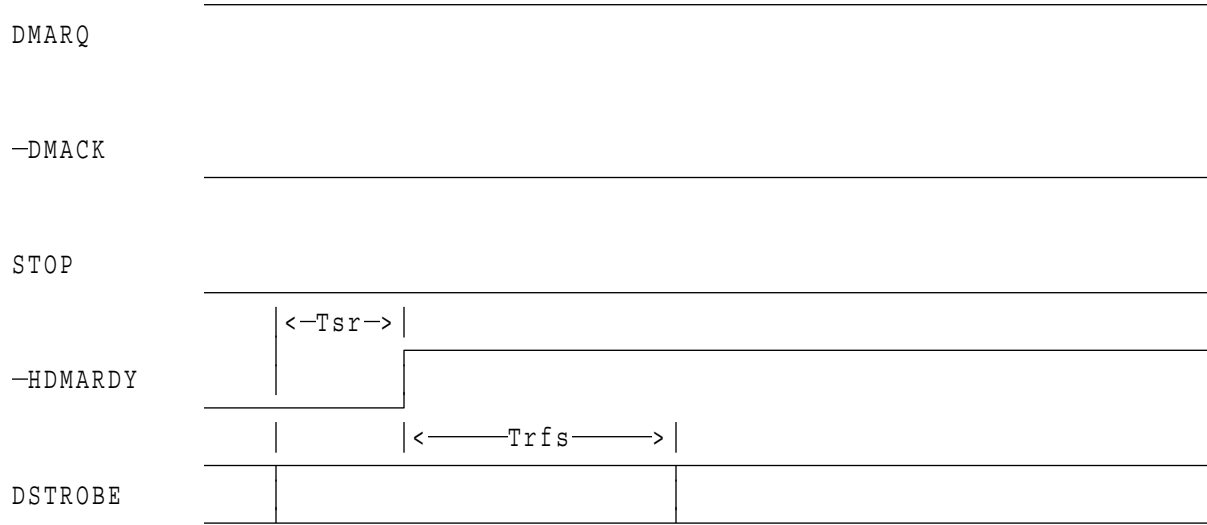


[nsec]

PARAMETER DESCRIPTION	MODE0		MODE1		MODE2	
	MIN	MAX	MIN	MAX	MIN	MAX
Tui	0	—	0	—	0	—
Tack	20	—	20	—	20	—
Tenv	20	70	20	70	20	70
Tzrdy	0	—	0	—	0	—
Tfs	0	230	0	200	0	170
Tcyc	114	—	75	—	55	—
T2cyc	235	—	156	—	117	—
Taz	—	10	—	10	—	10
Tzad	0	—	0	—	0	—
Tdvs	70	—	48	—	34	—
Tdvh	6	—	6	—	6	—

Figure 27. Ultra DMA cycle timings (Initiating Read)

6.5.3.2 Host Pausing Read DMA



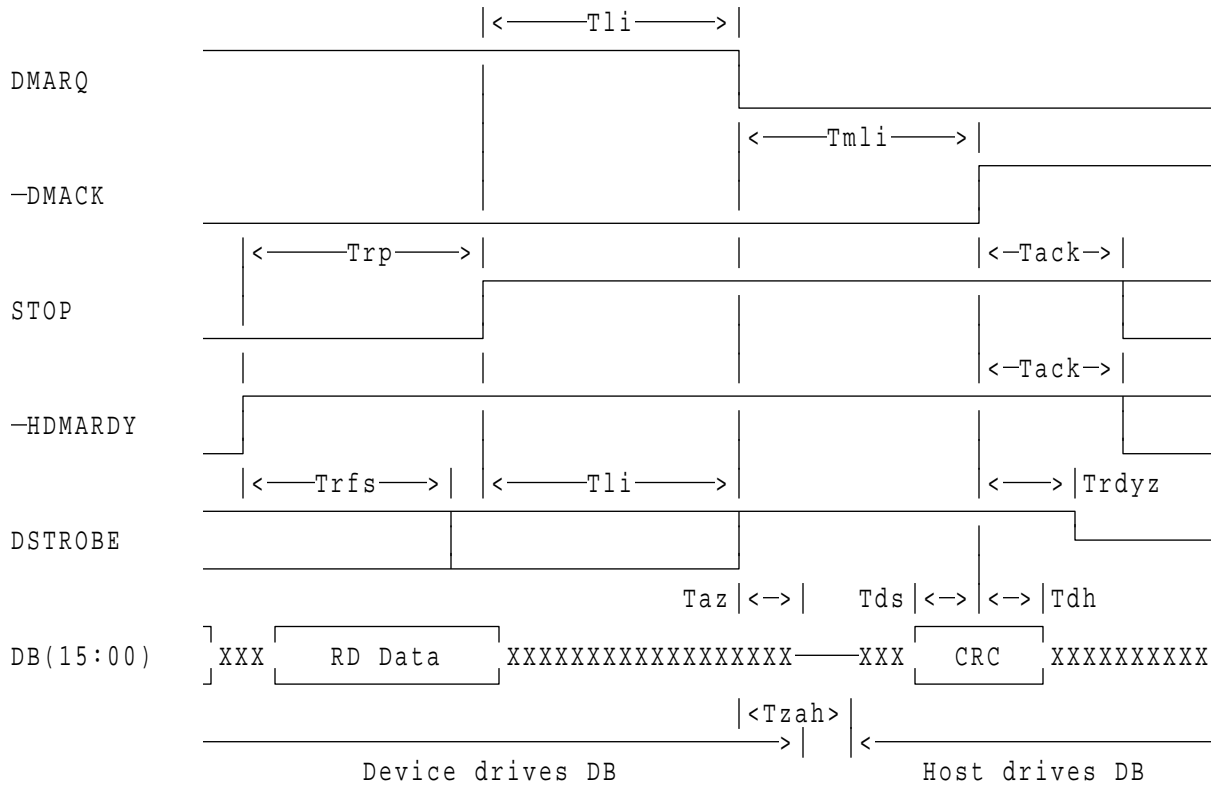
[nsec]

	PARAMETER DESCRIPTION	MODE0		MODE1		MODE2	
		MIN	MAX	MIN	MAX	MIN	MAX
Tsr	Strobe to ready response time	—	50	—	30	—	20
Trfs	Ready to final strobe time	—	75	—	60	—	50

Note : When a host does not meet Tsr, it should be ready to receive 2 more strobes after -HDMARDY is negated.

Figure 28. Ultra DMA cycle timings (Host pausing Read)

6.5.3.3 Host Terminating Read DMA

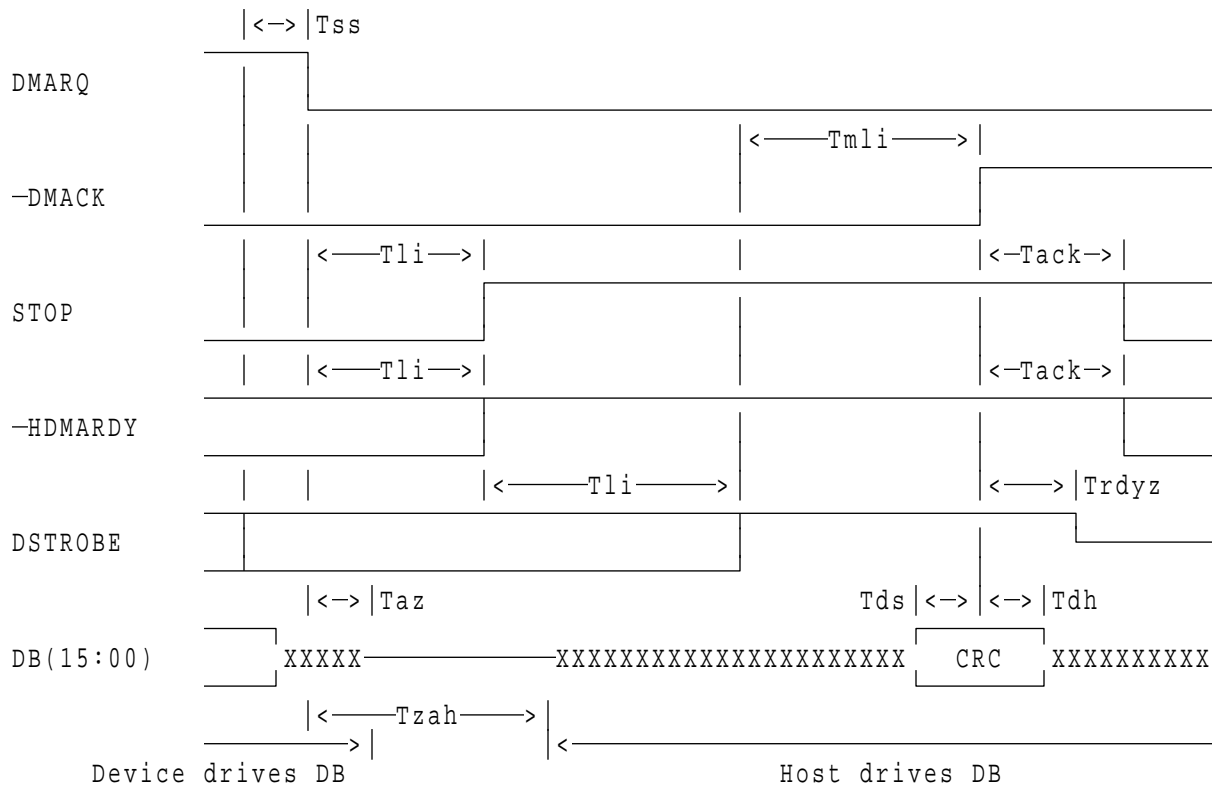


[nsec]

	PARAMETER DESCRIPTION	MODE0		MODE1		MODE2	
		MIN	MAX	MIN	MAX	MIN	MAX
Trfs	Ready to final strobe time	-	75	-	60	-	50
Trp	Ready to pause time	160	-	125	-	100	-
Tli	Limited interlock time	0	150	0	150	0	150
Taz	Output release time	-	10	-	10	-	10
Tzah	Output enable time	20	-	20	-	20	-
Tmli	Interlock time	20	-	20	-	20	-
Tds	Data setup time (at device side)	15	-	10	-	7	-
Tdh	Data Hold time (at device side)	5	-	5	-	5	-
Tack	Hold time after -DMACK negation	20	-	20	-	20	-
Trdyz	Pull-up time before DSTROBE release	-	20	-	20	-	20

Figure 29. Ultra DMA cycle timings (Host terminating Read)

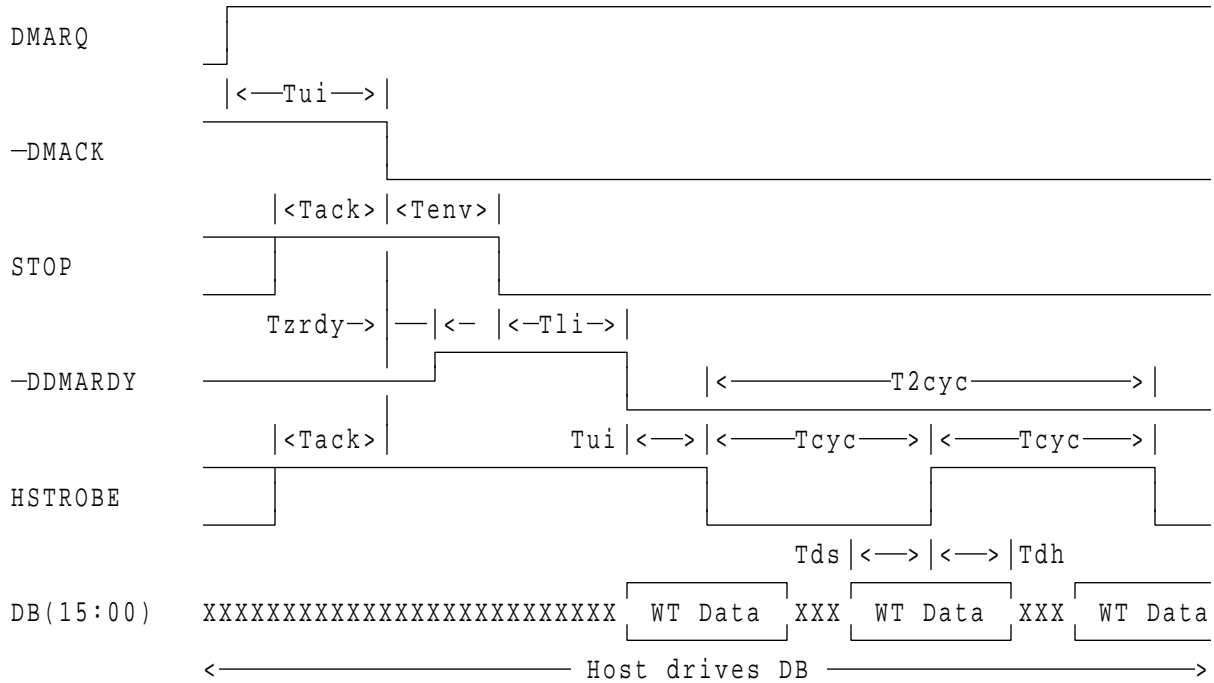
6.5.3.4 Device Terminating Read DMA



	PARAMETER DESCRIPTION	MODE0		MODE1		MODE2	
		MIN	MAX	MIN	MAX	MIN	MAX
Tss	Time from strobe to stop assertion	50	—	50	—	50	—
Tli	Limited interlock time	0	150	0	150	0	150
Taz	Output release time	—	10	—	10	—	10
Tzah	Output enable time	20	—	20	—	20	—
Tmli	Interlock time	20	—	20	—	20	—
Tds	Data setup time (at device side)	15	—	10	—	7	—
Tdh	Data Hold time (at device side)	5	—	5	—	5	—
Tack	Hold time after -DMACK negation	20	—	20	—	20	—
Trdyz	Pull-up time before DSTROBE release	—	20	—	20	—	20

Figure 30. Ultra DMA cycle timings (Device terminating Read)

6.5.3.5 Initiating Write DMA

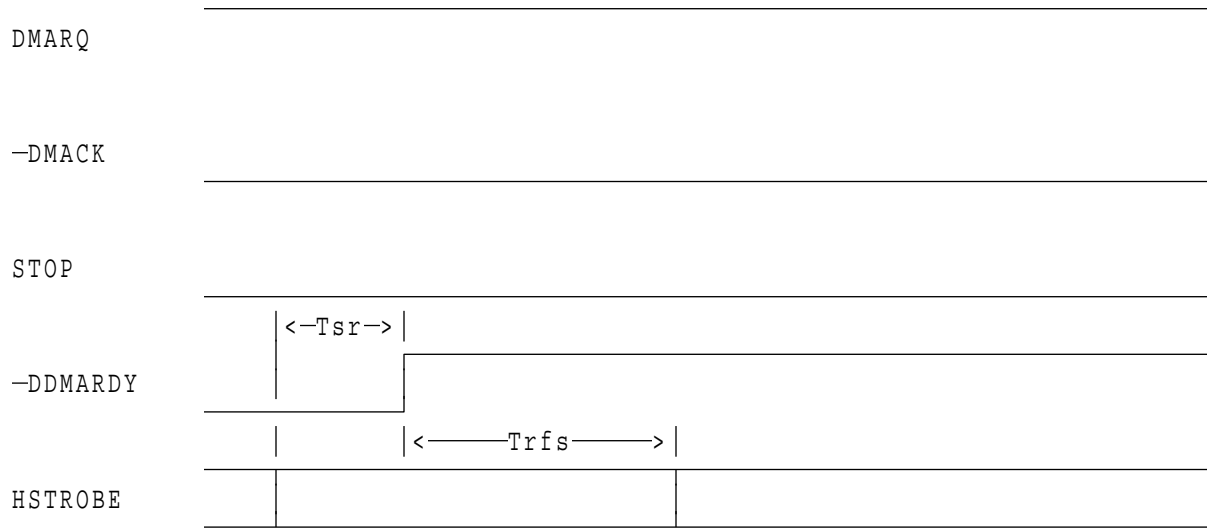


[nsec]

	PARAMETER DESCRIPTION	MODE0		MODE1		MODE2	
		MIN	MAX	MIN	MAX	MIN	MAX
Tui	Unlimited interlock time	0	—	0	—	0	—
Tack	Setup time before -DMACK assertion	20	—	20	—	20	—
Tenv	Envelope time	20	70	20	70	20	70
Tzrdy	Wait time before driving DDMARDY	0	—	0	—	0	—
Tli	Limited interlock time	0	150	0	150	0	150
Tcyc	Cycle Time	114	—	75	—	55	—
T2cyc	2 Cycle time	235	—	156	—	117	—
Tds	Data setup time (at device side)	15	—	10	—	7	—
Tdh	Data Hold time (at device side)	5	—	5	—	5	—

Figure 31. Ultra DMA cycle timings (Initiating Write)

6.5.3.6 Device Pausing Write DMA

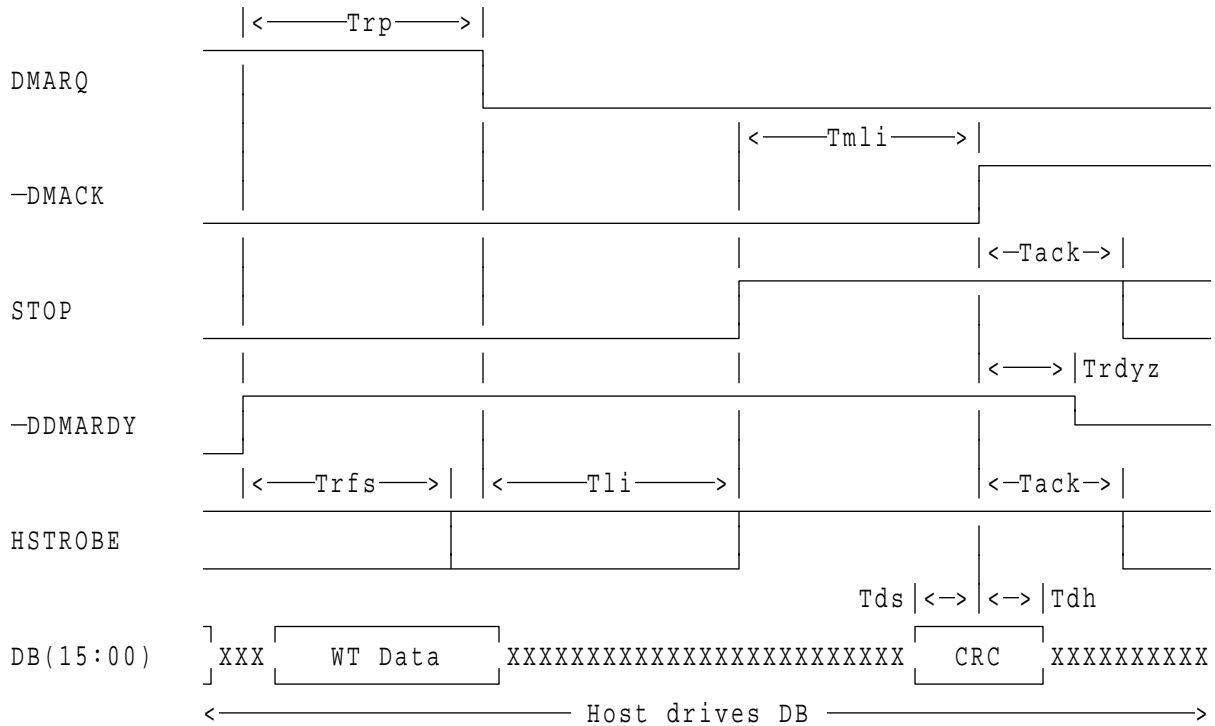


		[nsec]					
	PARAMETER DESCRIPTION	MODE0		MODE1		MODE2	
		MIN	MAX	MIN	MAX	MIN	MAX
Tsr	Strobe to ready response time	-	50	-	30	-	20
Trfs	Ready to final strobe time	-	75	-	60	-	50

Note : When a device does not meet Tsr, it shall be ready to receive 2 more strobcs after -DDMARDY is negated.

Figure 32. Ultra DMA cycle timings (Device pausing Write)

6.5.3.7 Device Terminating Write DMA

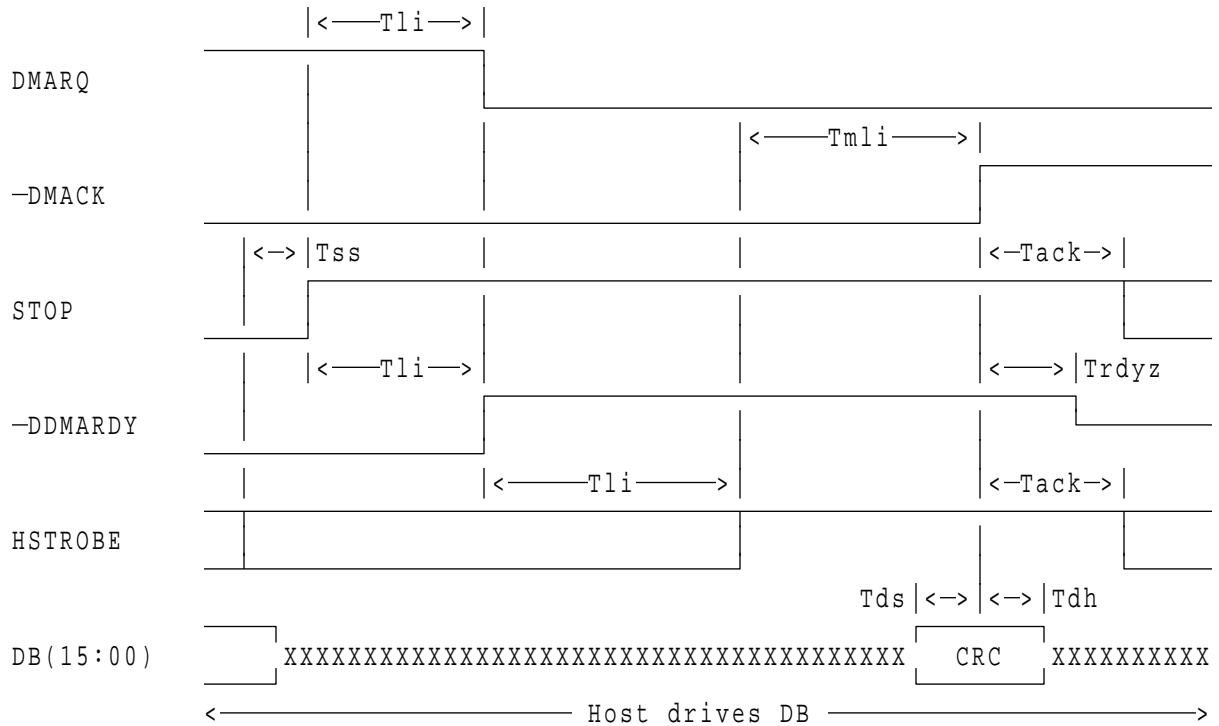


[nsec]

	PARAMETER DESCRIPTION	MODE0		MODE1		MODE2	
		MIN	MAX	MIN	MAX	MIN	MAX
Trfs	Ready to final strobe time	-	75	-	60	-	50
Trp	Ready to pause time	160	-	125	-	100	-
Tli	Limited interlock time	0	150	0	150	0	150
Tmli	Interlock time	20	-	20	-	20	-
Tds	Data setup time (at device side)	15	-	10	-	7	-
Tdh	Data Hold time (at device side)	5	-	5	-	5	-
Tack	Hold time after -DMACK negation	20	-	20	-	20	-
Trdys	Pull-up time before DDMARDY release	-	20	-	20	-	20

Figure 33. Ultra DMA cycle timings (Device terminating Write)

6.5.3.8 Host Terminating Write DMA



[nsec]

	PARAMETER DESCRIPTION	MODE0		MODE1		MODE2	
		MIN	MAX	MIN	MAX	MIN	MAX
Tss	Time from strobe to stop assertion	50	—	50	—	50	—
Tli	Limited interlock time	0	150	0	150	0	150
Tmli	Interlock time	20	—	20	—	20	—
Tds	Data setup time (at device side)	15	—	10	—	7	—
Tdh	Data Hold time (at device side)	5	—	5	—	5	—
Tack	Hold time after -DMACK negation	20	—	20	—	20	—
Trdyz	Pull-up time before DDMARDY release	—	20	—	20	—	20

Figure 34. Ultra DMA cycle timings (Host terminating Write)

6.6 Drive Address Setting

A jumper is available at the interface connector to determine the drive address. The set position of the jumper is as shown in Figure 35.

Using Cable Selection, the drive address depends on the condition of pin 28 of the AT interface cable. In the case when pin 28 is ground or low, the drive is a Master. If pin 28 is open or high level, the drive is a Slave.

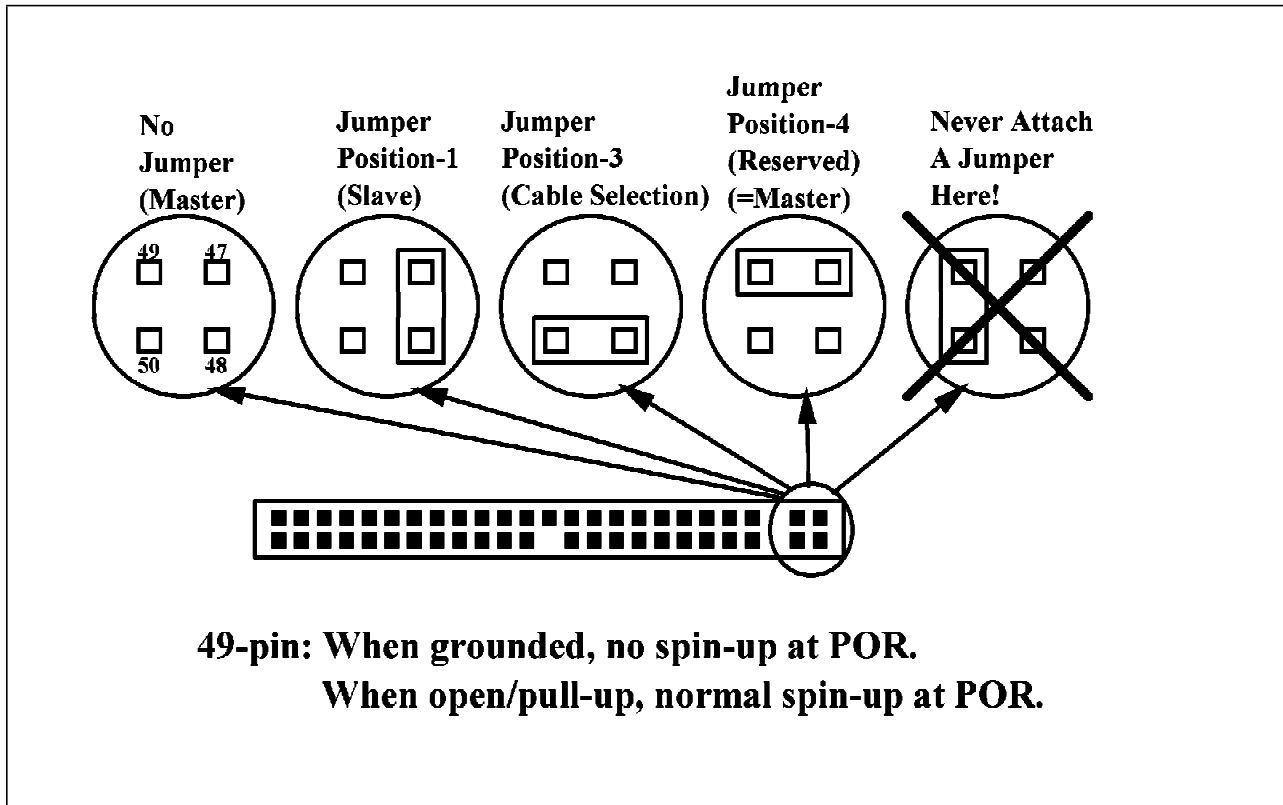


Figure 35. Address setting by a jumper for DPLA-24480/25120.

6.6.1 Default Setting

The default setting of jumper at shipment is No Jumper (Master).

6.7 Addressing of drive Registers

The host addresses the drive through a set of registers called a Task File. These registers are mapped into the host's I/O space. Two chip select lines (-HCS0 and -HCS1) and three address lines (HA00-02) are used to select one of these registers, while a -HIOR or -HIOW is provided at the specified time.

The -HCS0 is used to address Command Block registers, while the -HCS1 is used to address Control Block registers.

The following table shows the standard I/O address range for IBM PC-AT machines.

Addr.	-CS0	-CS1	HA2	HA1	HA0	-HIOR = 0 (Read)	-HIOW = 0 (Write)
Command Block Registers							
1F0	0	1	0	0	0	Data Reg.	Data Reg.
1F1	0	1	0	0	1	Error Reg.	Features Reg.
1F2	0	1	0	1	0	Sector count Reg.	Sector count Reg.
1F3	0	1	0	1	1	Sector number Reg.	Sector number Reg.
1F4	0	1	1	0	0	Cylinder low Reg.	Cylinder low Reg.
1F5	0	1	1	0	1	Cylinder high Reg.	Cylinder high Reg.
1F6	0	1	1	1	0	Drive/Head Reg.	Drive/Head Reg.
1F7	0	1	1	1	1	Status Reg.	Command Reg.
Control Block Registers							
3F6	1	0	1	1	0	Alt. Status Reg.	Device control Reg
3F7	1	0	1	1	1	Drive address Reg.	—

Figure 36. Register Address

Note: "Addr." field is shown just as an example.

Part 2. ATA Interface Specification

7.0 General

7.1 Introduction

This specification describes the host interface of DPLA-2xxxx.

The interface conforms to the Working Document of Information technology - AT Attachment-3 Interface (ATA-3) Revision 6 dated on October 26, 1995. with certain limitations described in 8.0, "Deviations From Standard" on page 59.

DPLA-2xxxx support following new functions included by ATA-3 standard.

- Security Mode Feature Set
- S.M.A.R.T.(Self-Monitoring, Analysis, and Reporting Technology) Function

DPLA-2xxxx support following functions as Vendor Specific Function.

- Format Unit Function
- Protected Area Function

7.2 Terminology

Device	Device indicates DPLA-2xxxx.
Host	Host indicates the system that the device is attached to.
First Command	The command which is executed first right after power on reset or hard reset when the initial power mode at power on is Standby mode.
INTRQ	Interrupt request (Device or Host)

8.0 Deviations From Standard

The device conforms to the referenced specifications, with deviations described below.

- Check Power Mode** CHECK POWER MODE command returns FFh to Sector Count Register when the device is in Idle mode. This command does not support 80h as the return value.
- Write Verify** WRITE VERIFY command does not include read verification after write operation. The function is exactly same as WRITE SECTORS command.
- Standby Timer** Even if IDLE command or STANDBY command is issued with Sector Cuont register value 00h, Standby Timer is not disabled, but it sets default value 109 minutes. In case Sector Count register value is other than 00h, Standby Timer is set to (Sector Count register value) x 5 seconds.
- SMART Return Status** SMART RETURN STATUS subcommand does not check advisory attributes. That is, the device will not report threshold exceeded condition unless prefailure attributes exceed their corresponding thresholds. For example, Power-On Hours Attribute never results in negative reliability status.

9.0 Registers

Addresses					Functions	
CS0-	CS1-	DA2	DA1	DA0	READ(DIOR-)	WRITE(DIOW-)
N	N	x	x	x	Data bus high imped*1	Not used
					Control block registers	
N	A	0	x	x	Data bus high imped	Not used
N	A	1	0	x	Data bus high imped	Not used
N	A	1	1	0	Alternate Status	Device Control
N	A	1	1	1	Device Address	Not used
					Command block registers	
A	N	0	0	0	Data	Data
A	N	0	0	1	Error Register	Features
A	N	0	1	0	Sector Count	Sector Count
A	N	0	1	1	Sector Number	Sector Number
A	N	0	1	1	*2 LBA bits 0-7	*2 LBA bits 0-7
A	N	1	0	0	Cylinder Low	Cylinder Low
A	N	1	0	0	*2 LBA bits 8-15	*2 LBA bits 8-15
A	N	1	0	1	Cylinder High	Cylinder High
A	N	1	0	1	*2 LBA bits 16-23	*2 LBA bits 16-23
A	N	1	1	0	Device/Head	Device/Head
A	N	1	1	0	*2 LBA bits 24-27	*2 LBA bits 24-27
A	N	1	1	1	Status	Command
A	A	x	x	x	Invalid address	Invalid address

*1 "imped" stands for "impedance".
 *2 Mapping of registers in LBA mode

Logic conventions : A = signal asserted
 N = signal negated
 x = does not matter which it is

Figure 37. Register Set

Communication to or from the device is through an I/O Register that routes the input or output data to or from registers addressed by the signals from the host (CS0-, CS1-, DA2, DA1, DA0, DIOR- and DIOW-).

The Command Block Registers are used for sending commands to the device or posting status from the device.

The Control Block Registers are used for device control and to post alternate status.

9.1 Alternate Status Register

Alternate Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR

Figure 38. Alternate Status Register

This register contains the same information as the Status Register. The only difference is that reading this register does not imply interrupt acknowledge or clear a pending interrupt. See 9.13, “Status Register” on page 65 for the definition of the bits in this register.

9.2 Command Register

This register contains the command code being sent to the device. Command execution begins immediately after this register is written. The command set is shown in Figure 54 on page 95.

All other registers required for the command must be set up before writing the Command Register.

9.3 Cylinder High Register

This register contains the high order bits of the starting cylinder address for any disk access. At the end of the command, this register is updated to reflect the current cylinder number.

In LBA Mode this register contains Bits 16-23. At the end of the command, this register is updated to reflect the current LBA Bits 16-23.

The cylinder number may be from zero to the number of cylinders minus one.

9.4 Cylinder Low Register

This register contains the low order 8 bits of the starting cylinder address for any disk access. At the end of the command, this register is updated to reflect the current cylinder number.

In LBA Mode this register contains Bits 8-15. At the end of the command, this register is updated to reflect the current LBA Bits 8-15.

The cylinder number may be from zero to the number of cylinders minus one.

9.5 Data Register

This register is used to transfer data blocks between the device data buffer and the host. It is also the register through which sector information is transferred on a Format Track command, and configuration information is transferred on an Identify Device command.

All data transfers are 16 bits wide, except for ECC byte transfers, which are 8 bits wide. Data transfers are PIO only.

The register contains valid data only when DRQ=1 in the Status Register.

9.6 Device Control Register

Device Control Register							
7	6	5	4	3	2	1	0
—	—	—	—	1	SRST	-IEN	0

Figure 39. Device Control Register

Bit Definitions

- SRST (RST)** Software Reset. The device is held reset when RST=1. Setting RST=0 re-enables the device.
- The host must set RST=1 and wait for at least 5 microseconds before setting RST=0, to ensure that the device recognizes the reset.
- IEN** Interrupt Enable. When IEN=0, and the device is selected, device interrupts to the host will be enabled. When IEN=1, or the device is not selected, device interrupts to the host will be disabled.

9.7 Drive Address Register

Drive Address Register							
7	6	5	4	3	2	1	0
HIZ	-WTG	-H3	-H2	-H1	-H0	-DS1	-DS0

Figure 40. Drive Address Register

This register contains the inverted drive select and head select addresses of the currently selected drive.

Bit Definitions

- HIZ** High Impedance. This bit is not device and will always be in a high impedance state.
- WTG** -Write Gate. This bit is 0 when writing to the disk device is in progress.
- H3,-H2,-H1,-H0** -Head Select. These four bits are the one's complement of the binary coded address of the currently selected head. -H0 is the least significant.

- DS1** -Drive Select 1. Drive select bit for device 1, active low. DS1=0 when device 1 (slave) is selected and active.
- DS0** -Drive Select 0. Drive select bit for device 0, active low. DS0=0 when device 0 (master) is selected and active.

9.8 Device/Head Register

Device/Head Register							
7	6	5	4	3	2	1	0
1	L	1	DRV	HS3	HS2	HS1	HS0

Figure 41. Device/Head Register

This register contains the device and head numbers.

Bit Definitions

- L** Binary encoded address mode select. When L=0, addressing is by CHS mode. When L=1, addressing is by LBA mode.
- DRV** Device. When DRV=0, device 0 (master) is selected. When DRV=1, device 1 (slave) is selected.
- HS3,HS2,HS1,HS0** Head Select. These four bits indicate binary encoded address of the head . HS0 is the least significant bit. At command completion, these bits are updated to reflect the currently selected head.

The head number may be from zero to the number of heads minus one.

In LBA mode, HS3 through HS0 contain bits 24-27 of the LBA. At command completion, these bits are updated to reflect the current LBA bits 24-27.

9.9 Error Register

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDNF	0	ABRT	TK0NF	AMNF

Figure 42. Error Register

This register contains status from the last command executed by the device, or a diagnostic code.

At the completion of any command except Execute Device Diagnostic, the contents of this register are valid always even if ERR=0 in the Status Register.

Following a power on, a reset, or completion of an Execute Device Diagnostic command, this register contains a diagnostic code. See Figure 46 on page 69 for the definition.

Bit Definitions

ICRCE (CRC)	Interface CRC Error. CRC=1 indicates a CRC error has occurred on the data bus during a Ultra-DMA transfer.
UNC	Uncorrectable Data Error. UNC=1 indicates an uncorrectable data error has been encountered.
IDNF (IDN)	ID Not Found. IDN=1 indicates the requested sector's ID field could not be found.
ABRT (ABT)	Aborted Command. ABT=1 indicates the requested command has been aborted due to a device status error or an invalid parameter in an output register.
TK0NF (T0N)	Track 0 Not Found. T0N=1 indicates track 0 was not found during a Recalibrate command.
AMNF (AMN)	Address Mark Not Found. AMN=1 indicates the data address mark has not been found after finding the correct ID field for the requested sector.

9.10 Features Register

This register is command specific. This is used with the Set Features command, S.M.A.R.T. Function Set command and Format Unit command.

9.11 Sector Count Register

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the device. If the value in the register is set to 0, a count of 256 sectors is specified.

If the register is zero at command completion, the command was successful. If not successfully completed, the register contains the number of sectors which need to be transferred in order to complete the request.

The contents of the register are defined otherwise on some commands. These definitions are given in the command descriptions.

9.12 Sector Number Register

This register contains the starting sector number for any disk data access for the subsequent command. The sector number is from one to the maximum number of sectors per track.

In LBA mode, this register contains Bits 0-7. At the end of the command, this register is updated to reflect the current LBA Bits 0-7.

9.13 Status Register

Status Register							
7	6	5	4	3	2	1	0
BSY	DRDY	DF	DSC	DRQ	CORR	IDX	ERR

Figure 43. Status Register

This register contains the device status. The contents of this register are updated whenever an error occurs and at the completion of each command.

If the host reads this register when an interrupt is pending, it is considered to be the interrupt acknowledge. Any pending interrupt is cleared whenever this register is read.

If BSY=1, no other bits in the register are valid.

Bit Definitions

BSY	Busy. BSY=1 whenever the device is accessing the registers. The host should not read or write any registers when BSY=1. If the host reads any register when BSY=1, the contents of the Status Register will be returned.
DRDY (RDY)	Device Ready. RDY=1 indicates that the device is capable of responding to a command. RDY will be set to 0 during power on until the device is ready to accept a command.
DF	Device Fault. DF=1 indicates that the device has detected a write fault condition. DF is set to 0 after the Status Register is read by the host.
DSC	Device Seek Complete. DSC=1 indicates that a seek has completed and the device head is settled over a track. DSC is set to 0 by the device just before a seek begins. When an error occurs, this bit is not changed until the Status Register is read by the host, at which time the bit again indicates the current seek complete status. When the device enters into or is in Standby mode or Sleep mode, this bit is set by device in spite of not spinning up.
DRQ	Data Request. DRQ=1 indicates that the device is ready to transfer a word or byte of data between the host and the device. The host should not write the Command register when DRQ=1.
CORR (COR)	Corrected Data. Always 0.
IDX	Index. IDX=1 once per revolution. Since IDX=1 only for a very short time during each revolution, the host may not see it set to 1 even if the host is reading the Status Register continuously. Therefore the host should not attempt to use IDX for timing purposes.
ERR	Error. ERR=1 indicates that an error occurred during execution of the previous command. The Error Register should be read to determine the error type. The device sets ERR=0 when the next command is received from the host.

10.0 General Operation Descriptions

10.1 Reset Response

There are three types of reset in ATA as follows:

Power On Reset (POR)

The device executes a series of electrical circuitry diagnostics, spins up the HDA, tests speed and other mechanical parametric, and sets default values.

Hard Reset (Hardware Reset)

RESET- signal is negated in ATA Bus.

The device executes a series of electrical circuitry diagnostics, spins up the HDA, tests speed and other mechanical parametric, and sets default values.

Soft Reset (Software Reset)

SRST bit in the Device Control Register is set, then is reset.

The device resets the interface circuitry according to the Set Features requirement.

The actions of each reset is shown in Figure 44

	POR	hard reset	soft reset
Aborting Host interface	—	0	0
Aborting Device operation	—	(*1)	(*1)
Initialization of hardware	0	0	x
Internal diagnostic	0	0	x
Spinning spindle	(*6)	(*6)	x
Initialization of registers (*2)	0	0	0
DASP handshake	0	0	x
PDIAG handshake	0	0	0
Reverting programmed parameters to default	0	0	(*3)
— Number of CHS (set by Initialize Device Parameter)			
— Multiple mode			
— Write cache			
— Read look-ahead			
— ECC bytes			
Disable Standby timer	0	0	x
Power mode	(*6)	(*6)	(*4)
Reset Standby timer value (*5)	0	0	x

0 — execute
x — not execute

Figure 44. Reset Response Table

Note.

(*1) Execute after the data in write cache has been written.

- (*2) Default value on POR is shown in Figure 45 on page 69.
- (*3) The Set Features command with Feature register = CCh enables the device to revert these parameters to the power on defaults.
- (*4) In the case of sleep mode, the device goes to idle mode. In other case, the device does not change current mode.
- (*5) After reset the Standby timer value, it is set to 109 minutes.
- (*6) According to the initial power mode selection.

10.1.1 Register Initialization

Register	Default Value
Error	Diagnostic Code
Sector Count	01h
Sector Number	01h
Cylinder Low	00h
Cylinder High	00h
Device/Head	E0h
Status	50h
Alternate Status	50h

Figure 45. Default Register Values

After power on, hard reset, or software reset, the register values are initialized as shown in Figure 45.

Code	Description
01h	No error detected
02h	Formatter device error
03h	Sector buffer error
04h	ECC circuitry error
05h	Controller microprocessor error
8xh	Device 1 failed

Figure 46. Diagnostic Codes

The meaning of the Error Register diagnostic codes resulting from power on, hard reset or the Execute Device Diagnostic command are shown in Figure 46.

10.2 Diagnostic and Reset considerations

For each Reset and Execute Device Diagnostic, the diagnostic is done as follows:

Power On Reset, Hard Reset

DASP- is read by Device 0 to determine if Device 1 is present. If Device 1 is present Device 0 shall read PDIAG- to determine when it is valid to clear the BSY bit and whether Device 1 has powered on or reset without error, otherwise Device 0 clears the BSY bit whenever it is ready to accept commands. Device 0 may assert DASP- to indicate device activity. If Device 1 is not present, Device 0 does not Assert DASP- at POR.

Soft Reset

If Device 1 is present Device 0 shall read PDIAG- to determine when it is valid to clear the BSY bit and whether Device 1 has reset without any errors, otherwise Device 0 shall simply reset and clear the BSY bit. DASP- is asserted by Device 0 (and Device 1 if it is present) in order to indicate device active.

Execute Device Diagnostic

If Device 1 is present, Device 0 shall read PDIAG- to determine when it is valid to clear the BSY bit and if Device 1 passed or failed the EXECUTE DEVICE DIAGNOSTIC command, otherwise Device 0 shall simply execute its diagnostics and then clear the BSY bit. DASP- is asserted by Device 0 (and Device 1 if it is present) in order to indicate the device is active.

In all the above cases: Power on, RESET-, Soft reset, and the EXECUTE DEVICE DIAGNOSTIC command the Device 0 Error register is shown in Figure 47.

Device 1 Present?	PDIAG- Asserted?	Device 0 Passed	Error Register
Yes	Yes	Yes	01h
Yes	Yes	No	0xh
Yes	No	Yes	81h
Yes	No	No	8xh
No	(not read)	Yes	01h
No	(not read)	No	0xh

Where x indicates the appropriate Diagnostic Code for the Power on, RESET-, Soft reset, or Device Diagnostic error.

Figure 47. Reset error register values

10.3 Sector Addressing Mode

All addressing of data sectors recorded on the device's media is by a logical sector address. The logical CHS address for DTCA-2xxxx/DPLA-2xxxx is different from the actual physical CHS location of the data sector on the disk media.

DTCA-2xxxx/DPLA-2xxxx support both Logical CHS Addressing Mode and LBA Addressing Mode as the sector addressing mode.

The host system may select either the currently selected CHS translation addressing or LBA addressing on a command-by-command basis by using the L bit in the DEVICE/HEAD register. So a host system must set the L bit to 1 if the host uses LBA Addressing mode.

10.3.1 Logical CHS Addressing Mode

The logical CHS addressing is made up of three fields: the cylinder number, the head number and the sector number. Sectors are numbered from 1 to the maximum value allowed by the current CHS translation mode but can not exceed 255(0FFh). Heads are numbered from 0 to the maximum value allowed by the current CHS translation mode but can not exceed 15(0Fh). Cylinders are numbered from 0 to the maximum value allowed by the current CHS translation mode but cannot exceed 65535(0FFFFh).

When the host selects a CHS translation mode using the INITIALIZE DEVICE PARAMETERS command, the host requests the number of sectors per logical track and the number of heads per logical cylinder. The device then computes the number of logical cylinders available in requested mode.

The default CHS translation mode is described in the Identify Device Information. The current CHS translation mode also is described in the Identify Device Information.

10.3.2 LBA Addressing Mode

Logical sectors on the device shall be linearly mapped with the first LBA addressed sector (sector 0) being the same sector as the first logical CHS addressed sector (cylinder 0, head 0, sector 1). Irrespective of the logical CHS translation mode currently in effect, the LBA address of a given logical sector does not change. The following is always true:

$$\text{LBA} = ((\text{cylinder} * \text{heads_per_cylinder} + \text{heads}) * \text{sectors_per_track}) + \text{sector} - 1$$

where heads_per_cylinder and sectors_per_track are the current translation mode values.

On LBA addressing mode, the LBA value is set to the following register.

Device/Head	<---	LBA bits 27-24
Cylinder High	<---	LBA bits 23-16
Cylinder Low	<---	LBA bits 15- 8
Sector Number	<---	LBA bits 7- 0

10.4 Power Management Feature

The power management feature set permits a host to modify the behavior in a manner which reduces the power required to operate. The power management feature set provides a set of commands and a timer that enables a device to implement low power consumption modes.

DTCA-2xxxx/DPLA-2xxxx implement the following set of functions.

1. A Standby timer
2. Idle command
3. Idle Immediate command
4. Sleep command
5. Standby command
6. Standby Immediate command

10.4.1 Power Mode

Sleep Mode	The lowest power consumption when the device is powered on occurs in Sleep Mode. When in sleep mode, the device requires a reset to be activated. The time to respond could be as long as the power on reset time.
Standby Mode	The device interface is capable of accepting commands, but as the media may not immediately accessible, there is a delay while waiting for the spindle to reach operating speed.
Idle Mode	Refer to the section of Adaptive Battery Life Extender Feature.
Active Mode	The device is in execution of a command or accessing the disk media with read look-ahead function or write cache function.

10.4.2 Power Management Commands

The Check Power Mode command allows a host to determine if a device is currently in, going to or leaving standby mode.

The Idle and Idle Immediate commands move a device to idle mode immediately from the active or standby modes. The idle command also sets the standby timer count and starts the standby timer.

The sleep command moves a device to sleep mode. The device's interface becomes inactive at the completion of the sleep command. A reset is required to move a device out of sleep mode. When a device exits sleep mode it will enter idle mode.

The Standby and Standby Immediate commands move a device to standby mode immediately from the active or idle modes. The standby command also sets the standby timer count.

10.4.3 Standby/Sleep command completion timing

1. Confirm the completion of writing cached data in the buffer to media
2. Unload heads on the ramp
3. Set DRDY bit and DSC bit in Status Register
4. Set INTRQ (completion of the command)

5. Activate the spindle break to stop the spindle motor
6. Wait until spindle motor is stopped
7. Perform post process

10.4.4 Standby timer

The standby timer provides a method for the device to automatically enter standby mode from either active or idle mode following a host programmed period of inactivity. If the device is in the active or idle mode, the device waits for the specified time period and if no command is received, the device automatically enters the standby mode.

If the value of SECTOR COUNT register on Idle command or Standby command is set to 00h, the device will automatically set the standby timer to 109 minutes.

10.4.5 Status

In the active, idle and standby modes, the device shall have RDY bit of the status register set. If BSY bit is not set, device shall be ready to accept any command.

In sleep mode, the device's interface is not active. A host shall not attempt to read the device's status or issue commands to the device.

10.4.6 Interface Capability for Power Modes

Each power mode affects the physical interface as defined in the following table:

Mode	BSY	RDY	Interface active	Media
Active	x	x	Yes	Active
Idle	o	1	Yes	Active
Standby	o	1	Yes	Inactive
Sleep	x	x	No	Inactive

Figure 48. Power conditions

Ready(RDY) is not a power condition. A device may post ready at the interface even though the media may not be accessible.

Though the interface is inactive in sleep mode, the access to the interface registers and the validity of INTRQ is guaranteed for two seconds after Sleep command is completed. After this period, the contents of interface registers may be lost. Since the contents of interface registers may be invalid, host should NOT check Status register nor Alternate Status register prior to issuing soft reset to wake up a device.

10.4.7 Initial Power Mode at Power On

After power on or hard reset the device goes to IDLE mode or STANDBY mode depending on the option. Refer DTCA-2xxxx Final Functional Specification (P/N TBD)/DPLA-2xxxx Final Functional Specification (P/N TBD) for the initial power mode selection.

10.5 Adaptive Battery Life Extender (ABLE-2) Feature

This feature provides power saving without performance degradation. The ABLE-2 technology intelligently manages transition among power modes within the device by monitoring access patterns of the host.

This feature has three idle modes; Performance Idle mode, Active Idle mode, and Low Power Idle mode.

This feature allows the host to select a power management level. The power management level is a scale from the lowest power consumption setting of 01h to the maximum performance level of FEh. Device performance may increase with increasing power management levels. Device power consumption may increase with increasing power management levels. The power management levels contain discrete bands, described in the section of Set Feature command in detail.

This feature set uses the following functions:

- A SET FEATURES subcommand to enable Advanced Power Management
- A SET FEATURES subcommand to disable Advanced Power Management

The ABLE-2 is independent of the Standby timer setting. If both ABLE-2 and the Standby timer are set, the device will go to the Standby state when the timer times out or the device's Advanced Power Management algorithm indicates that it is time to enter the Standby state.

The IDENTIFY DEVICE response word 83, bit 3 indicates that Advanced Power Management is supported if set. Word 86, bit 3 indicates that Advanced Power Management is enabled if set. Word 96, bits 7-0 contain the current Advanced Power Management level if Advanced Power Management is enabled.

10.5.1 Performance Idle mode

This mode is usually entered immediately after Active mode command processing is complete, instead of conventional idle mode. In Performance Idle mode, all electronic components remain powered and full frequency servo remains operational. This provides instantaneous response to the next command. The duration of this mode is intelligently managed as described below.

10.5.2 Active Idle mode

In this mode, power consumption is 35-50% less than that of Performance Idle mode. Additional electronics are powered off, and the head is parked near the mid-diameter of the disk without servoing. Recovery time to Active mode is about 40ms.

10.5.3 Low Power Idle mode

Power consumption is 55%-65% less than that of Performance Idle mode. The heads are unloaded on the ramp, however the spindle is still rotated at the full speed. Recovery time to Active mode is about 300ms.

10.5.4 Transition Time

The transition time is dynamically managed by users recent access pattern, instead of fixed times. The algorithm monitors the frequency of commands over intervals of interest, usually several seconds. The algorithm judges how long the current burst of commands will continue by maintaining a distribution of command frequencies. After each command, the algorithm calculates the probability that the current burst of commands is complete based on the statistics of the distribution.

Each time this algorithm decides that the current burst of commands is not yet complete, it places the device in Performance Idle mode. This means another command will arrive very soon, and the response to it can now be instantaneous without the delay associated with conventional idle. Since bursts usually contain tens of commands, performance is improved.

When this algorithm decides the current burst of commands is complete, it knows with high probability that the next command will not occur for a relatively long time (seconds). To conserve power, this feature places the device in Active Idle mode, then performs a seek to the mid-band and enters a low power state.

The optimal time to enter Active Idle is variable depending on the users recent behavior. It is not possible to achieve the same level of savings with a fixed entry time into Active Idle because every users data and access pattern is different. The optimum entry time changes over time.

To recover to Active mode from Active Idle requires about 40 ms. This does not represent a significant performance impact because it is a relatively rare event, and because a new burst of commands almost always begins with a seek to a new location which requires the time anyway. Throughput is maintained because Active Idle is entered only when a long idle interval is anticipated.

The same algorithm works for entering into Low Power Idle mode, which consumes less power and need more recovery time switching from this mode to Active mode.

10.6 S.M.A.R.T. Function

The intent of Self-monitoring, analysis and reporting technology (S.M.A.R.T) is to protect user data and prevent unscheduled system downtime that may be caused by predictable degradation and/or fault of the device. By monitoring and storing critical performance and calibration parameters, S.M.A.R.T devices employ sophisticated data analysis algorithms to predict the likelihood of near-term degradation or fault condition. By alerting the host system of a negative reliability status condition, the host system can warn the user of the impending risk of a data loss and advise the user of appropriate action.

Since S.M.A.R.T. utilizes the internal device microprocessor and other device resources, there may be some small overhead associated with its operation. However, special care has been taken in the design of the S.M.A.R.T. algorithms to minimize the impact to host system performance. Actual impact of S.M.A.R.T. overhead is dependent on the specific device design and the usage patterns of the host system. To further ensure minimal impact to the user, S.M.A.R.T. capable devices are shipped from the device manufacturer's factory with the S.M.A.R.T. feature disabled. S.M.A.R.T. capable devices can be enabled by the system OEMs at time of system integration or in the field by aftermarket products.

10.6.1 Attributes

Attributes are the specific performance or calibration parameters that are used in analyzing the status of the device. Attributes are selected by the device manufacturer based on that attribute's ability to contribute to the prediction of degrading or faulty conditions for that particular device. The specific set of attributes being used and the identity of these attributes is vendor specific and proprietary.

10.6.2 Attribute values

Attribute values are used to represent the relative reliability of individual performance or calibration attributes. Higher attribute values indicate that the analysis algorithms being used by the device are predicting a lower probability of a degrading or fault condition existing. Accordingly, lower attribute values indicate that the analysis algorithms being used by the device are predicting a higher probability of a degrading or fault condition existing. There is no implied linear reliability relationship corresponding to the numerical relationship between different attribute values for any particular attribute.

10.6.3 Attribute thresholds

Each attribute value has a corresponding attribute threshold limit which is used for direct comparison to the attribute value to indicate the existence of a degrading or faulty condition. The numerical value of the attribute thresholds are determined by the device manufacturer through design and reliability testing and analysis. Each attribute threshold represents the lowest limit to which its corresponding attribute value can be equal while still retaining a positive reliability status. Attribute thresholds are set at the device manufacturer's factory and cannot be changed in the field. The valid range for attribute thresholds is from 1 through 253 decimal.

10.6.4 Threshold exceeded condition

If one or more attribute values are less than or equal to their corresponding attribute thresholds, then the device reliability status is negative, indicating an impending degrading or faulty condition.

10.6.5 S.M.A.R.T. commands

The S.M.A.R.T. commands provide access to attribute values, attribute thresholds and other logging and reporting information.

10.6.6 S.M.A.R.T. operation with power management modes

It is recommended that, when a host system utilizes both the power management and S.M.A.R.T. features, the system enable the device's attribute autosave feature to allow the device's automatic attribute saving upon receipt of STANDBY IMMEDIATE or SLEEP commands. If the device has been set to utilize the standby timer, the device also saves attributes values prior to going from an Idle state to Standby state.

10.7 Security Mode Feature Set

Security Mode Feature Set is a powerful security feature. With a device lock password, a user can prevent unauthorized access to hard disk device even if the device is removed from the computer.

New commands are supported for this feature as below.

Security Set Password	('F1'h)
Security Unlock	('F2'h)
Security Erase Prepare	('F3'h)
Security Erase Unit	('F4'h)
Security Freeze Lock	('F5'h)
Security Disable Password	('F6'h)

10.7.1 Security mode

Following security modes are provided.

Device Locked mode	The device disables media access commands after power on. Media access commands are enabled by either a security unlock command or a security erase unit command.
Device Unlocked mode	The device enables all commands. If a password is not set this mode is entered after power on, otherwise it is entered by a security unlock or a security erase unit command.
Device Frozen mode	The device enables all commands except those which can update the device lock function, set/change password. The device enters this mode via a Security Freeze Lock command. It cannot quit this mode until power off.

10.7.2 Security level

Following security levels are provided.

High level security	When the device lock function is enabled and the User Password is forgotten the device can be unlocked via a Master Password.
Maximum level security	When the device lock function is enabled and the User Password is forgotten then only the Master Password with a Security Erase Unit command can unlock the device. Then user data is erased.

10.7.3 Password

This function can have 2 types of passwords as described below.

Master Password	When the Master Password is set, the device does NOT enable the Device Lock Function, and the device can NOT be locked with the Master Password, but the Master Password can be used for unlocking the device locked.
User Password	The User Password should be given or changed by a system user. When the User Password is set, the device enables the Device Lock Function, and then the device is locked on next power on reset or hard reset.

The system manufacturer/dealer who intends to enable the device lock function for the end users, must set the master password even if only single level password protection is required. Otherwise, the 'default' master password which is set by IBM can unlock the device which is locked with user password.

10.7.4 Operation example

10.7.4.1 Master Password setting

The system manufacturer/dealer can set a new Master Password from default Master Password using the Security Set Password command, without enabling the Device Lock Function.

10.7.4.2 User Password setting

When a User Password is set, the device will automatically enter lock mode the next time the device is powered on.

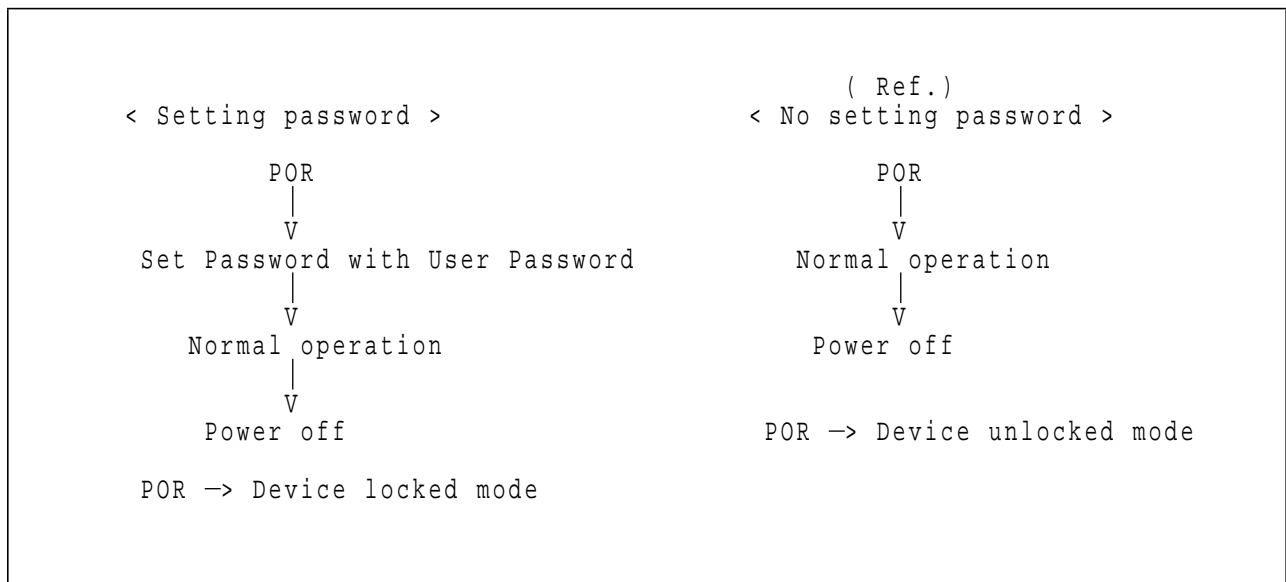


Figure 49. Initial Setting

10.7.4.3 Operation from POR after User Password is set

When Device Lock Function is enabled, the device rejects media access command until a Security Unlock command is successfully completed.

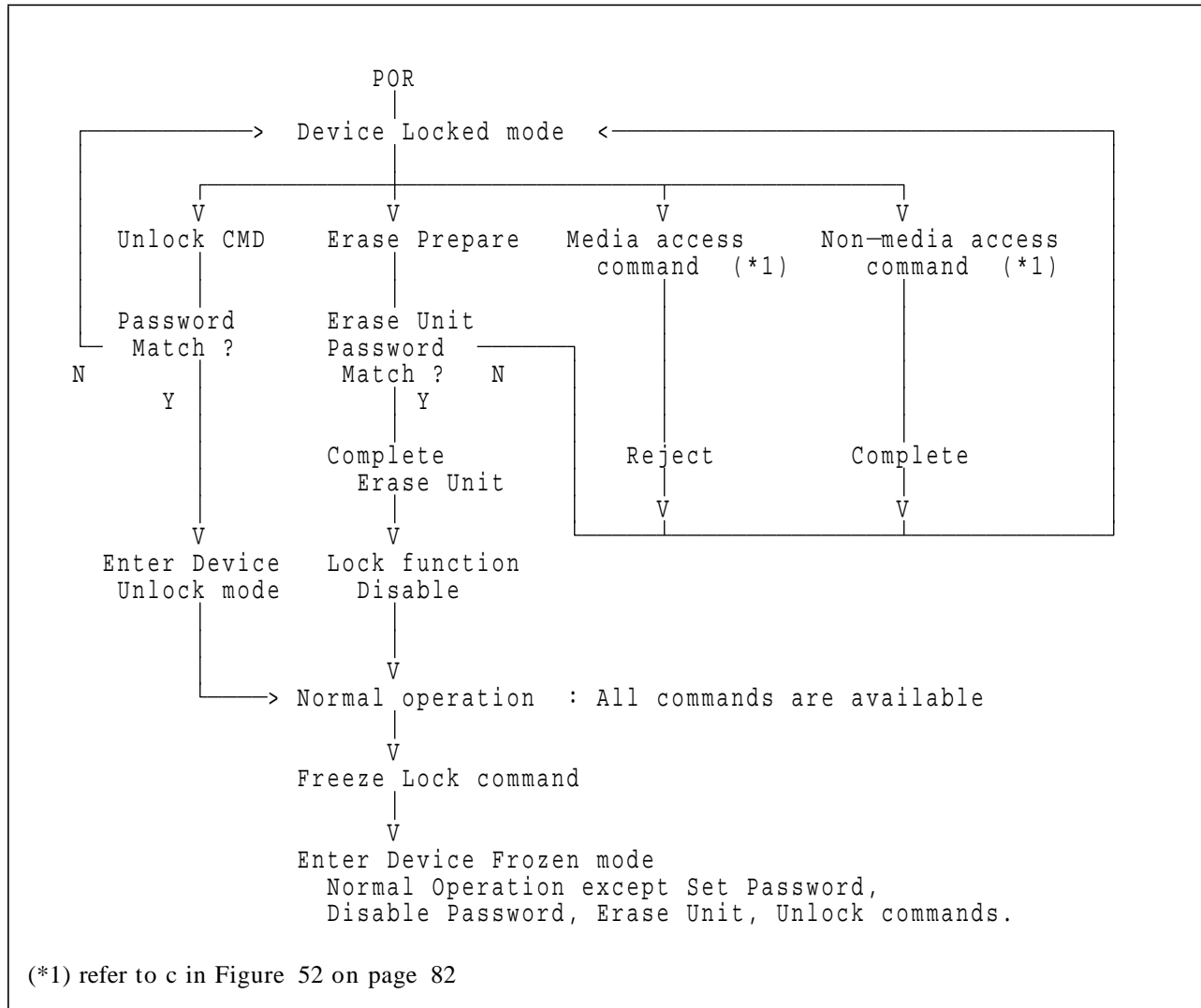


Figure 50. Usual Operation

10.7.4.4 User Password Lost

If the User Password is forgotten and High level security is set, the system user can't access any data. However the device can be unlocked using the Master Password.

If a system user forgets the User Password and Maximum security level is set, data access is impossible. However the device can be unlocked using the Security Erase Unit command to unlock the device and erase all user data with the Master Password.

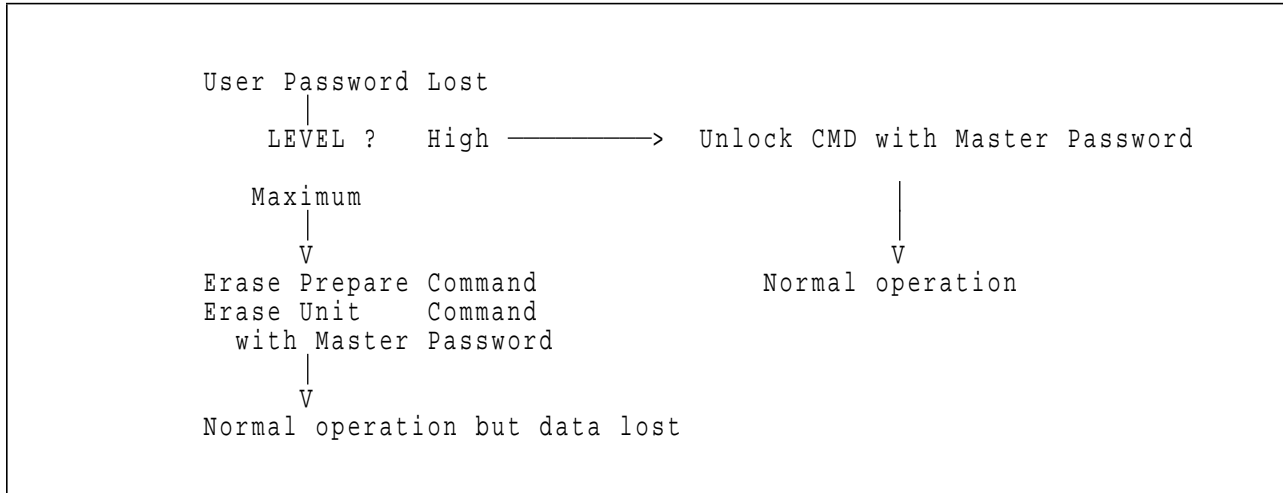


Figure 51. Password Lost

10.7.4.5 Attempt limit for SECURITY UNLOCK command

The SECURITY UNLOCK command has an attempt limit. The purpose of this attempt limit is to prevent that someone attempts to unlock the drive by using various passwords many times.

The device counts the password mismatch. If the password does not match, the device counts it up without distinguishing the Master password and the User password. If the count reaches 5, EXPIRE bit(bit 4) of Word 128 in Identify Device information is set, and then SECURITY ERASE UNIT command and SECURITY UNLOCK command are aborted until a hard reset or a power off. The count and EXPIRE bit are cleared after a power on reset or a hard reset.

10.7.5 Command Table

This table shows the device's response to commands when the Security Mode Feature Set (Device lock function) is enabled.

Command	Device Locked Mode	Device Unlock Mode	Device Frozen Mode
Check Power Mode	0	0	0
Execute Device Diagnostic	0	0	0
Flush Cache	0	0	0
Format Track	X	0	0
Format Unit	X	0	0
Identify Device	0	0	0
Identify Device DMA	0	0	0
Idle	0	0	0
Idle Immediate	0	0	0
Initialize Device Parameters	0	0	0
Read Buffer	0	0	0
Read DMA (w/o retry)	X	0	0
Read DMA (w/retry)	X	0	0
Read Long (w/o retry)	X	0	0
Read Long (w/retry)	X	0	0
Read Multiple	X	0	0
Read Native Max LBA/CYL	0	0	0
Read Sector(s) (w/o retry)	X	0	0
Read Sector(s) (w/retry)	X	0	0
Read Verify Sector(s) (w/o retry)	X	0	0
Read Verify Sector(s) (w/retry)	X	0	0
Recalibrate	0	0	0
Security Disable Password	X	0	X
Security Erase Prepare	0	0	0
Security Erase Unit	0	0	X
Security Freeze Lock	X	0	0
Security Set Password	X	0	X
Security Unlock	0	0	X
Seek	0	0	0
Set Features	0	0	0
Set Max LBA/CYL	0	0	0
Set Multiple Mode	0	0	0
Sleep	0	0	0

Figure 52. Command table for device lock operation

Command	Device Locked Mode	Device Unlock Mode	Device Frozen Mode
SMART Disable Operations	o	o	o
SMART Enable/Disable Attribute Autosave	o	o	o
SMART Enable Operations	o	o	o
SMART Execute Off-line Immediate	o	o	o
SMART Read Attribute Values	o	o	o
SMART Read Attribute Thresholds	o	o	o
SMART Return Status	o	o	o
SMART Save Attribute Values	o	o	o
Standby	o	o	o
Standby Immediate	o	o	o
Write Buffer	o	o	o
Write DMA (w/o retry)	x	o	o
Write DMA (w/retry)	x	o	o
Write Long (w/o retry)	x	o	o
Write Long (w/retry)	x	o	o
Write Multiple	x	o	o
Write Sector(s) (w/o retry)	x	o	o
Write Sector(s) (w/retry)	x	o	o
Write Verify	x	o	o

- o — Device executes command normally
- x — Device terminates command with error register of Aborted Command.

Figure 53. Command table for device lock operation - continued

10.8 Protected Area Function (Vendor Specific)

Protected Area Function is to provide the 'protected area' which can not be accessed via conventional method. This 'protected area' is used to contain critical system data such as BIOS or system management information. The contents of entire system main memory may also be dumped into 'protected area' to resume after system power off.

The LBA/CYL changed by following command affects the Identify Device Information.

Two vendor specific commands are defined for this function.

Read Native Max LBA/CYL ('F8'h)

Set Max LBA/CYL ('F9'h)

10.8.1 Example for operation (In LBA mode)

Assumptions :

For better understanding, the following example uses actual values for LBA, size, etc. Since it is just an example, these values could be different.

Device characteristics

Capacity (native)	: 536,870,912 byte (536MB)
Max LBA (native)	: 1,048,575 (0FFFFFFh)
Required size for protected area	: 8,388,608 byte
Required blocks for protected area	: 16,384 (004000h)
Customer usable device size	: 528,482,304 byte (528MB)
Customer usable sector count	: 1,032,192 (0FC000h)
LBA range for protected area	: 0FC000h to 0FFFFFFh

1. Shipping HDDs from HDD manufacturer

When the HDDs are shipped from HDD manufacturer, the device has been tested to have a capacity of 536MB, flagging the media defects not to be visible by system.

2. Preparing HDDs at system manufacturer

Special utility software is required to define the size of protected area and store the data into it. The sequence is :

Issue Read Native Max LBA/CYL command to get the real device max of LBA/CYL. Returned value shows that native device Max LBA is 0FFFFFFh regardless to the current setting.

Make entire device be accessible including the protected area by setting device Max LBA as 0FFFFFFh via Set Max LBA/CYL command. The option could be either nonvolatile or volatile.

Test the sectors for protected area (LBA > = 0FC000h) if required.

Write information data such as BIOS code within the protected area.

Change maximum LBA using Set Max LBA/CYL command to 0FBFFFh with nonvolatile option.

From this point, the protected area cannot be accessed until next Set Max LBA/CYL command is issued. Any BIOSes, device drivers, or application software access the HDD as if that is the 528MB device because the device acts exactly same as real 528MB device does.

3. Conventional usage without system software support

Since the HDD works as 528MB device, there is no special care to use this device for normal use.

4. Advanced usage using protected area

The data in the protected area is accessed by following.

Issue Read Native Max LBA/CYL command to get the real device max LBA/CYL. Returned value shows that native device Max LBA is 0FFFFFFh regardless of the current setting.

Make entire device be accessible including the protected area by setting device Max LBA as 0FFFFFFh via Set Max LBA/CYL command with volatile option. By using this option, unexpected power removal or reset will not make the protected area remained accessible.

Read information data from protected area.

Issue hard reset or POR to inhibit any access to the protected area.

10.9 Write Cache Function

Write cache is a performance enhancement whereby the device reports completion of the write command (Write Sectors and Write Multiple) to the host as soon as the device has received all of the data into its buffer. The device assumes responsibility to write the data subsequently onto the disk.

- While writing data after completed acknowledgment of a write command, soft reset or hard reset does not affect its operation. But power off terminates writing operation immediately and unwritten data are to be lost.
- Flush cache, Check power mode, Standby, Standby immediate, Sleep commands and Soft reset are executed after completion of flushing cache if write cache is enabled, so completion of flushing cache can be checked by confirming successful completion of these commands or Soft reset. For **Power Off Sequence**, refer to 5.3.6, “ Load/Unload” on page 24.
- The retry bit of Write Sectors is ignored when write cache is enabled.

10.10 Reassign Function

The reassign Function is used with read commands and write commands. The sectors of data for reassignment are prepared as the spare data sector. The assured number of the spare sectors is a minimum of 1230 sectors.

This reassignment information is registered internally, and the information is available right after completing the reassign function. Also the information is used on the next power on reset or hard reset.

If the number of the spare sector reaches 0 sector, the reassign function will be disabled automatically.

The spare sectors for reassignment are located at reserved area. As a result of reassignment, the physical location of logically sequenced sectors will be dispersed.

10.10.1 Auto Reassign Function

The sectors that show some errors may be reallocated automatically when specific conditions are met. The spare sectors for reallocation are located at reserved area. The conditions for auto-reallocation are described below.

When a device shipped from IBM, a minimum of 1230 usable spare sectors are available.

Non recovered write errors

When a write operation can not be completed after the Error Recovery Procedure(ERP) is fully carried out, the sector(s) are reallocated to the spare location. An error is reported to the host system only when the write cache is disabled and the auto reallocation fails.

If the number of available spare sectors reaches 16 sectors, the write cache function will be disabled automatically.

If the command is without retry and the write cache function is disabled, the auto reassign function is not invoked.

Non recovered read errors

When a read operation fails after defined ERP is fully carried out, a hard error is reported to the host system. This location is registered internally as a candidate for the reallocation. When a registered location is specified as a target of a write operation, a sequence of media verification is performed automatically. When the result of this verification meets the criteria, this sector is reallocated.

Recovered read errors

When a read operation for a sector failed once then recovered at the specific ERP step, this sector of data is reallocated automatically. A media verification sequence may be run prior to the relocation according to the pre-defined conditions.

11.0 Command Protocol

The commands are grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined below.

For all commands, the host must first check if BSY=1, and should proceed no further unless and until BSY=0. For all commands, the host must also wait for RDY=1 before proceeding.

A device must maintain either BSY=1 or DRQ=1 at all times until the command is completed. The INTRQ signal is used by the device to signal most, but not all, times when the BSY bit is changed from 1 to 0 during command execution.

A command shall only be interrupted with a hardware or software reset. The result of writing to the Command register while BSY=1 or DRQ=1 is unpredictable and may result in data corruption. A command should only be interrupted by a reset at times when the host thinks there may be a problem, such as a device that is no longer responding.

Interrupts are cleared when the host reads the Status Register, issues a reset, or writes to the Command Register.

Figure 108 on page 171 shows the device timeout values.

11.1 Data In Commands

These commands are:

- Identify Device
- Read Buffer
- Read Long
- Read Multiple
- Read Sectors
- SMART Read Attribute Values
- SMART Read Attribute Thresholds

Execution includes the transfer of one or more 512 byte (>512 bytes on Read Long) sectors of data from the device to the host.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head Registers.
2. The host writes the command code to the Command Register.
3. For each sector (or block) of data to be transferred:
 - a. The device sets BSY=1 and prepares for data transfer.
 - b. When a sector (or block) of data is available for transfer to the host, the device sets BSY=0, sets DRQ=1, and interrupts the host.
 - c. In response to the interrupt, the host reads the Status Register.
 - d. The device clears the interrupt in response to the Status Register being read.
 - e. The host reads one sector (or block) of data via the Data Register.

- f. The device sets DRQ=0 after the sector (or block) has been transferred to the host.
4. For the Read Long command:
 - a. The device sets BSY=1 and prepares for data transfer.
 - b. When the sector of data is available for transfer to the host, the device sets BSY=0, sets DRQ=1, and interrupts the host.
 - c. In response to the interrupt, the host reads the Status Register.
 - d. The device clears the interrupt in response to the Status Register being read.
 - e. The host reads the sector of data including ECC bytes via the Data Register.
 - f. The device sets DRQ=0 after the sector has been transferred to the host.

The Read Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.

Note that the status data for a sector of data is available in the Status Register **before** the sector is transferred to the host.

If the device detects an invalid parameter, then it will abort the command by setting BSY=0, ERR=1, ABT=1, and interrupting the host.

If an error occurs, the device will set BSY=0, ERR=1, and DRQ=1. The device will then store the error status in the Error Register, and interrupt the host. The registers will contain the location of the sector in error. The errored location will be reported with CHS mode or LBA mode, the mode is decided by mode select bit (bit 6) of Device/Head register on issuing the command.

If an Uncorrectable Data Error (UNC=1) occurs, the defective data will be transferred from the media to the sector buffer, and will be available to be transferred to the host, at the host's option. In case of Read Multiple command, the host should complete transfer the block which includes the error from the sector buffer and terminate whatever kind of type of error occurred.

If an error occurs that is correctable by retries, the data will be corrected and the transfer will continue normally. There will be no indication to the host that any retry occurred.

All data transfers to the host through the Data Register are 16 bits, except for the ECC bytes, which are 8 bits.

11.2 Data Out Commands

These commands are:

- Format Track
- Security Disable Password
- Security Erase Unit
- Security Set Password
- Security Unlock
- Write Buffer
- Write Long
- Write Multiple

- Write Sectors
- Write Verify

Execution includes the transfer of one or more 512 byte (>512 bytes on Write Long) sectors of data from the host to the device.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head Registers.
2. The host writes the command code to the Command Register.
3. The device sets BSY=1.
4. For each sector (or block) of data to be transferred:
 - a. The device sets BSY=0 and DRQ=1 when it is ready to receive a sector (or block).
 - b. The host writes one sector (or block) of data via the Data Register.
 - c. The device sets BSY=1 after it has received the sector (or block).
 - d. When the device has finished processing the sector (or block), it sets BSY=0, and interrupts the host.
 - e. In response to the interrupt, the host reads the Status Register.
 - f. The device clears the interrupt in response to the Status Register being read.
5. For the Write Long command:
 - a. The device sets BSY=0 and DRQ=1 when it is ready to receive a sector.
 - b. The host writes one sector of data including ECC bytes via the Data Register.
 - c. The device sets BSY=1 after it has received the sector.
 - d. After processing the sector of data the device sets BSY=0 and interrupts the host.
 - e. In response to the interrupt, the host reads the Status Register.
 - f. The device clears the interrupt in response to the Status Register being read.

The Write Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.

If the device detects an invalid parameter, then it will abort the command by setting BSY=0, ERR=1, ABT=1, and interrupting the host.

If an uncorrectable error occurs, the device will set BSY=0 and ERR=1, store the error status in the Error Register, and interrupt the host. The registers will contain the location of the sector in error. The errored location will be reported with CHS mode or LBA mode. The mode is decided by mode select bit (bit 6) of Device/Head register on issuing the command.

All data transfers to the device through the Data Register are 16 bits, except for the ECC bytes, which are 8 bits.

11.3 Non-Data Commands

These commands are:

- Check Power Mode
- Execute Device Diagnostic
- Flush Cache
- Format Unit
- Idle
- Idle Immediate
- Initialize Device Parameters
- Read Native Max LBA/CYL
- Read Verify Sectors
- Recalibrate
- Security Erase Prepare
- Security Freeze Lock
- Seek
- Set Features
- Set Max LBA/CYL
- Set Multiple Mode
- Sleep
- SMART Disable Operations
- SMART Enable/Disable Attribute Autosave
- SMART Enable Operations
- SMART Execute Off-line Immediate
- SMART Return Status
- SMART Save Attribute Values
- Standby
- Standby Immediate

Execution of these commands involves no data transfer.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head Registers.
2. The host writes the command code to the Command Register.
3. The device sets BSY=1.
4. When the device has finished processing the command, it sets BSY=0, and interrupts the host.
5. In response to the interrupt, the host reads the Status Register.
6. The device clears the interrupt in response to the Status Register being read.

11.4 DMA Data Transfer Commands

These commands are:

- Identify Device DMA
- Read DMA
- Write DMA

Data transfer using DMA commands differ in two ways from PIO transfers:

- data transfers are performed using the slave-DMA channel
- no intermediate sector interrupts are issued on multi-sector commands

Initiation of the DMA transfer commands is identical to the Read Sector or Write Sector commands except that the host initializes the slave-DMA channel prior to issuing the command.

The interrupt handler for DMA transfers is different in that:

- no intermediate sector interrupts are issued on multi-sector commands
- the host resets the DMA channel prior to reading status from the device.

The DMA protocol allows high performance multi-tasking operating systems to eliminate processor overhead associated with PIO transfers.

1. Host initializes the slave-DMA channel
2. Host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder and Device/Head registers.
3. Host writes command code to the Command Register
4. The device sets DMARQ when it is ready to transfer any part of the data.
5. Host transfers the data using the DMA transfer protocol currently in effect.
6. When all of the data has been transferred, the device generates an interrupt to the host.
7. Host resets the slave-DMA channel
8. Host reads the Status Register and, optionally, the Error Register

12.0 Command Descriptions

Proto col	Command	Code (Hex)	Binary Code Bit							
			7	6	5	4	3	2	1	0
3	Check Power Mode	E5	1	1	1	0	0	1	0	1
3	Check Power Mode*	98	1	0	0	1	1	0	0	0
3	Execute Device Diagnostic	90	1	0	0	1	0	0	0	0
3	Flush Cache	E7	1	1	1	0	0	1	1	1
2	Format Track	50	0	1	0	1	0	0	0	0
3+	Format Unit	F7	1	1	1	1	0	1	1	1
1	Identify Device	EC	1	1	1	0	1	1	0	0
4	Identify Device DMA	EE	1	1	1	0	1	1	1	0
3	Idle	E3	1	1	1	0	0	0	1	1
3	Idle*	97	1	0	0	1	0	1	1	1
3	Idle Immediate	E1	1	1	1	0	0	0	0	1
3	Idle Immediate*	95	1	0	0	1	0	1	0	1
3	Initialize Device Parameters	91	1	0	0	1	0	0	0	1
1	Read Buffer	E4	1	1	1	0	0	1	0	0
4	Read DMA (retry)	C8	1	1	0	0	1	0	0	0
4	Read DMA (no retry)	C9	1	1	0	0	1	0	0	1
1	Read Long (retry)	22	0	0	1	0	0	0	1	0
1	Read Long (no retry)	23	0	0	1	0	0	0	1	1
1	Read Multiple	C4	1	1	0	0	0	1	0	0
3+	Read Native Max LBA/CYL	F8	1	1	1	1	1	0	0	0
1	Read Sectors (retry)	20	0	0	1	0	0	0	0	0
1	Read Sectors (no retry)	21	0	0	1	0	0	0	0	1
3	Read Verify Sectors (retry)	40	0	1	0	0	0	0	0	0
3	Read Verify Sectors (no retry)	41	0	1	0	0	0	0	0	1
3	Recalibrate	1x	0	0	0	1	—	—	—	—
2	Security Disable Password	F6	1	1	1	1	1	0	1	0
3	Security Erase Prepare	F3	1	1	1	1	0	0	1	1
2	Security Erase Unit	F4	1	1	1	1	0	1	0	0
3	Security Freeze Lock	F5	1	1	1	1	0	1	0	1
2	Security Set Password	F1	1	1	1	1	0	0	0	1
2	Security Unlock	F2	1	1	1	1	0	0	1	0
3	Seek	7x	0	1	1	1	—	—	—	—
3	Set Features	EF	1	1	1	0	1	1	1	1
3+	Set Max LBA/CYL	F9	1	1	1	1	1	0	0	1
3	Set Multiple Mode	C6	1	1	0	0	0	1	1	0

Figure 54. Command Set

Protocol	Command	Code (Hex)	Binary Code Bit							
			7	6	5	4	3	2	1	0
3	Sleep	E6	1	1	1	0	0	1	1	0
3	Sleep*	99	1	0	0	1	1	0	0	1
3	SMART Disable Operations	B0	1	0	1	1	0	0	0	0
3	SMART Enable/Disable Attribute Autosave	B0	1	0	1	1	0	0	0	0
3	SMART Enable Operations	B0	1	0	1	1	0	0	0	0
3	SMART Execute Off-line Immediate	B0	1	0	1	1	0	0	0	0
1	SMART Read Attribute Values	B0	1	0	1	1	0	0	0	0
1	SMART Read Attribute Thresholds	B0	1	0	1	1	0	0	0	0
3	SMART Return Status	B0	1	0	1	1	0	0	0	0
3	SMART Save Attribute Values	B0	1	0	1	1	0	0	0	0
3	Standby	E2	1	1	1	0	0	0	1	0
3	Standby*	96	1	0	0	1	0	1	1	0
3	Standby Immediate	E0	1	1	1	0	0	0	0	0
3	Standby Immediate*	94	1	0	0	1	0	1	0	0
2	Write Buffer	E8	1	1	1	0	1	0	0	0
4	Write DMA (retry)	CA	1	1	0	0	1	0	1	0
4	Write DMA (no retry)	CB	1	1	0	0	1	0	1	1
2	Write Long (retry)	32	0	0	1	1	0	0	1	0
2	Write Long (no retry)	33	0	0	1	1	0	0	1	1
2	Write Multiple	C5	1	1	0	0	0	1	0	1
2	Write Sectors (retry)	30	0	0	1	1	0	0	0	0
2	Write Sectors (no retry)	31	0	0	1	1	0	0	0	1
2	Write Verify	3C	0	0	1	1	1	1	0	0

Protocol : 1 : PIO data IN command
2 : PIO data OUT command
3 : Non data command
4 : DMA command
+ : Vendor specific command

Figure 55. Command Set - continued

Commands marked * are alternate command codes for previously defined commands.

Command (Subcommand)	Command Code (Hex)	Feature Register (Hex)
(S.M.A.R.T function)		
SMART Read Attribute Values	B0	D0
SMART Read Attribute Thresholds	B0	D1
SMART Enable/Disable Attribute Autosave	B0	D2
SMART Save Attribute Values	B0	D3
SMART Execute Off-line Immediate	B0	D4
SMART Enable Operations	B0	D8
SMART Disable Operations	B0	D9
SMART Return Status	B0	DA
(Set Features)		
Enable Write Cache	EF	02
Set Transfer Mode	EF	03
22 bytes of ECC apply on Read/Write Long	EF	44
Disable read look-ahead feature	EF	55
Disable reverting to power on defaults	EF	66
Disable write cache	EF	82
Enable read look-ahead feature	EF	AA
4 bytes of ECC apply on Read/Wrtie Long	EF	BB
Enable reverting to power on defaults	EF	CC
Enable Advanced Power Management feature	EF	05
Disable Advanced Power Management feature	EF	85

Figure 56. Command Set (Subcommand)

Figure 54 on page 95 and Figure 55 on page 96 shows the commands that are supported by the device. Figure 56 shows the sub-commands that are supported by each command or feature.

The following symbols are used in the command descriptions:

Output Registers

- 0** Indicates that the bit must be set to 0.
- 1** Indicates that the bit must be set to 1.
- D** The device number bit. Indicates that the device number bit of the Device/Head Register should be specified. Zero selects the master device and one selects the slave device.
- H** Head number. Indicates that the head number part of the Device/Head Register is an output parameter and should be specified.
- L** LBA mode. Indicates the addressing mode. Zero specifies CHS mode and one does LBA addressing mode.
- R** Retry. Indicates that the Retry bit of the Command Register should be specified.
- B** Option Bit. Indicates that the Option Bit of the Sector Count Register should be specified. (This bit is used by Set Max LBA/CYL command)
- V** Valid. Indicates that the bit is part of an output parameter and should be specified.
- x** Indicates that the hex character is not used.
- Indicates that the bit is not used.

Input Registers

- 0** Indicates that the bit is always set to 0.
- 1** Indicates that the bit is always set to 1.
- H** Head number. Indicates that the head number part of the Device/Head Register is an input parameter and will be set by the device.
- V** Valid. Indicates that the bit is part of an input parameter and will be set to 0 or 1 by the device.
- Indicates that the bit is not part of an input parameter.

The command descriptions show the contents of the Status and Error Registers after the device has completed processing the command and has interrupted the host.

12.1 Check Power Mode (E5h/98h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	1	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	-	-	0	-	V

Figure 57. Check Power Mode Command (E5h/98h)

The Check Power Mode command will report whether the device is spun up and the media is available for immediate access.

Input Parameters From The Device

Sector Count The power mode code. The command returns FFh in the Sector Count Register if the spindle motor is at speed and the device is not in Standby or Sleep mode. Otherwise, the Sector Count Register will be set to 0.

12.2 Execute Device Diagnostic (90h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	-	-	-	-	-
Command	1	0	0	1	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	V	V	V	V	V	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	-	-	0	-	0

Figure 58. Execute Device Diagnostic Command (90h)

The Execute Device Diagnostic command performs the internal diagnostic tests implemented by the device. The results of the test are stored in the Error Register.

The normal Error Register bit definitions do not apply to this command. Instead, the register contains a diagnostic code. See Figure 46 on page 69 for the definition.

12.3 Flush Cache (E7h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	1	1	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 59. Flush Cache Command (E7h)

This command causes the device to complete writing data from its cache.

The device returns a status, RDY=1 and DSC=1 (50h), after following sequence.

- Data in the write cache buffer is written to disk media.
- Return a successfully completion.

| **Note:** Flush cache command does not invoke head unload.

12.4 Format Track (50h: Vendor Specific)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	1	0	1	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 60. Format Track Command (50h)

The Format Track command formats a single logical track on the device. Each good sector of data on the track will be initialized to zero with write operation. At this time, whether the sector of data is initialized correctly is not verified with read operation. Any data previously stored on the track will be lost.

The host transfers a sector of data containing a format table to the device. The format table should contain two bytes for each sector on the track to be formatted. The structure of format table is shown in Figure 61 on page 103. The first byte should contain a descriptor value and the second byte should contain the sector number. The descriptor value should be 0 for a good sector, and any other descriptor value will cause an aborted error. The remaining bytes of the sector following the format table are ignored.

Since device performance is optimal at 1:1 interleave, and the device uses relative block addressing internally, the device will always format a track in the same way no matter what sector numbering is specified in the format table.

Output Parameters To The Device

Sector Number In LBA mode, this register specifies LBA address bits 0 - 7 to be formatted. (L=1)

Cylinder High/Low The cylinder number of the track to be formatted. (L=0)

In LBA mode, this register specifies LBA address bits 8 - 15 (Low), 16 - 23 (High) to be formatted. (L=1)

H The head number of the track to be formatted. (L=0)

In LBA mode, this register specifies LBA address bits 24 - 27 to be formatted. (L=1)

Input Parameters From The Device

- Sector Number** In LBA mode, this register specifies current LBA address bits 0-7. (L=1)
- Cylinder High/Low** In LBA mode, this register specifies current LBA address bits 8 - 15 (Low), 16 - 23 (High)
- H** In LBA mode, this register specifies current LBA address bits 24 - 27. (L=1)
- Error** The Error Register. An Abort error (ABT=1) will be returned under the following conditions:
- The descriptor value does not match the certain value. (except 00h)

In LBA mode, this command formats a single logical track including the specified LBA.

Explanation for descriptor

Descriptor : 00h The sector of data will be initialized to 00h.

Byte	Data	Description
0 1	xxh 00h	descriptor value for sector number 00h sector number
2 3	xxh 01h	descriptor value for sector number 01h sector number
4 5	xxh 02h	descriptor value for sector number 02h sector number
: :	: :	
N*2 N*2+1	xxh N	descriptor value for sector number N sector number (last sector for the track)
N*2+2 N*2+3 : : 510 511	00h 00h : : 00h 00h	remainder of buffer filled with 00h

Descriptor : 00h – Format sector as good sector

Figure 61. Format track data field format

12.5 Format Unit (F7h: Vendor Specific)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	V	V	V	V	V	V	V	V
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	0	1	1	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 62. Format Unit Command (F7h)

The Format Unit command initializes all user data sectors after merging reassigned sector location into the defect information of the device and clearing the reassign information. Both new reassign information and new defect information are available right after this command completion, and are also used on next power on reset or hard reset. Both previous information are erased from the device by this command.

Note that the Format Unit command initializes from LBA 0 to Native MAX LBA. Host MAX LBA set by Initialize Drive Parameter or Set MAX LBA/CYL command is ignored. So the protected area by Set MAX LBA/CYL command is also initialized.

The security erase prepare command should be completed immediately prior to the Format Unit command. If the device receives a Format Unit command without a prior Security Erase Prepare command the device aborts the Format Unit command.

If Feature register is NOT 11h, the device returns Abort error to the host.

This command does not request to data transfer.

Output Parameters To The Device

Feature Destination code for this command.
11H Merge reassigned location into the defect information

The execution time of this command is shown below.

DPLA-25120	about 16min
DPLA-24480	about 14min

12.6 Identify Device (ECh)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 63. Identify Device Command (ECh)

The Identify Device command requests the device to transfer configuration information to the host. The device will transfer a sector to the host containing the information in Figure 64 on page 107.

Word	Content	Description
00	045AH	Drive classification, bit assignments: 15(=0): 1=ATAPI device, 0=ATA device * 14(=0): 1=format speed tolerance gap required * 13(=0): 1=track offset option available * 12(=0): 1=data strobe offset option available * 11(=0): 1=rotational speed tolerance > 0.5% * 10(=1): 1=disk transfer rate > 10 Mbps * 9(=0): 1=disk transfer rate > 5 Mbps but <= 10 Mbps * 8(=0): 1=disk transfer rate <= 5 Mbps 7(=0): 1=removable cartridge device 6(=1): 1=fixed device * 5(=0): 1=spindle motor control option implemented * 4(=1): 1=head switch time > 15 us * 3(=1): 1=not MFM encoded * 2(=0): 1=soft sectored * 1(=1): 1=hard sectored 0(=0): Reserved
01	Note.1	Number of cylinders in default translate mode
02	0	* Number of removable cylinders
03	000FH	Number of heads in default translate mode
04	0	* Reserved
05	0	* Reserved
06	003FH	Number of sectors per track in default translate mode
07	0000H	* Number of bytes of sector gap
08	0000H	* Number of bytes in sync field
09	0000H	* Reserved
10-19	XXXX	Serial number in ASCII (0 = not specified)
20	0003H	* Controller type: 0003: dual ported, multiple sector buffer with look-ahead read
21	03A8H	* Buffer size in 512-byte increments (=468KB)
22	00XXH	Number of ECC bytes as currently selected via the set features command
23-26	XXXX	Microcode version in ASCII
27-46	Note.2	Model number in ASCII
47	0010H	Maximum number of sectors that can be transferred per interrupt on Read and Write Multiple commands
48	0000H	Capable of double word I/O, '0000'= cannot perform
49	0F00H	Capabilities, bit assignments: 15-14(=0) Reserved 13(=0) Standby timer value are vendor specific 12(=0) Reserved 11(=1) IORDY Supported 10(=1) IORDY can be disabled 9(=1) 1=LBA Supported 8(=1) 1=DMA Supported * 7- 0(=0) Reserved
50	0000H	15(=0) 1=Security Mode Feature Set Supported 14- 8(=0) Maximum number of passwords supported
51	0200H	PIO data transfer cycle timing mode
52	0200H	DMA data transfer cycle timing mode Refer Word 62 and 63

Figure 64. Identify device information

Word	Content	Description
53	XXX7H	Validity flag of the word 15- 3 Reserved 2(=1) 1=Word 88 is Valid 1(=1) 1=Word 64-70 are Valid 0(=1) 1=Word 54-58 are Valid
54	XXXXH	Number of current cylinders
55	XXXXH	Number of current heads
56	XXXXH	Number of current sectors per track
57-58	XXXXH	Current capacity in sectors Word 57 specifies the low word of the capacity
59	0XXXH	Current Multiple setting. bit assignments 15- 9(=0) Reserved 8 1= Multiple Sector Setting is Valid 7- 0 xxh = Current setting for number of sectors
60-61	Note.3	Total Number of User Addressable Sectors Word 60 specifies the low word of the number
62	XX07H	Single Word DMA Transfer Capability 15- 8 Single word DMA transfer mode active 7- 0(=7) Single word DMA transfer modes supported (support mode 0,1 and 2)
63	XX07H	Multiword DMA Transfer Capability 15- 8 Multi word DMA transfer mode active 7- 0(=7) Multi word DMA transfer modes supported (support mode 0,1 and 2)
64	0003H	Flow Control PIO Transfer Modes Supported 15- 8(=0) Reserved 7- 0(=3) Advanced PIO Transfer Modes Supported '11' = PIO Mode 3 and 4 Supported
65	0078H	Minimum Multiword DMA Transfer Cycle Time Per Word 15- 0(=78) Cycle time in nanoseconds (120ns, 16.6MB/s)
66	0078H	Manufacturer's Recommended Multiword DMA Transfer Cycle Time 15- 0(=78) Cycle time in nanoseconds (120ns, 16.6MB/s)
67	00F0H	Minimum PIO Transfer Cycle Time Without Flow Control 15- 0(=F0) Cycle time in nanoseconds (240ns, 8.3MB/s)
68	0078H	Minimum PIO Transfer Cycle Time With IORDY Flow Control 15- 0(=78) Cycle time in nanoseconds (120ns, 16.6MB/s)
69-79	0000H	Reserved
80	000EH	Major version number 15- 0(=0E) ATA-1, ATA-2 and ATA-3
81	0006H	Minor version number 15- 0(=06) ATA-3 X3T10 2008D revision 1
82	000BH	Command set supported 15- 4(=0) Reserved 3(=1) 1=supports Power Management Feature Set 2(=0) 1=supports Removable Feature Set 1(=1) 1=supports Security Feature Set 0(=1) 1=supports S.M.A.R.T Feature Set
83	4008H	Command set supported 15(=0) Always 14(=1) Always 13- 4(=0) Reserved 3(=1) 1=supports Advanced Power Management Feature Set 2- 0(=0) Reserved

Figure 65. Identify device information --- Continued ---

Word	Content	Description
84-85	0000H	Reserved
86	000XH	ABLE enable. Bit assignments 15- 4 Reserved 3 1= Enable, 0= Disable 2- 0 Reserved
87	0000H	Reserved
88	0007H	Ultra DMA Transfer mode (mode 2 supported)
89	000AH	Reserved
90	0010H	Reserved
91	4080H	ABLE mode current setting 15(=0) Always 14(=1) Always 13- 8(=0) Reserved 7- 0(=X) Current Adaptive Power Save Transition Setting Set by Set Features Command (01h to FEh)
92-127	0000H	Reserved
128	XXXXH	Security Mode Feature. Bit assignments 0 Capability 1= Support 1 Enable/Disable 1= Enable 2 Lock 1= Locked 3 Freeze 1= Frozen 4 Expire 1= Expired 8 Security Level 1= Maximum, 0= High 9-15 Reserved
129	XXXXH *	Current Set Feature Option. Bit assignments 0 Write Cache 1= Enable 1 Read Look-ahead 1= Enable 2 Reverting 1= Enable 3 Auto reassign 1= Enable 4-15 Reserved
130	XXXXH *	Reserved
131	000XH *	Initial Power Mode Selection. Bit assignments 0 Initial Power Mode 1= Standby, 0= Idle 1-15 Reserved
132-255	0000H	Reserved

Figure 66. Identify device information --- Continued ---

Note. The '*' mark in 'Content' field indicates the use of those parameters that are vendor specific.

Note 1. The number of cylinders is
2960H for DPLA-25120,
2430H for DPLA-24480,

Note 2. The model number in ASCII is
'IBM-DPLA-25120' for DPLA-25120,
'IBM-DPLA-24480' for DPLA-24480,

Note 3. Total number of user addressable sectors is
98BB60H for DPLA-25120,
859530H for DPLA-24480,

12.7 Identify Device DMA (EEh)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	1	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 67. Identify Device Command DMA (EEh)

The Identify Device DMA command requests the device to transfer configuration information to the host. The device will transfer the same 256 words of device identification data by the Identify Device command(ECh) via DMA channel.

12.8 Idle (E3h/97h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	0	1	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 68. Idle Command (E3h/97h)

The Idle command causes the device to enter Idle mode immediately, and set auto power down timeout parameter(standby timer). And then the timer starts counting down.

When the Idle mode is entered, the device is spun up to operating speed. If the device is already spinning, the spin up sequence is not executed.

During Idle mode the device is spinning and ready to respond to host commands immediately.

Output Parameters To The Device

Sector Count Timeout Parameter. If zero, the timeout interval(Standby Timer) is NOT disabled, but the timeout interval is set for 109 minutes automatically. If other than zero, the timeout interval is set for (Timeout Parameter × 5) seconds.

The device will enter Standby mode automatically if the timeout interval expires with no device access from the host. The timeout interval will be reinitialized if there is a device access before the timeout interval expires.

12.9 Idle Immediate (E1h/95h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 69. Idle Immediate Command (E1h/95h)

The Idle Immediate command causes the device to enter Idle mode.

The device is spun up to operating speed. If the device is already spinning, the spin up sequence is not executed.

During Idle mode the device is spinning and ready to respond to host commands immediately.

The Idle Immediate command will not affect the auto power down timeout parameter.

12.10 Initialize Device Parameters (91h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	H	H	H	H
Command	1	0	0	1	0	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	-	-	0	-	V

Figure 70. Initialize Device Parameters Command (91h)

The Initialize Device Parameters command enables the host to set the number of sectors per track and the number of heads minus 1, per cylinder. Words 54-58 in Identify Device Information reflects these parameters.

The parameters remain in effect until the following events:

- Another Initialize Device Parameters command is received.
- The device is powered off.
- Hard reset occurs.
- Soft reset occurs and the Set Feature option of CCh is set instead of 66h.

Output Parameters To The Device

Sector Count The number of sectors per track. 0 does not mean there are 256 sectors per track, but there is no sector per track.

H The number of heads minus 1 per cylinder. The minimum is 0 and the maximum is 15.

Note: The following condition needs to be satisfied to avoid invalid number of cylinder beyond FFFFh, which will cause performance degradation of the drive.

$$(\text{Total customer usable data sectors}) / ((\text{Sector Count}) * (\text{H} + 1)) \rightarrow \text{FFFFh}$$

The total customer usable data sectors are indicated at 3.1, “Logical Drive Format” on page 9, and related description is at 10.3.1, “Logical CHS Addressing Mode” on page 71.

12.11 Read Buffer (E4h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 71. Read Buffer Command (E4h)

The Read Buffer command transfers a sector of data from the sector buffer of device to the host.

The sector is transferred through the Data Register 16 bits at a time.

The sector transferred will be from the same part of the buffer written to by the last Write Buffer command. The contents of the sector may be different if any reads or writes have occurred since the Write Buffer command was issued.

12.12 Read DMA (C8h/C9h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	1	0	0	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 72. Read DMA Command (C8h/C9h)

The Read DMA command reads one or more sectors of data from disk media, then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. The data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Output Parameters To The Device

- Sector Count** The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
- Sector Number** The sector number of the first sector to be transferred. (L=0)
In LBA mode, this register specifies LBA address bits 0 - 7 to be transferred. (L=1)
- Cylinder High/Low** The cylinder number of the first sector to be transferred. (L=0)
In LBA mode, this register specifies LBA address bits 8 - 15 (Low) 16 - 23 (High) to be transferred. (L=1)

- H** The head number of the first sector to be transferred. (L=0)
In LBA mode, this register specifies LBA bits 24-27 to be transferred. (L=1)
- R** The retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

- Sector Count** The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
- Sector Number** The sector number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
- Cylinder High/Low** The cylinder number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
- H** The head number of the sector to be transferred. (L=0)
In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

12.13 Read Long (22h/23h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	0	0	0	0	0	0	0	1
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	0	1	0	0	0	1	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 73. Read Long Command (22h/23h)

The Read Long command reads the designated one sector of data and the ECC bytes from the disk media, then transfers the data and ECC bytes from the device to the host.

After 512 bytes of data have been transferred, the device will keep setting DRQ=1 to indicate that the device is ready to transfer the ECC bytes to the host. The data is transferred 16 bits at a time, and the ECC bytes are transferred 8 bits at a time. The number of ECC bytes are 4 or 28 according to the setting of Set Feature option. The default setting is 4 bytes of ECC data.

The command makes a single attempt to read the data and does not check the data using ECC. Whatever is read is returned to the host.

Output Parameters To The Device

Sector Count The number of continuous sectors to be transferred. The Sector Count must be set to one.

Sector Number The sector number of the sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

- H** The head number of the sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 24-27. (L=1)
- R** The retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

- Sector Count** The number of requested sectors not transferred.
- Sector Number** The sector number of the transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
- Cylinder High/Low** The cylinder number of the transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
- H** The head number of the transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 24-27. (L=1)

It should be noted that the device internally uses 28 bytes of ECC data on all data written or read from the disk. The 4 byte mode of operation is provided via an emulation. It is recommended that for testing the effectiveness and integrity of the devices ECC functions that the 28 byte ECC mode should be used.

12.14 Read Multiple (C4h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	—	—	—	—	—	—	—	—
Feature	—	—	—	—	—	—	—	—
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	0	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	—	—	—	—	—	—	—	—
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	—	—	—	—	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	—	0	—	V

Figure 74. Read Multiple Command (C4h)

The Read Multiple command reads one or more sectors of data from disk media, then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time. Command execution is identical to the Read Sectors command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector.

Output Parameters To The Device

- Sector Count** The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
- Sector Number** The sector number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 0 - 7. (L=1)
- Cylinder High/Low** The cylinder number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
- H** The head number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 24 - 27. (L=1)

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

12.15 Read Native Max LBA/CYL (F8h: Vendor Specific)

Command Block Output Registers							
Register	7	6	5	4	3	2	1 0
Data	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-
Device/Head	1	L	1	D	-	-	-
Command	1	1	1	1	1	0	0 0

Command Block Input Registers							
Register	7	6	5	4	3	2	1 0
Data	-	-	-	-	-	-	-
Error	...See Below...						
Sector Count	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H
Status	...See Below...						

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 75. Read Native Max LBA/CYL (F8h)

This command returns the native max LBA/CYL of HDD which is not effected by Set Max LBA/CYL command.

Output Parameters To The Device

- L** LBA mode. Indicates the addressing mode. L=0 specifies CHS mode and L=1 does LBA addressing mode.
- D** The device number bit. Indicates that the device number bit of the Device/Head Register should be specified. D=0 selects the master device and D=1 selects the slave device.
- Indicates that the bit is not used.

Input Parameters From The Device

- Sector Number** In LBA mode, this register contains native max LBA bits 0 - 7. (L=1)
In CHS mode, this register contains native max sector number. (L=0)
- Cylinder High/Low** In LBA mode, this register contains native max LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
In CHS mode, this register contains native max cylinder number. (L=0)
- H** In LBA mode, this register contains native max LBA bits 24 - 27. (L=1)
In CHS mode, this register contains native max head number. (L=0)

- V Valid. Indicates that the bit is part of an input parameter and will be set to 0 or 1 by the device.
- Indicates that the bit is not used.

12.16 Read Sectors (20h/21h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	0	1	0	0	0	0	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 76. Read Sectors Command (20h/21h)

The Read Sectors command reads one or more sectors of data from disk media, then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Output Parameters To The Device

Sector Count The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number The sector number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H The head number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 24 - 27. (L=1)

R The retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

12.17 Read Verify Sectors (40h/41h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	0	1	0	0	0	0	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 77. Read Verify Sectors Command (40h/41h)

The Read Verify Sectors verifies one or more sectors on the device. No data is transferred to the host.

The difference of Read Sectors command and Read Verify Sectors command is whether the data is transferred to the host or not.

If an uncorrectable error occurs, the read verify will be terminated at the failing sector.

Output Parameters To The Device

- Sector Count** The number of continuous sectors to be verified. If zero is specified, then 256 sectors will be verified.
- Sector Number** The sector number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 0 - 7. (L=1)
- Cylinder High/Low** The cylinder number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
- H** The head number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 24 - 27. (L=1)
- R** The retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

Sector Count	The number of requested sectors not verified. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

12.18 Recalibrate (1xh)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	0	0	0	1	-	-	-	-

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	V	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 78. Recalibrate Command (1xh)

The Recalibrate command moves the read/write heads from anywhere on the disk to cylinder 0.

If the device cannot reach cylinder 0, T0N (Track 0 Not Found) will be set in the Error Register.

12.19 Security Disable Password (F6h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	0	1	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 79. Security Disable Password Command (F6h)

The Security Disable Password command disables the security mode feature (device lock function).

The Security Disable Password command requests a transfer of a single sector of data from the host including information specified in Figure 80. Then the device checks the transferred password. If the User Password or Master Password matches the given password, the device disables the security mode feature (device lock function). This command does not change the Master Password which may be re-activated later by setting User Password. This command should be executed in device unlock mode.

Word	Description
00	Control word bit 0 : Identifier (1- Master, 0- User) bit 1-15 : Reserved
01-16	Password (32 bytes)
17-255	Reserved

Figure 80. Password Information for Security Disable Password command

The device will compare the password sent from this host with that specified in the control word.

Identifier Zero indicates that the device should check the supplied password against the user password stored internally. One indicates that the device should check the given password against the master password stored internally.

12.20 Security Erase Prepare (F3h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	0	0	1	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 81. Security Erase Prepare Command (F3h)

The Security Erase Prepare Command must be issued immediately before the Security Erase Unit Command to enable device erasing and unlocking.

The Security Erase Prepare Command must be issued immediately before the Format Unit Command. This command is to prevent accidental erasure of the device.

This command does not request to transfer data.

12.21 Security Erase Unit (F4h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	0	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 82. Security Erase Unit Command (F4h)

The Security Erase Unit command initializes all user data sectors, then disables the device lock function.

Note that the Security Erase Unit command initializes from LBA 0 to Native MAX LBA. Host MAX LBA set by Initialize Drive Parameter or Set MAX LBA/CYL command is ignored. So the protected area by Set MAX LBA/CYL command is also initialized.

This command requests to transfer a single sector data from the host including information specified in Figure 83.

If the password does not match then the device rejects the command with an Aborted error.

Word	Description
00	Control word bit 0 : Identifier (1- Master, 0- User) bit 1-15 : Reserved
01-16	Password (32 bytes)
17-255	Reserved

Figure 83. Erase Unit information

Identifier Zero indicates that the device should check the supplied password against the user password stored internally. One indicates that the device should check the given password against the master password stored internally.

The Security Erase Unit command erases all user data and disables the security mode feature (device lock function). So after completing this command, all user data will be initialized to zero with write operation. At this time, it is not verified with read operation whether the sector of data is initialized correctly. Also, the defective sector information and the reassigned sector information for the device are not updated. The security erase prepare command should be completed immediately prior to the Security Erase Unit command. If the device receives a Security Erase Unit command without a prior Security Erase Prepare command the device aborts the security erase unit command.

This command disables the security mode feature (device lock function), however the master password is still stored internally within the device and may be re-activated later when a new user password is set. If you execute this command on disabling the security mode feature (device lock function), the password sent by the host is NOT compared with the password stored in the device for both the Master Password and the User Password, and then the device only erases all user data.

The execution time of this command is shown below.

DPLA-25120 16 min

DPLA-24480 14 min

12.22 Security Freeze Lock (F5h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	0	1	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 84. Security Freeze Lock Command (F5h)

The Security Freeze Lock Command allows the device to enter frozen mode immediately.

After this command is completed, the command which updates Security Mode Feature (Device Lock Function) is rejected.

| Frozen mode is quitted only by Power off or Hard Reset.

The following commands are rejected when the device is in frozen mode. For detail, refer to Figure 52 on page 82.

- Security Set Password
- Security Unlock
- Security Disable Password
- Security Erase Unit

12.23 Security Set Password (F1h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	0	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 85. Security Set Password Command (F1h)

The Security Set Password command enables security mode feature (device lock function), and sets the master password or the user password.

The security mode feature (device lock function) is enabled by this command, and the device is not locked immediately. The device is locked after next power on reset or hard reset. When the MASTER password is set by this command, the master password is registered internally, but the device is NOT locked after next power on reset or hard reset.

This command requests a transfer of a single sector of data from the host including the information specified in Figure 86 on page 134.

The data transferred controls the function of this command.

Word	Description
00	Control word bit 0 : Identifier (1- Master, 0- User) bit 1-7 : Reserved bit 8 : Security level (1- Maximum, 0- High) bit 9-15 : Reserved
01-16	Password (32 byte)
17-255	Reserved

Figure 86. Security Set Password Information

- Identifier** Zero indicates that device regards Password as User Password. One indicates that device regards Password as Master Password.
- Security Level** Zero indicates High level, one indicates Maximum level. If the host sets High level and the password is forgotten, then the Master Password can be used to unlock the device. If the host sets Maximum level and the user password is forgotten, only an Security Erase Prepare/Security Unit command can unlock the device and all data will be lost.
- Password** The text of the password - all 32 bytes are always significant.

The setting of the Identifier and Security level bits interact as follows.

- Identifier=User / Security level = High** The password supplied with the command will be saved as the new user password. The security mode feature (lock function) will be enabled from the next power on. The file may then be unlocked by either the user password or the previously set master password.
- Identifier=Master / Security level = High** This combination will set a master password but will NOT enable the security mode feature (lock function).
- Identifier=User / Security level = Maximum** The password supplied with the command will be saved as the new user password. The security mode feature (lock function) will be enabled from the next power on. The file may then be unlocked by only the user password. The master password previously set is still stored in the file but may NOT be used to unlock the device.
- Identifier=Master / Security level = Maximum** This combination will set a master password but will NOT enable the security mode feature (lock function).

12.24 Security Unlock (F2h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	0	0	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 87. Security Unlock Command (F2h)

This command unlocks the password and causes the device to enter device unlock mode. If power on reset or hard reset is done without executing the Security Disable Password command after this command is completed, the device will be in device lock mode. The password has not been changed yet.

The Security Unlock command requests to transfer a single sector of data from the host including information specified in Figure 88 on page 136.

If the Identifier bit is set to master and the file is in high security mode then the password supplied will be compared with the stored master password. If the file is in maximum security mode then the security unlock will be rejected.

If the Identifier bit is set to user, then the file compares the supplied password with the stored user password.

If the password compare fails then the device returns an abort error to the host and decrements the unlock attempt counter. This counter is initially set to 5 and is decremented for each password mismatch. When this counter reaches zero then all password protected commands are rejected until a hard reset or a power off.

Word	Description
00	Control word bit 0 : Identifier (1- Master, 0- User) bit 1-15 : Reserved
01-16	Password (32 bytes)
17-255	Reserved

Figure 88. Security Unlock Information

Identifier Zero indicates that device regards Password as User Password. One indicates that device regards Password as Master Password.

The user can detect if the attempt to unlock the device has failed due to a mismatched password as this is the only reason that an abort error will be returned by the file AFTER the password information has been sent to the device. If an abort error is returned by the device BEFORE the password data has been sent to the file then another problem exists.

12.25 Seek (7xh)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	1	1	1	-	-	-	-

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 89. Seek Command (7xh)

The Seek command initiates a seek to the designated track and selects the designated head. The device need not be formatted for a seek to execute properly.

Output Parameters To The Device

Sector Number In LBA mode, this register specifies LBA address bits 0 - 7 for seek. (L=1)

Cylinder High/Low The cylinder number of the seek.

In LBA mode, this register specifies LBA address bits 8 - 15 (Low), 16 - 23 (High) for seek. (L=1)

H The head number of the seek.

In LBA mode, this register specifies LBA address bits 24 - 27 for seek. (L=1)

Input Parameters From The Device

Sector Number In LBA mode, this register contains current LBA bits 0 - 7. (L=1)

Cylinder High/Low In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

12.26 Set Features (EFh)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	V	V	V	V	V	V	V	V
Sector Count	Note.1							
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	1	1	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 90. Set Features Command (EFh)

The Set Feature command establishes the following parameters which affect the execution of certain features as shown in below table.

ABT will be set to 1 in the Error Register if the Feature register contains any undefined values.

Output Parameters To The Device

Feature	Destination code for this command.
02H	Enable write cache (Warning.1)
03H	Set transfer mode based on value in sector count register
05H	Enable Adaptive mode
44H	28 bytes of ECC apply on Read Long/Write Long commands
55H	Disable read look-ahead feature
66H	Disable reverting to power on defaults
82H	Disable write cache
85H	Disable Adaptive mode
AAH	Enable read look-ahead feature
BBH	4 bytes of ECC apply on Read Long/Write Long commands

CCH Enable reverting to power on defaults

Note 1.

When Feature register is 03h (=Set Transfer mode), the Sector Count Register specifies the transfer mechanism. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value.

PIO Default Transfer Mode	00000	000
PIO Default Transfer Mode,Disable IORDY	00000	001
PIO Flow Control Transfer Mode x	00001	nnn (nnn=000,001,010,011,100)
Single word DMA mode x	00010	nnn (nnn=000,001,010)
Multiword DMA mode x	00100	nnn (nnn=000,001,010)
Ultra DMA mode x	01000	nnn (nnn=000,001,010)

Note 2.

When Feature register is 05h (=Enable Adaptive mode), the Sector Count Register specifies the ABLE2 (=Adaptive battery life extender II) mode. ABLE2 support three modes.

C0h - FEh ... Able mode 0	(Up to Active Idle)
80h - BFh ... Able mode 1	(Up to Low power Idle)
60h - 7Fh ... Able mode 2	(Up to Standby) Performance
30h - 5Fh ... Able mode 2	(Up to Standby) Intermediate
01h - 2Fh ... Able mode 2	(Up to Standby) Low power
00h, FFh ... Aborted	

When Feature register is 85h (=Disable Adaptive mode), the ABLE mode is set to 0.

Note 3.

If the number of auto reassigned sectors reaches the device's reassignment capacity, the write cache function will be automatically disabled. Although the device still accepts the Set Features command (with Feature register = 02h) without error, the write cache function will remain disabled. For current write cache function status, please refer to the Identify Device Information(129word) by Identify Device command.

Note 4.

After power on reset or hard reset, the device is set to the following features as default.

Write cache	:	Enable
Adaptive battery life extender	:	Enable (Able mode 1)
ECC bytes	:	4 bytes
Read look-ahead	:	Enable
Reverting to power on defaults	:	Disable

12.27 Set Max LBA/CYL (F9h: Vendor Specific)

Command Block Output Registers							
Register	7	6	5	4	3	2	1 0
Data	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	B
Sector Number	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H
Command	1	1	1	1	1	0	0 1

Command Block Input Registers							
Register	7	6	5	4	3	2	1 0
Data	-	-	-	-	-	-	-
Error	...See Below...						
Sector Count	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H
Status	...See Below...						

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 91. Set Max LBA/CYL (F9h)

This command overwrites the max LBA/CYL of HDD in a range of actual device capacities. Once device receives this command, all accesses beyond that LBA/CYL are rejected with setting ABORT bit in status register. Identify device command and Identify device DMA command returns the LBA/CYL which is set via this command as a default value.

Read Native Max LBA/CYL command should be issued and completed immediately prior to issuing Set Max LBA/CYL command. If the device receives Set Max LBA/CYL command without a prior Read Native Max LBA/CYL command, the device aborts the Set Max LBA/CYL command.

In CHS mode,Cylinder High,Cylinder Low specify the max cylinder number. The Head number of DEVICE/HEAD and Sector Number are ignored. The default value(See default CHS in Identify device information) is used for that.

In LBA mode,the Head number of DEVICE/HEAD , Cylinder High, Cylinder Low and Sector Number specify the max LBA. This command will be set this LBA as the max LBA of the device.

Output Parameters To The Device

- B** Option bit for selection whether nonvolatile or volatile. B=0 is volatile condition. When B=1, MAX LBA/CYL which is set by Set Max LBA/CYL command is preserved by POR and HARD RESET. When B=0, MAX LBA/CYL which is set by Set Max LBA/CYL command will be lost by POR and HARD RESET.

Sector Number	In LBA mode, this register contains LBA bits 0 - 7 which is to be input.(L=1) In CHS mode, this register is ignored. (L=0)
Cylinder High/Low	In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High) which is to be set. (L=1) In CHS mode, this register contains cylinder number which is to be input.(L=0)
H	In LBA mode, this register contains LBA bits 24 - 27 which is to be input.(L=1) In CHS mode, this register is ignored. (L=0)
L	LBA mode.Indicates the addressing mode.L=0 specifies CHS mode and L=1 does LBA addressing mode.
D	The device number bit. Indicates that the device number bit of the Device/Head should be specified. D=0 selects the master device and D=1 selects the slave device.
V	Valid. Indicates that the bit is part of an output parameter and should be specified.
-	Indicates that the bit is not used.

Input Parameters From The Device

Sector Number	In LBA mode, this register contains Adjusted max LBA bits 0 - 7.(L=1) In CHS mode, this register contains max sector number(= 63). (L=0)
Cylinder High/Low	In LBA mode, this register contains Adjusted max LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1) In CHS mode, this register contains max cylinder number which is set. (L=0)
H	In LBA mode, this register contains Adjusted max LBA bits 24 - 27. (L=1) In CHS mode, this register contains max head number(= 15).(L=0)
V	Valid. Indicates that the bit is part of an input parameter and will be set to 0 or 1 by the device.
-	Indicates that the bit is not used.

12.28 Set Multiple (C6h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	0	0	0	1	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 92. Set Multiple Command (C6h)

The Set Multiple command enables the device to perform Read and Write Multiple commands and establishes the block size for these commands. The block size is the number of sectors to be transferred for each interrupt.

The default block size after power up, or hard reset is 0, and Read Multiple and Write Multiple commands are disabled.

If an invalid block size is specified, an Abort error will be returned to the host, and Read Multiple and Write Multiple commands will be disabled.

Output Parameters To The Device

Sector Count. The block size to be used for Read Multiple and Write Multiple commands. Valid block sizes can be selected from 0, 2, 4, 8 or 16. If 0 is specified, then Read Multiple and Write Multiple commands are disabled.

12.29 Sleep (E6h/99h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	1	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 93. Sleep Command (E6h/99h)

This command is the only way to cause the device to enter Sleep Mode.

When this command is issued, the device confirms the completion of the cached write commands before it asserts INTRQ. Then the device is spun down, and the interface becomes inactive. The only way to recover from Sleep Mode is with a software reset or a hardware reset.

The use of hardware reset to recover from Sleep Mode may be incompatible with continued operation of the host system.

If the device is already spun down, the spin down sequence is not executed.

12.30 S.M.A.R.T. Function Set (B0h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	V	V	V	V	V	V	V	V
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	0	1	0	0	1	1	1	1
Cylinder High	1	1	0	0	0	0	1	0
Device/Head	1	-	1	D	-	-	-	-
Command	1	0	1	1	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 94. S.M.A.R.T. Function Set Command (B0h)

The S.M.A.R.T. Function Set command provides access to Attribute Values, Attribute Thresholds and other low level subcommands that can be used for logging and reporting purposes and to accommodate special user needs. The S.M.A.R.T. Function Set command has several separate subcommands which are selectable via the device's Features Register when the S.M.A.R.T. Function Set command is issued by the host.

In order to select a subcommand the host must write the subcommand code to the device's Features Register before issuing the S.M.A.R.T. Function Set command. The subcommands and their respective codes are listed below.

Code	Subcommand
D0h	SMART Read Attribute Values
D1h	SMART Read Attribute Thresholds
D2h	SMART Enable/disable Attribute Autosave
D3h	SMART Save Attribute Values
D4h	SMART Execute Off-line Immediate
D8h	SMART Enable Operations
D9h	SMART Disable Operations

12.30.1.1 SMART Read Attribute Values (Subcommand D0h)

This subcommand returns the device's Attribute Values to the host. Upon receipt of the SMART Read Attribute Values subcommand from the host, the device asserts BSY, saves any updated Attribute Values to the Attribute Data sectors, asserts DRQ, clears BSY, asserts INTRQ, and then waits for the host to transfer the 512 bytes of Attribute Value information from the device via the Data Register.

12.30.1.2 SMART Read Attribute Thresholds (Subcommand D1h)

This subcommand returns the device's Attribute Thresholds to the host. Upon receipt of the SMART Read Attribute Thresholds subcommand from the host, the device asserts BSY, reads the Attribute Thresholds from the Attribute Threshold sectors, asserts DRQ, clears BSY, asserts INTRQ, and then waits for the host to transfer the 512 bytes of Attribute Thresholds information from the device via the Data Register.

12.30.1.3 SMART Enable/Disable Attribute Autosave (Subcommand D2h)

This subcommand enables and disables the attribute autosave feature of the device. The SMART Enable/Disable Attribute Autosave subcommand allows the device to automatically save its updated Attribute Values to the Attribute Data Sector at the timing of the first transition to LP idle mode after 30 minutes since the last saving of Attribute Values; this subcommand causes the autosave feature to be disabled. The state of the Attribute Autosave feature (either enabled or disabled) will be preserved by the device across power cycle.

A value of 00h written by the host into the device's Sector Count Register before issuing the SMART Enable/Disable Attribute Autosave subcommand will cause this feature to be disabled. Disabling this feature does not preclude the device from saving Attribute Values to the Attribute Data sectors during some other normal operation such as during a power-up or power-down.

A value of F1h written by the host into the device's Sector Count Register before issuing the SMART Enable/Disable Attribute Autosave subcommand will cause this feature to be enabled. Any other non-zero value written by the host into this register before issuing the SMART Enable/Disable Attribute Autosave subcommand will not change the current Autosave status but the device will respond with the error code specified in Figure 100 on page 156.

The SMART Disable Operations subcommand disables the autosave feature along with the device's SMART operations.

Upon the receipt of the subcommand from the host, the device asserts BSY, enables or disables the Autosave feature, clears BSY and asserts INTRQ.

12.30.1.4 SMART Save Attribute Values (Subcommand D3h)

This subcommand causes the device to immediately save any updated Attribute Values to the device's Attribute Data sector regardless of the state of the Attribute Autosave feature. Upon receipt of the SMART Save Attribute Values subcommand from the host, the device asserts BSY, writes any updated Attribute Values to the Attribute Data sector, clears BSY and asserts INTRQ.

12.30.1.5 SMART Execute Off-line Immediate (Subcommand D4h)

This subcommand causes the device to immediately initiate the set of off-line data collection activities that collect attribute data in an off-line mode.

Upon receipt of the subcommand from the host, the device sets BSY to one, begins its set of off-line data collection activities, clears BSY to zero and asserts INTRQ.

During execution of its off-line activities the device will not set BSY nor clear DRDY.

If the device is in the process of performing its set of off-line data collection activities as a result of receiving a SMART Execute Off-line Immediate subcommand from the host and is interrupted by any new command from the host, the device will abort its off-line data collection activities and service the host within two seconds after receipt of the new command. Off-line data collection activity must be restarted by a new SMART Execute Off-line Immediate subcommand from the host.

An issuance of this subcommand just initiates only one off-line test item (called a "segment"). Once a segment completes, the device just advances the current segment pointer to next one and set the off-line data collection status to be 02h ("A segment completed"), then terminates off-line activity. The host shall continue to issue this subcommand until off-line data collection status is set to 06h ("All Segments Completed") in order to perform all set of off-line segments.

The host can obtain device's estimated time to complete the current segment, along with the off-line data collection status, by issuing a SMART Read Attribute Values subcommand. Since the device may not complete a segment within its estimated time, an issuance of a SMART Read Attribute Values subcommand could abort ongoing off-line test. In this case, the current segment pointer remains unchanged and off-line data collection status is set to 02h (as any other commands do for ongoing off-line test).

12.30.1.6 SMART Enable Operations (Subcommand D8h)

This subcommand enables access to all S.M.A.R.T. capabilities within the device. Prior to receipt of a SMART Enable Operations subcommand, Attribute Values are neither monitored nor saved by the device. The state of S.M.A.R.T. (either enabled or disabled) will be preserved by the device across power cycles. Once enabled, the receipt of subsequent SMART Enable Operations subcommands will not affect any of the Attribute Values.

Upon receipt of the SMART Enable Operations subcommand from the host, the device asserts BSY, enables S.M.A.R.T. capabilities and functions, clears BSY and asserts INTRQ.

12.30.1.7 SMART Disable Operations (Subcommand D9h)

This subcommand disables all S.M.A.R.T. capabilities within the device including the device's attribute autosave feature. After receipt of this subcommand the device disables all S.M.A.R.T. operations. Non self-preserved Attribute Values will no longer be monitored. The state of S.M.A.R.T. (either enabled or disabled) is preserved by the device across power cycles. Note that this subcommand does not preclude the device's power mode attribute autosaving.

Upon receipt of the SMART Disable Operations subcommand from the host, the device asserts BSY, disables S.M.A.R.T. capabilities and functions, clears BSY and asserts INTRQ.

After receipt of the device of the SMART Disable Operations subcommand from the host, all other S.M.A.R.T. subcommands -- with the exception of SMART Enable Operations -- are disabled, and invalid

and will be aborted by the device (including the SMART Disable Operations subcommand), returning the error code as specified in Figure 100 on page 156.

Any Attribute Values accumulated and saved to volatile memory prior to receipt of the SMART Disable Operations command will be preserved in the device's Attribute Data Sectors. If the device is re-enabled, these Attribute Values will be updated, as needed, upon receipt of a SMART Read Attribute Values or SMART Save Attribute Values command.

12.30.1.8 SMART Return Status (Subcommand DAh)

This command is used to communicate the reliability status of the device to the host's request. Upon receipt of the SMART Return Status subcommand the device asserts BSY, saves any updated Attribute Values to the reserved sector and compares the updated Attribute Values to the Attribute Thresholds.

If the device does not detect a Threshold Exceeded Condition, or detects a Threshold Exceeded Condition but involving attributes are advisory, the device loads 4Fh into the Cylinder Low register, C2h into the Cylinder High register, clears BSY, and asserts INTRQ.

If the device detects a Threshold Exceeded Condition for prefailure attributes, the device loads F4h into the Cylinder Low register, 2Ch into the Cylinder High register, clears BSY, and asserts INTRQ. Advisory attributes never result in negative reliability condition.

12.30.2 Device Attributes Data Structure

The following defines the 512 bytes that make up the Attribute Value information. This data structure is accessed by the host in its entirety using the SMART Read Attribute Values subcommand. All multi-byte fields shown in these data structures follow the ATA-3 specification for byte ordering, namely that the least significant byte occupies the lowest numbered byte address location in the field.

Description	Bytes	Offset	Format	Value
Data Structure Revision Number	2	00h	binary	0005h
1st Device Attribute	12	02h	(*1)	(*2)
...	..			
...	..			
30th Device Attribute	12	15Eh	(*1)	(*2)
Off-line data collection status	1	16Ah	(*1)	(*2)
Total segments required for off-line data collection	1	16Bh	(*1)	07h
Total time in seconds to complete next segment	2	16Ch	(*1)	(*2)
Current segment pointer	1	16Eh	(*1)	(*2)
Off-line data collection capability	1	16Fh	(*1)	05h
S.M.A.R.T. capability	2	170h	(*1)	03h
Reserved	16	172h		(*3)
Vendor specific	125	182h		(*3)
Data structure checksum	1	1FFh		(*2)
	512			

(*1) – See following definitions

(*2) – Value varied by actual operating condition

(*3) – Filled with 00h

Figure 95. Device Attribute Data Structure

12.30.2.1 Data Structure Revision Number

The Data Structure Revision Number identifies which version of this data structure is implemented by the device. This revision number will be set to 0005h. This revision number identifies both the Attribute Value and Attribute Threshold Data structures.

12.30.2.2 Individual Attribute Data Structure

The following defines the 12 bytes that make up the information for each Attribute entry in the Device Attribute Data Structure.

Description	Bytes	Offset	Format
Attribute ID Number (01h to FFh)	1	00h	binary
Status Flags	2	01h	bit flags
Bit 0 Pre-Failure/Advisory			
Bit 1 On-line Collection			
Bit 2-5 Reserved (may either 0 or 1)			
Bit 6-15 Reserved (all 0)			
Attribute Value (valid values from 01h to FEh)	1	03h	binary
00h invalid for attribute value – not to be used			
01h minimum value			
64h initial value for all attributes prior to any data collection			
FDh maximum value			
FEh value is not valid			
FFh invalid for attribute value – not to be used			
Reserved (may not be 0)	1	04h	binary
Reserved (may not be 0)	6	05h	binary
Reserved (00h)	1	0Bh	binary
Total Bytes	12		

Figure 96. Individual Attribute Data Structure

12.30.2.2.1 Attribute ID Numbers: Any non-zero value in the Attribute ID Number indicates an active attribute. The device supports following Attribute ID Numbers. Those marked with (*) indicate that corresponding Attribute Values can be either collected on-line or off-line.

ID	Attribute Name
0	Indicates that this entry in the data structure is not used
1	Raw Read Error Rate (*)
2	Throughput Performance (*)
3	Spin Up Time
4	Start/Stop Count
5	Reallocated Sector Count

7	Seek Error Rate
8	Seek Time Performance (*)
9	Power-On Hours Count
10	Spin Retry Count
12	Device Power Cycle Count
220	Disk Shift
221	G-Sense Error Rate
222	Loaded Hours
223	Load Retry Count
224	Load Friction
225	Load Cycle Count
226	Load-in Time
227	Torq-amp Count
228	Power-off Retract Count

12.30.2.2.2 Status Flag Definitions

Bit	Flag Name	Definition
0	Pre-Failure/ Advisory bit	If bit = 0, an Attribute Value less than or equal to its corresponding Attribute Threshold indicates an Advisory condition where the usage or age of the device has exceeded its intended design life period. If bit = 1, an Attribute Value less than or equal to its corresponding Attribute Threshold indicates a Pre-Failure condition where imminent loss of data is being predicted.
1	On-Line Collective bit	If bit = 0, the Attribute Value is updated only during Off-Line testing. If bit = 1, the Attribute Value is updated only during On-Line testing
2-5	Reserved bits	may either 0 or 1
6-15	Reserved bits	Always 0

Figure 97. Status Flag Definitions

12.30.2.2.3 Normalized Values: The device will perform conversion of the raw Attribute Values to transform them into normalized values, which the host can then compare with the Threshold values. A Threshold is the excursion limit for a normalized Attribute Value. In normalizing the raw data, the device will perform any necessary statistical validity checks to ensure that an instantaneous raw value is not improperly reflected in the normalized Attribute Value (i.e., one read error in the first 10 reads being interpreted as exceeding the read error rate threshold when the subsequent 1 billion reads all execute without error). The end points for the normalized values for all Attributes will be 1 (01h) at the low end, and 100 (64h) at the high end for the device. For Performance and Error Rate Attributes, values greater than 100 are also possible, up to a maximum value of 253 (FDh).

12.30.2.3 Off-Line Data Collection Status

The value of this byte defines the current status of the off-line activities of the device. Bit 7 indicates Automatic Off-Line Data Collection Status.

Bit 7 Automatic Off-Line Data Collection Status

0 Automatic Off-Line Data Collection is enabled.

1 Automatic Off-Line Data Collection is disabled.

Bits 0 thru 6 represents a hexadecimal status value reported by the device.

Value Definition

0 Off-line data collection never started

- 1 Segment completed without error
- 2 All segments completed without errors. In this case, current segment pointer equals to total segments required.
- 5 Off-line data collecting aborted by interrupting command
- 6 Off-line data collection aborted with fatal error

12.30.2.4 Total Segments Required for Off-line Data Collection

The device will return 01h as the total segments for off-line data collection. A segment is a unit of off-line data collection activity. The device divides its segment into 7 subsegments. A subsegment is not a host-visible test unit. Subsegment 1 through 4 are raw read error rate and throughput measurement. Each of them reads from LBA 0000h to 95040h, resulting the total number of read bits to be 10000269312. Subsegment 5 is 1680 track to track seeks. Subsegment 6 is 1680 1/3 stroke seeks. Subsegment 7 = 1680 full stroke seeks.

12.30.2.5 Total Time in Seconds to Complete Next Segment

This field tells the host how many seconds the device requires to complete the segment pointed by the current segment pointer. The host can use this time to set a count down timer that will trigger it to issue the “SMART Read Attribute Values” subcommand to check on the status of off-line data collection. This field indicates the total time in seconds for the first segment if the current segment pointer is 00h or the off-line status indicates all segments completed (02h).

12.30.2.6 Current Segment Pointer

This byte is a counter indicating the next segment to execute as an off-line data collection activity. This varies from 00h to the total number of segments. The current segment pointer will be 00h if the off-line data collection has not been started. If the off-line data collection is aborted by a command or an error (i.e., the status is 05h or 06h), this byte will point to the aborted segment. If the all segments complete, this byte will equal to the total number of segments.

12.30.2.7 Off-Line Data Collection Capability

The device returns 05h as its off-line data collection capability which means:

Bit	Definition
0	Execute Off-line Immediate is implemented
1	Enable/Disable Automatic Off-line is NOT implemented
2	Abort/restart off-line by host

The device will abort all off-line data collection activity initiated by an S.M.A.R.T. Execute Off-line Immediate subcommand upon receipt of a new command. Off-line data collection activity must be restarted by a new S.M.A.R.T. Execute Off-line Immediate subcommand from the host.

12.30.2.8 S.M.A.R.T. Capability

This word of bit flags describes the S.M.A.R.T. capabilities of the device. The device will return 03h as its S.M.A.R.T. capability which means:

Bit	Definition
0	Power mode attribute saving capability If bit = 1, the device will save its Attribute Values prior to going into a power saving mode (Standby or Sleep mode).
1	Attribute autosave after event capability The device supports the S.M.A.R.T. Enable/Disable Attribute Autosave subcommand.
2-15	Reserved (0)

12.30.2.9 Data Structure Checksum

The Data Structure Checksum is the 2's compliment of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

12.30.3 Device Attribute Thresholds Data Structure

The following defines the 512 bytes that make up the Attribute Threshold information. This data structure is accessed by the host in its entirety using the SMART Read Attribute Thresholds. All multi-byte fields shown in these data structures follow the ATA-3 specification for byte ordering, namely that the least significant byte occupies the lowest numbered byte address location in the field.

The sequence of active Attribute Thresholds will appear in the same order as their corresponding Attribute Values.

Description	Bytes	Offset	Format	Value
Data Structure Revision Number	2	00h	binary	0005h
1st Attribute Threshold	12	02h	(*1)	(*2)
...	..			
...	..			
30th Attribute Threshold	12	15Eh	(*1)	(*2)
Reserved	18	16Ah		(*3)
Vendor specific	131	17Ch		(*3)
Data structure checksum	1	1FFh		(*2)
	512			

- (*1) – See following definitions
- (*2) – Value varied by actual operating condition
- (*3) – Filled with 00h

Figure 98. Device Attribute Thresholds Data Structure

12.30.3.1 Data Structure Revision Number

This value (0005h) is the same as the value used in the Device Attributes Values Data Structure.

12.30.3.2 Individual Thresholds Data Structure

The following defines the 12 bytes that make up the information for each Threshold entry in the Device Attribute Thresholds Data Structure. Attribute entries in the Individual Threshold Data Structure is in the same order and correspond to the entries in the Individual Attribute Data Structure.

Description	Bytes	Offset	Format
Attribute ID Number (01h to FFh)	1	00h	binary
Attribute Threshold (for comparison with Attribute Values from 00h to FFh)	1	01h	binary
00h – "always passing" threshold value to be used for code test purposes			
01h – minimum value for normal operation			
FDh – maximum value for normal operation			
FEh – invalid for threshold value			
FFh – "always failing" threshold value to be used for code test purposes			
Reserved (00h)	10	02h	binary
Total Bytes	12		

Figure 99. Individual Threshold Data Structure

12.30.3.3 Attribute ID Numbers

Attribute ID Numbers supported by the device are the same as Attribute Values Data Structures.

12.30.3.4 Attribute Threshold

These values are preset at the factory and are not meant to be changeable. However, the host might use "SMART Write Attribute Threshold" subcommand to override these preset values in the Threshold sectors.

12.30.3.5 Data Structure Checksum

The Data Structure Checksum is the 2's compliment of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

12.30.4 Error Reporting

The following table shows the values returned in the Status and Error Registers when specific error conditions are encountered by a device.

Error Condition	Status Register	Error Register
A S.M.A.R.T. FUNCTION SET command was received by the device without the required key being loaded into the Cylinder High and Cylinder Low registers.	51h	04h
A S.M.A.R.T. FUNCTION SET command was received by the device with a subcommand value in the Features Register that is either invalid or not supported by this device.	51h	04h
A S.M.A.R.T. FUNCTION SET command subcommand other than SMART ENABLE OPERATIONS was received by the device while the device was in a "S.M.A.R.T. disabled" state.	51h	04h
The device is unable to read its Attribute Values or Attribute Thresholds data structure.	51h	10h or 40h
The device is unable to write to its Attribute Values data structure.	51h	10h or 01h

Figure 100. S.M.A.R.T. Error Codes

12.31 Standby (E2h/96h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	0	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 101. Standby Command (E2h/96h)

The Standby command causes the device to enter the Standby Mode immediately, and set auto power down timeout parameter(standby timer).

When this command is issued, the device confirms the completion of the cached write commands before it asserts INTRQ. Then the device is spun down, but the interface remains active.

If the device is already spun down, the spin down sequence is not executed.

During the Standby mode the device will respond to commands, but there is a delay while waiting for the spindle to reach operating speed.

The timer starts counting down when the device returns to Idle mode.

Output Parameters To The Device

Sector Count Timeout Parameter. If zero, the timeout interval(Standby Timer) is NOT disabled, but the timeout interval is set for 109 minutes automatically. If other than zero, the timeout interval is set for (Timeout Parameter × 5) seconds.

When the automatic power down sequence is enabled,

The device will enter Standby mode automatically if the timeout interval expires with no device access from the host. The timeout interval will be reinitialized if there is a device access before the timeout interval expires.

12.32 Standby Immediate (E0h/94h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 102. Standby Immediate Command (E0h/94h)

The Standby Immediate command causes the device to enter Standby mode immediately.

When this command is issued, the device confirms the completion of the cached write commands before asserts INTRQ. Then the device is spun down, but the interface remains active.

If the device is already spun down, the spin down sequence is not executed.

During the Standby mode, the device will respond to commands, but there is a delay while waiting for the spindle to reach operating speed.

The Standby Immediate command will not affect the auto power down timeout parameter.

12.33 Write Buffer (E8h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 103. Write Buffer Command (E8h)

The Write Buffer command transfers a sector of data from the host to the sector buffer of the device. The sectors of data are transferred through the Data Register 16 bits at a time.

The Read Buffer and Write Buffer commands are synchronized such that sequential Write Buffer and Read Buffer commands access the same 512 byte within the buffer.

12.34 Write DMA (CAh/CBh)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	1	0	1	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 104. Write DMA Command (CAh/CBh)

The Write DMA command transfers one or more sectors of data from the host to the device, then the data is written to the disk media.

The sectors of data are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. Data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Output Parameters To The Device

Sector Count The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number The sector number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

- H** The head number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 24 - 27. (L=1)
- R** The retry bit. If set to one, then retries are disabled. When write cache is enabled, they are ignored. (Ignoring the retry bit is in violation of ATA-3.)

Input Parameters From The Device

- Sector Count** The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
- Sector Number** The sector number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
- Cylinder High/Low** The cylinder number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
- H** The head number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

12.35 Write Long (32h/33h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	0	0	0	0	0	0	0	1
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	0	1	1	0	0	1	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 105. Write Long Command (32h/33h)

The Write Long command transfers the data and the ECC bytes of the designated one sector from the host to the device, then the data and the ECC bytes are written to the disk media.

After 512 bytes of data have been transferred, the device will keep setting DRQ=1 to indicate that the device is ready to receive the ECC bytes from the host. The data is transferred 16 bits at a time, and the ECC bytes are transferred 8 bits at a time. The number of ECC bytes are 4 or 28 according to setting of Set Feature option. The default number after power on is 4 bytes.

Output Parameters To The Device

- Sector Count** The number of continuous sectors to be transferred. The Sector Count must be set to one.
- Sector Number** The sector number of the sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 0 - 7. (L=1)
- Cylinder High/Low** The cylinder number of the sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
- H** The head number of the sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 24 - 27. (L=1)
- R** The retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred.
Sector Number	The sector number of the sector to be transferred. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the sector to be transferred. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the sector to be transferred. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

The file internally uses 28 bytes of ECC on all data read or writes. The 4 byte mode of operation is provided via an emulation technique. As a consequence of this emulation it is recommended that 28 byte ECC mode is used for all tests to confirm the operation of the files ECC hardware. Unexpected results may occur if such testing is performed using 4 byte mode.

12.36 Write Multiple (C5h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	0	1	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 106. Write Multiple Command (C5h)

The Write Multiple command transfers one or more sectors from the host to the device, then the data is written to the disk media.

Command execution is identical to the Write Sectors command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector. The sectors are transferred through the Data Register 16 bits at a time.

Output Parameters To The Device

Sector Count The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number The sector number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H The head number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 24 - 27. (L=1)

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

12.37 Write Sectors (30h/31h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	0	1	1	0	0	0	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 107. Write Sectors Command (30h/31h)

The Write Sectors command transfers one or more sectors from the host to the device, then the data is written to the disk media.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the write will be terminated at the failing sector, when the auto reassign function is disable.

Output Parameters To The Device

- Sector Count** The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
- Sector Number** The sector number of the first sector to be transferred. (L=0)
 In LBA mode, this register contains LBA bits 0 - 7. (L=1)
- Cylinder High/Low** The cylinder number of the first sector to be transferred. (L=0)
 In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
- H** The head number of the first sector to be transferred. (L=0)
 In LBA mode, this register contains LBA bits 24 - 27. (L=1)
- R** The retry bit. If set to one, then retries are disabled. But ignored, when write cache is enabled. (Ignoring the retry bit is in violation of ATA-3.)

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

12.38 Write Verify (3Ch: Vendor Specific)

In DPLA-2xxxx implementation, Write Verify command is exactly same as Write Sectors command(30h). No read verification is performed after write operation.

Refer to Write Sectors Command for parameters.

13.0 Timings

The timing of BSY and DRQ in Status Register are shown in Figure 108

FUNCTION	INTERVAL	START	STOP	TIMEOUT
Power On	Device Busy After Power On	Power On	Status Register BSY=1	400 ns
	Device Ready After Power On	Power On	Status Register BSY=0 and RDY=1	31 sec
Software Reset	Device Busy After Software Reset	Device Control Register RST=1	Status Register BSY=1	400 ns
	Device Ready After Software Reset	Device Control Register RST=1	Status Register BSY=0 and RDY=1	6 sec
Hard Reset	Device Busy After Hard Reset	Bus RESET Signal Asserted	Status Register BSY=1	400 ns
	Device Ready After Hard Reset	Bus RESET Signal Asserted	Status Register BSY=0 and RDY=1	31 sec
Data In Command	Device Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns
	Interrupt, DRQ For Data Transfer In	Status Register BSY=1	Status Register BSY=0 and DRQ=1, Interrupt	30 sec
	Device Busy After Data Transfer In	256th Read From Data Register	Status Register BSY=1	10 us
Data Out Command	Device Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns
	Data Request For Data Transfer Out	Status Register BSY=1	Status Register BSY=0 and DRQ=1	700 us (Note.3)
	Device Busy After Data Transfer Out	256th Write From Data Register	Status Register BSY=1	5 us
	Interrupt For Data Transfer Out	Status Register BSY=1	Status Register BSY=0 and RDY=1 Interrupt	30 sec (Note.1)
Non-Data Command	Device Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns
	Interrupt For Command Complete	Status Register BSY=1	Interrupt	30 sec (Note.2)

Figure 108. Timeout Values

FUNCTION	INTERVAL	START	STOP	TIMEOUT
DMA Data Transfer Command	Device Busy after Command Code Out	Out to Command Register	Status Register BSY=1	400 ns

Figure 109. Timeout Values --- Continued ---

Command category is referred to 11.0, “Command Protocol” on page 89.

The abbreviations "ns", "us", "ms" and "sec" mean nanoseconds, microseconds, milliseconds and seconds, respectively.

We recommend that the host system executes Soft reset and then retry to issue the command if the host system timeout would occur for the device.

(Note.1) For SECURITY ERASE UNIT command, the timeout value is 16 minutes.

(Note.2) For FORMAT UNIT command, the timeout value is 16 minutes.

(Note.3) When the initial power mode at power on is Standby mode, and when the following commands are issued by the host as First Command, the command's timeout value of the field is 10 seconds.

Security Disable Password, Security Erase Unit,

Security Set Password, Security Unlock.

14.0 Appendix

14.1 Commands Support Coverage

Following table is provided to facilitate the understanding of DPLA-2xxxx command support coverage comparing to the ATA-3 defined command set. The column of 'Implementation' shows the capability of DPLA-2xxxx for those commands.

Command Code	Command Name		Implementation for DPLA-2xxxx	ATA-3 Category
00h	NOP		No	Optional
01h-0Fh	Reserved		Reserved	Reserved
1xh	RECALIBRATE		Yes	Optional
20h	READ SECTOR(S)	(w/ retry)	Yes	Mandatory
21h	READ SECTOR(S)	(w/o retry)	Yes	Mandatory
22h	READ LONG	(w/ retry)	Yes	Optional
23h	READ LONG	(w/o retry)	Yes	Optional
24h-2Fh	Reserved		Reserved	Reserved
30h	WRITE SECTOR(S)	(w/ retry)	Yes	Mandatory
31h	WRITE SECTOR(S)	(w/o retry)	Yes	Mandatory
32h	WRITE LONG	(w/ retry)	Yes	Optional
33h	WRITE LONG	(w/o retry)	Yes	Optional
34h-3Bh	Reserved		Reserved	Reserved
3Ch	WRITE VERIFY (2)		Vendor specific	Optional
3Dh-3Fh	Reserved		Reserved	Reserved
40h	READ VERIFY SECTOR(S)	(w/ retry)	Yes	Mandatory
41h	READ VERIFY SECTOR(S)	(w/o retry)	Yes	Mandatory
42h-4Fh	Reserved		Reserved	Reserved
50h	FORMAT TRACK		Yes	Vendor specific
51h-5Fh	Reserved		Reserved	Reserved
60h-6Fh	Reserved		Reserved	Reserved
7xh	SEEK		Yes	Mandatory
8xh	Vendor specific		Reserved	Vendor specific
90h	EXECUTE DEVICE DIAGNOSTIC		Yes	Mandatory
91h	INITIALIZE DEVICE PARAMETERS		Yes	Mandatory
92h	DOWNLOAD MICROCODE		No	Optional
93h	Reserved		Reserved	Reserved
94h,E0h	STANDBY IMMEDIATE (1)		Yes	Optional (4)
95h,E1h	IDLE IMMEDIATE (1)		Yes	Optional (4)
96h,E2h	STANDBY (1)		Yes	Optional (4)
97h,E3h	IDLE (1)		Yes	Optional (4)
98h,E5h	CHECK POWER MODE (1)		Yes	Optional (4)
99h,E6h	SLEEP (1)		Yes	Optional (4)
9Ah	Vendor specific		Reserved	Vendor specific
9Bh-9Fh	Reserved		Reserved	Reserved
A0h-AFh	Reserved		Reserved	Reserved

Figure 110. Command coverage

Command Code	Command Name	Implementation for DPLA-2xxxx	ATA-3 Category
B0h	SMART FUNCTION SET	Yes	Optional - (5)
B1h-BFh	Reserved	Reserved	Reserved
C0h-C3h	Vendor specific	Reserved	Vendor specific
C4h	READ MULTIPLE	Yes	Optional
C5h	WRITE MULTIPLE	Yes	Optional
C6h	SET MULTIPLE MODE	Yes	Optional
C7h	Reserved	Reserved	Reserved
C8h	READ DMA (w/ retry)	Yes	Optional
C9h	READ DMA (w/o retry)	Yes	Optional
CAh	WRITE DMA (w/ retry)	Yes	Optional
CBh	WRITE DMA (w/o retry)	Yes	Optional
CCh-CFh	Reserved	Reserved	Reserved
D0h-DAh	Reserved	Reserved	Reserved
DBh	ACKNOWLEDGE MEDIA CHANGE	No	Optional - (7)
DCh	BOOT - POST-BOOT	No	Optional - (7)
DDh	BOOT - PRE-BOOT	No	Optional - (7)
DEh	DOOR LOCK	No	Optional - (7)
DFh	DOOR UNLOCK	No	Optional - (7)
E0h,94h	STANDBY IMMEDIATE (1)	Yes	Optional - (4)
E1h,95h	IDLE IMMEDIATE (1)	Yes	Optional - (4)
E2h,96h	STANDBY (1)	Yes	Optional - (4)
E3h,97h	IDLE (1)	Yes	Optional - (4)
E4h	READ BUFFER	Yes	Optional
E5h,98h	CHECK POWER MODE (1)	Yes	Optional - (4)
E6h,99h	SLEEP (1)	Yes	Optional - (4)
E7h	FLUSH CACHE	Yes	Optional
E8h	WRITE BUFFER	Yes	Optional
E9h	WRITE SAME	No	Optional
EAh-EBh	Reserved	Reserved	Reserved
ECh	IDENTIFY DEVICE	Yes	Mandatory
EDh	MEDIA EJECT	No	Optional - (7)
EEh	IDENTIFY DEVICE DMA	Yes	Optional
EFh	SET FEATURES	Yes	Optional
F0h	Vendor specific	Reserved	Vendor specific
F1h	SECURITY SET PASSWORD	Yes	Optional - (6)
F2h	SECURITY UNLOCK	Yes	Optional - (6)
F3h	SECURITY ERASE PREPARE	Yes	Optional - (6)
F4h	SECURITY ERASE UNIT	Yes	Optional - (6)
F5h	SECURITY FREEZE LOCK	Yes	Optional - (6)
F6h	SECURITY DISABLE PASSWORD	Yes	Optional - (6)
F7h	FORMAT UNIT	Vendor specific	Vendor specific
F8h	READ NATIVE MAX LBA/CYL (3)	Vendor specific	Vendor specific
F9h	SET MAX LBA/CYL (3)	Vendor specific	Vendor specific
FAh-FFh	Vendor specific	Reserved	Vendor specific

Figure 111. Command coverage --- Continued ---

- Note:(1) These commands have two command codes and appear in this table twice, once for each command code.
- (2) The WRITE VERIFY command implemented vendor specific. The operation is same as WRITE SECTORS and verification is not performed.
 - (3) Vendor specific command F8h and F9h are used for PROTECTED AREA FEATURE.
 - (4) Power Management Feature Set
 - (5) S.M.A.R.T. Function Set
 - (6) Security Mode Feature Set
 - (7) Removable

Figure 112. Command coverage --- Continued ---

14.2 SET FEATURES Command Support Coverage

The following table is provided to facilitate the understanding of DPLA-2xxxx "Set Features" command support coverage comparing to the ATA-3 defined command set. The column of 'Implementation' shows the capability of DPLA-2xxxx for those commands. For detail operation, refer to 12.26, "Set Features (EFh)" on page 138.

Features Register	Features Name	Implementation for DPLA-2xxxx	ATA-3 Category
01h	Enable 8 bit data transfers	No	Optional
02h	Enable write cache	Yes	Vendor specific
03h	Set transfer mode	Yes	Optional
04h	Enable all auto reassignment	No	Vendor specific
05h	Enable Adaptive mode	Yes	Optional
33h	Disable retry	No	Vendor specific
44h	Set vendor specific bytes ECC	Yes	Optional
54h	Set cache segments	No	Vendor specific
55h	Disable read look-ahead feature	Yes	Optional
66h	Disable reverting to power on defaults	Yes	Optional
77h	Disable ECC	No	Vendor specific
81h	Disable 8 bit data transfers	No	Optional
82h	Disable write cache	Yes	Vendor specific
84h	Disable all auto reassignment	No	Vendor specific
85h	Disable Adaptive mode	Yes	Optional
88h	Enable ECC	No	Vendor specific
99h	Enable retries	No	Vendor specific
9Ah	Set device maximum average current	No	Optional
AAh	Enable read look-ahead feature	Yes	Optional
ABh	Set maximum prefetch	No	Vendor specific
BBh	Set 4 bytes ECC	Yes	Optional
CCh	Enable reverting to power on defaults	Yes	Optional
others	Reserved	Reserved	Reserved

Figure 113. SET FEATURES Command coverage

Index

A

- ABRT 65
- ABT 65
- Adaptive Battery Life Extender (ABLE-2) Feature 74
- Adaptive Power Management Feature
 - Active Idle mode 74
 - Low Power Idle mode 74
 - Performance Idle mode 74
 - Transition Time 74
- AMN 65
- AMNF 65
- Auto Reassign Function 87
 - Non recovered read errors 87
 - Non recovered write errors 87
 - Recovered read errors 87
- Automatic Power Down Sequence 157

B

- B 98
- BSY 66

C

- Check Power Mode 92, 99
- Command
 - Check Power Mode (E5h/98h) 99
 - Execute Device Diagnostic (90h) 100
 - Flush Cache (E7h) 101
 - Format Track (50h) 102
 - Format Unit (F7h) 104
 - Identify Device (ECh) 106
 - Identify Device DMA (EEh) 110
 - Idle (E3h/97h) 111
 - Idle Immediate (E1h/95h) 112
 - Initialize Device Parameters (91h) 113
 - Read Buffer (E4h) 114
 - Read DMA (C8h/C9h) 115
 - Read Long (22h/23h) 117
 - Read Multiple (C4h) 119
 - Read Native Max LBA/CYL (F8h) 121
 - Read Sectors (20h/21h) 123
 - Read Verify Sectors (40h/41h) 125
 - Recalibrate (1xh) 127
 - S.M.A.R.T. Function Set (B0h) 144
 - Security Disable Password (F6h) 128
 - Security Erase Prepare (F3h) 129
 - Security Erase Unit (F4h) 130
 - Security Freeze Lock (F5h) 132
 - Security Set Password (F1h) 133
 - Security Unlock (F2h) 135
 - Seek (7xh) 137
 - Set Features (EFh) 138
 - Set Max LBA/CYL (F9h) 140

Command (continued)

- Set Multiple (C6h) 142
 - Sleep (E6h/99h) 143
 - Standby (E2h/96h) 157
 - Standby Immediate (E0h/94h) 158
 - Write Buffer (E8h) 159
 - Write DMA (CAh/CBh) 160
 - Write Long (32h/33h) 162
 - Write Multiple (C5h) 164
 - Write Sectors (30h/31h) 166
 - Write Verify (3Ch) 168
- Commands support Coverage 175
- COR 66
 - CORR 66

D

- D 98
- DF 66
- Diagnostic
 - Diagnostic and Reset considerations 70
- Diagnostic and Reset considerations 70
- Diagnostic Codes 64, 69, 100
- DRDY 66
- DRQ 66
- DRV 64
- DS0 64
- DS1 63
- DSC 66

E

- ERR 66
- Error Register
 - Diagnostic Codes 69
- Example of operation 84
- Execute Device Diagnostic 92, 100

F

- Flush Cache 92, 101
- Format Track 90, 102
- Format Unit 92, 104

H

- H 98
- H0 63
- H1 63
- H2 63
- H3 63
- HS0 64
- HS1 64
- HS2 64

HS3 64

I

ICRCE 65
Identify Device 89, 106
Identify Device DMA 93, 110
Idle 92, 111
Idle Immediate 92, 112
IDN 65
IDNF 65
IDX 66
IEN 63
Initial Power Mode at Power On 73
Initialize Device Parameters 92, 113

L

L 64, 98
LBA Addressing Mode 71
Logical CHS Addressing Mode 71

M

Master 64

P

Power Management Feature 72
 Initial Power Mode at Power On 73
 Interface Capability for Power Modes 73
 Power Management Commands 72
 Power Mode 72
 Standby timer 73
 Standby/Sleep command completion timing 72
 Status 73

R

R 98
RDY 66
Read Buffer 89, 114
Read DMA 93, 115
Read Long 89, 117
Read Multiple 89, 119
Read Native Max LBA/CYL 92, 121
Read Sectors 89, 123
Read Verify Sectors 92, 125
Reassign Function 87
Recalibrate 92, 127
Register
 Alternate Status Register 62
 Command Register 62
 Cylinder High Register 62
 Cylinder Low Register 62
 Data Register 63
 Device Control Register 63
 Device/Head Register 64
 Drive Address Register 63

Register (*continued*)

 Error Register 64
 Features Register 65
 Register Initialization 69
 Sector Count Register 65
 Sector Number Register 65
 Status Register 65
Register Initialization 69
Reset
 Diagnostic and Reset considerations 70
 Register Initialization 69
RST 63

S

S.M.A.R.T. Function 76
 Attribute thresholds 76
 Attribute values 76
 Attributes 76
 S.M.A.R.T. commands 76
 S.M.A.R.T. operation with power management modes 76
 Threshold exceeded condition 76
S.M.A.R.T. Function Set 144
Sector Addressing Mode 71
 LBA Addressing Mode 71
 Logical CHS Addressing Mode 71
Security Disable Password 90, 128
Security Erase Prepare 92, 129
Security Erase Unit 90, 130
Security Freeze Lock 92, 132
Security Mode Feature Set 78
Security Set Password 90, 133
Security Unlock 90, 135
Seek 92, 137
Set Features 92, 138
SET FEATURES Command support Coverage 178
Set Max LBA/CYL 92, 140
Set Multiple 142
Set Multiple Mode 92
Slave 64
Sleep 92, 143
SMART Disable Operations 92
SMART Enable Operations 92
SMART Enable/Disable Attribute Autosave 92
SMART Execute Off-line Immediate 92
SMART Read Attribute Thresholds 89
SMART Read Attribute Values 89
SMART Return Status 92
SMART Save Attribute Values 92
SRST 63
Standby 92, 157
Standby Immediate 92, 158

T

TON 65
Timeout Interval 63, 171

Timeout Parameter 111, 157
TK0NF 65

U

UNC 65

V

V 98

W

Write Buffer 90, 159
Write Cache 86
Write DMA 93, 160
Write Long 90, 162
Write Multiple 90, 164
Write Sectors 90, 166
Write Verify 91, 168
WTG 63

X

x 98



S82H-9141-05