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# **OEM HARD DISK DRIVE SPECIFICATIONS**

**for**

**DPEA-30540/30810/31080 (528/541/812/1083 MB)**

**3.5-Inch Hard Disk Drive with ATA Interface**

**Revision (1.2)**

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# Contents

<b>1.0 General</b>	1
1.1 Introduction	1
1.2 References	1
1.3 Caution	1
1.4 Glossary	1
<b>2.0 Products Outline</b>	3
<b>3.0 Drive Characteristics</b>	5
3.1 Logical Drive Format	5
3.2 Data Sheet	5
3.3 Performance Characteristics	6
3.3.1 Command Overhead	6
3.3.2 Single Track Seek Time	6
3.3.3 Average Seek Time (Including Settling)	6
3.3.4 Full Stroke Seek	8
3.3.5 Average Latency	8
3.3.6 Drive Ready Time	9
<b>4.0 Data integrity</b>	11
4.1 Equipment Status	11
4.2 WRITE Safety	11
4.3 Data Buffer Test	11
4.4 Error Recovery	12
<b>5.0 Physical Format</b>	13
5.1 After Formatting	13
<b>6.0 Specifications</b>	15
6.1 Environment	15
6.1.1 Temperature and Humidity	15
6.2 DC Power Requirements	16
6.3 Reliability	17
6.3.1 Mean Time To Failures (MTTF)	17
6.3.2 Product Life and Usage	17
6.4 Contact Start Stop (CSS)	17
6.5 Warranty	17
6.6 Preventive Maintenance	17
6.7 Error rate	17
6.8 Mechanical Specifications	18
6.8.1 Outline	18
6.8.2 Mechanical Dimensions	18
6.8.3 Mounting Positions and the Tappings	20
6.8.4 Connector Dimension	21
6.8.5 Connector and Jumper	22
6.8.6 Mounting Orientation	24
6.8.7 Landing Zone and Lock	24
6.9 Vibration and Shock	25
6.9.1 Operating Vibration	25
6.9.2 Non-Operating Vibrations	25
6.9.3 Operating Shock	26

6.9.4 Non-Operating Shock	26
6.10 Acoustics	27
6.10.1 Sound Power Levels	27
6.10.2 Sound Power Acceptance Criteria	27
6.11 Identification Labels	28
6.12 Electromagnetic Compatibility	28
6.13 Safety	29
6.13.1 Underwriters Lab (UL) Approval	29
6.13.2 Canadian Standards Authority (CSA) Approval	29
6.13.3 IEC Compliance	29
6.13.4 German Safety Mark	29
6.13.5 Flammability	29
6.13.6 Safe Handling	29
6.13.7 Environment	30
6.13.8 Secondary Circuit Protection	30
6.14 Packaging	30
6.15 Electrical Interface Specifications	30
6.15.1 Power Connectors	30
6.15.2 Cabling	31
6.15.3 Interface Connector	31
6.15.4 Signal Definition	31
<b>6.0 Interface Specification</b>	<b>41</b>
6.1 Conformance	41
<b>7.0 Registers</b>	<b>45</b>
7.1 Alternate Status Register	45
7.2 Command Register	46
7.3 Cylinder High Register	46
7.4 Cylinder Low Register	46
7.5 Data Register	46
7.6 Device Control Register	46
7.7 Drive Address Register	47
7.8 Drive/Head Register	47
7.9 Error Register	48
7.10 Features Register	48
7.11 Sector Count Register	49
7.12 Sector Number Register	49
7.13 Status Register	49
<b>8.0 Command Protocol</b>	<b>51</b>
8.1 PIO Data In Commands	51
8.2 PIO Data Out Commands	52
8.3 Non-Data Commands	53
8.4 DMA Data Transfer Commands	54
<b>9.0 Command Descriptions</b>	<b>57</b>
9.1 Check Power Mode	59
9.2 Execute Drive Diagnostics	60
9.3 Format Track	61
9.4 Identify Drive	62
9.5 Idle	66
9.6 Idle Immediate	67
9.7 Initialize Drive Parameters	68
9.8 Read Buffer	69

9.9 Read DMA	70
9.10 Read Long	72
9.11 Read Multiple	74
9.12 Read Sectors	75
9.13 Read Verify Sectors	76
9.14 Recalibrate	77
9.15 Seek	78
9.16 Set Features	79
9.17 Set Multiple	81
9.18 Sleep	82
9.19 Standby	83
9.20 Standby Immediate	84
9.21 Write Buffer	85
9.22 Write DMA	86
9.23 Write Long	88
9.24 Write Multiple	90
9.25 Write Sectors	91
<b>10.0 Reset</b>	<b>95</b>
10.1 Power On Reset	95
10.2 Hard Reset	95
10.3 Software Reset	95
10.4 Register Initialization	95
<b>11.0 Timings</b>	<b>99</b>
<b>Appendix A. Cache</b>	<b>101</b>
A.1 Read Look-Ahead	101
A.2 Write Cache	101
<b>Appendix B. Index</b>	<b>103</b>



# Figures

1.	Drive Parameter	5
2.	Data Sheet	5
3.	Performance Parameter	6
4.	Single Track Seek Time	6
5.	Mechanical Positioning Performance	7
6.	Full Stroke Seek Time	8
7.	Latency Time	8
8.	Drive Ready Time	9
9.	Operating Modes	9
10.	Mode Transition Time	10
11.	DC Power Requirement	16
12.	Outline of DPEA-3xxxx	18
13.	Physical Dimension	18
14.	Mechanical Dimension	19
15.	Mounting Positions and the Tappings	20
16.	Connector Dimension	21
17.	Connector and Jumper Location	22
18.	Jumper Pins	23
19.	Default Jumper Setting	24
20.	Random Vibration PSD Profile Breakpoints (Operating)	25
21.	Random Vibration PSD Profile Breakpoints (Non-Operating)	25
22.	A-weighted Sound Power Levels	27
23.	Power Connector Pin Assignments	31
24.	Alternate Power Connector Pin Assignments	31
25.	Table of Signals	32
26.	Logic Signal Levels	34
27.	System Reset timing	35
28.	PIO cycle timings	36
29.	DMA (Single Word) cycle timings	37
30.	DMA (Multi Word) cycle timings	38
31.	Task File	39
32.	Relations Among Write Cache/Auto Reallocation Jumpers And Write Cache	42
33.	Register Set	45
34.	Alternate Status Register	45
35.	Device Control Register	46
36.	Drive Address Register	47
37.	Drive/Head Register	47
38.	Error Register	48
39.	Status Register	49
40.	Command Set	57
41.	Check Power Mode Command (E5h)	59
42.	Execute Drive Diagnostics Command (90h)	60
43.	Format Track Command (50h)	61
44.	Identify Drive Command (ECh)	62
45.	Identify Drive Information	63
46.	Idle Command (E3h)	66
47.	Idle Immediate Command (E1h)	67
48.	Initialize Drive Parameters Command (91h)	68
49.	Read Buffer Command (E4h)	69
50.	Read DMA Command (C8h/C9h)	70
51.	Read Long Command (22h/23h)	72

52.	Read Multiple Command (C4h)	74
53.	Read Sectors Command (20h/21h)	75
54.	Read Verify Sectors Command (40h/41h)	76
55.	Recalibrate Command (1xh)	77
56.	Seek Command (7xh)	78
57.	Set Features Command (EFh)	79
58.	Set Feature Parameters	79
59.	Set Multiple Command (C6h)	81
60.	Sleep Command (E6h)	82
61.	Standby Command (E2h)	83
62.	Standby Immediate Command (E0h)	84
63.	Write Buffer Command (E8h)	85
64.	Write DMA Command (CAh/CBh)	86
65.	Write Long Command (32h/33h)	88
66.	Write Multiple Command (C5h)	90
67.	Write Sectors Command (30h/31h)	91
68.	Default Register Values	96
69.	Diagnostic Codes	96
70.	Timeout Values	99

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# 1.0 General

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## 1.1 Introduction

This document describes the characteristics of the following IBM 3.5-inch, ATA interface Hard Disk Drives:

- DPEA-30540 (528/541 MB)
- DPEA-30810 (812 MB)
- DPEA-31080 (1083 MB)

This document defines the functional and interface specifications for 3.5" Hard Disk Drives of DPEA-3xxxx series .

---

## 1.2 References

.ISO/IEC Draft. ANSI X3.221 (Information Technology AT Attachment I nterface for Disk Drive)

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## 1.3 Caution

The drive can be easily damaged by shocks or ESD (Electric Static Discharge), so any damages applied to the drive after taking out from shipping package and opening ESD protective bag are user's responsibilities.

---

## 1.4 Glossary

<i>Word</i>	<i>Meaning</i>
<b>Kbpi</b>	1000 Bit Per Inch
<b>Mbps</b>	1000 000 Bit per second
<b>MB</b>	1000 000 bytes
<b>KB</b>	1000 bytes
<b>448 KB</b>	448 X 1024 bytes
<b>Mb/sq.in</b>	1000 000 bits per square inch
<b>MLC</b>	Machine Level Control



---

## 2.0 Products Outline

- 3.5-inch form factor
- No-ID technology
- Data capacity 528MB/541MB/812MB/1083 MB
- 512 bytes/sector
- ATA-2 interface
- Closed Loop actuator servo
- Dedicated head landing zone
- Automatic actuator lock
- Interleave factor 1:1
- 448 KB Sector Buffer
  - Adaptive segment buffer implementation
- Read ahead of LRU cache algorithm
- Write Cache
- Enhanced ECC implementation
  - 128-bit Read Solomon Code operating 10-bit symbol
  - On-The-Fly correction (up to 4 symbols of errors in sector)
- Automatic Error Recovery Procedures for Read and Write
- Self Diagnostics during Power On and resident diagnostics
- PIO Data Transfer - Mode 3 ( Max 11.1 MB/s)
- DMA Data Transfer
  - Single Word mode : mode 2 ( Max 13.3 MB/s)
  - Multiword mode : mode 1 ( Max 11.1 MB/s)
- CHS and LBA mode
- Transparent defect management by Automatic Defect Reallocation during Write Cache
- Power saving modes
- MR (Magneto Resistive) Head technology
- Seek time 10.5ms average (read operation)
- MTTF is 500,000 power on hours



## 3.0 Drive Characteristics

This chapter provides numbers of logical cylinder/head/sector and capacity of the drive. For model name DPEA-30540, a jumper can set the drive to 541MB or 528MB.

### 3.1 Logical Drive Format

The customer usable data capacity is shown below.

Figure 1. Drive Parameter				
Descriptions	DPEA-30540 (CLIPPED)	DPEA-30540	DPEA-30810	DPEA-31080
Logical Head Number	16	16	16	16
Logical Sectors/Track	63	63	63	63
Logical Cylinder Number	1024	1050	1574	2100
Logical Sector Size	512	512	512	512
Sector number for default CHS	1,032,192	1,058,400	1,586,592	2,116,800
Sector number for LBA	1,058,496	1,058,496	1,586,664	2,116,992
Usable Bytes for default CHS	528 MB	541 MB	812 MB	1083 MB
Usable Bytes for LBA	541 MB	541 MB	812 MB	1083 MB

### 3.2 Data Sheet

Figure 2. Data Sheet	
Media transfer rate [Mb/sec]	39.8 - 55.1
Interface transfer rate [MB/sec]	11.1MB Max(PIO) 11.1 MB (DMA)
Data buffer size [KB]	448
Rotational speed [RPM]	5400
Recording density [Kbpi]	68.0(Ave) / 85.6(Max)
Track density [TPI]	5340
Areal density [Mb/sq.in.]	358(Ave) / 457(Max)
Number of zone	8
Number of disks	
DPEA-30540	1
DPEA-30810	2
DPEA-31080	2
Servo design method	Embedded sector servo

## 3.3 Performance Characteristics

The drive performance is characterized by the following parameters:

- Command Overhead
- Mechanical Positioning
  - Seek Time
  - Latency
- Data Transfer Speed
- Buffering Operation

**Note:** The following specification defines the drive characteristics, not the system throughput which is dependant on the system and the application.

Function	Typical
Command overhead	(Read-Cache not hit) < 0.9 [msec] (Read-Cache hit) < 0.3 [msec] (Write) < 0.3 [msec] (Seek) < 0.3 [msec]
Seek time: Read	10.5 [msec]
Seek time: Write	12.5 [msec]
Rotational speed	5400 [rpm]

### 3.3.1 Command Overhead

Command overhead is defined as the time required:

- from the command is written into command register by a host
- to the assertion of DRQ for the first data byte of a READ command when the requested data is not in the buffer
- exclude
  - Physical seek time
  - Latency time

### 3.3.2 Single Track Seek Time

Function	Typical	Max.
Read [msec]	2.3	2.7
Write [msec]	3.2	4.1

The single track seek time is the average of the 1000 single track seeks.

### 3.3.3 Average Seek Time (Including Settling)

Figure 5. Mechanical Positioning Performance		
Command Type	Typical	Max
Read	10.5 [msec]	11.5 [msec]
Write	12.5 [msec]	13.5 [msec]

The seek time is measured from the start of actuator's motion to the start of **a reliable read or write operation**. Reliable read or write implies that error correction/recovery is not used to correct for arrival problems. The average seek time is measured as the weighted average of all possible seek combinations.

$$\text{Weighted Average} = \frac{\sum_{n=1}^{\text{max}} (\text{max} + 1 - n) (T_{n.in} + T_{n.out})}{(\text{max} + 1) (\text{max})}$$

Where:

max = Maximum seek length

n = Seek length (1 to max)

Tn.in = Inward measured seek time for an n track seek

Tn.out = Outward measured seek time for an n track seek

### 3.3.4 Full Stroke Seek

Figure 6. Full Stroke Seek Time		
Function	Typical	Max.
Read [msec]	22	25
Write [msec]	24	27

Full stroke seek is measured as the average of 1000 full stroke seeks.

### 3.3.5 Average Latency

Figure 7. Latency Time		
Rotation	Time for a revolution	Average Latency
5400 [RPM]	11.1 [msec]	5.56 [msec]

### 3.3.6 Drive Ready Time

Figure 8. Drive Ready Time		
Condition	Typical (Model)	Max.
Power On to Ready [sec]	10 (DPEA-30540) 12 (DPEA-30810,DPEA-31080)	31

**Ready** The condition in which the drive is able to perform a media access command (read, write) immediately.

**Power On** This includes the time required for the internal self diagnostics.

#### 3.3.6.1 Operating Modes

Figure 9. Operating Modes	
Operating Mode	Description
Spin-Up	Start up time from spindle-stop or power-down.
Seek	Seek operation mode
Write	Write operation mode
Read	Read operation mode
Idle	Spindle motor and servo system are working normally. Other modules except the servo control and the host interface are sleeping. Commands can be received and processed immediately.
Standby	Spindle motor is stopped. All modules except the host interface are sleeping. Commands can be received immediately. Drive is in an interrupt waiting mode with the lowest power dissipation.

**Notes:**

1. After power-down or spindle-stop, a head locking mechanism secures the heads in the landing zone.

### 3.3.6.2 Mode Transition Time

Figure 10. Mode Transition Time			
From	To	Typical [sec]	Max [sec]
Standby	Idle	8 (DPEA-3540) 10 (DPEA-3810/31080)	31
Idle	Standby	Immediately*	Immediately*

\* : Immediately - The actual spin down time exists, however the command is processed immediately.

---

## 4.0 Data integrity

No more than one sector is lost by hard reset or power down during write operation while write cache is disabled.

In case of that hard reset or power down occurs before completion of data transfer from write cache to disk while write cache is enabled, the data remaining in write cache is lost. To prevent customer data lost at power off, the last write access before power off is recommended to be issued after setting write cache disable by command.

It is possible to check if the data in the write cache have been written onto the disk by successful completion of Soft Reset or the following commands.

Check Power Mode, Execute Drive Diagnostics, Format Track, Identify Drive, Idle, Idle Immediate, Initialize Drive Parameters, Read Buffer, Read Long with Retry, Read Long without Retry, Recalibrate, Seek, Set Features, Set Multiple, Sleep, Standby, Standby Immediate, Write Buffer, Write Long with retry, Write Long without Retry.

---

## 4.1 Equipment Status

Equipment status is available to the host system any time, the drive is not ready to read, write, or seek. This status normally exists at power-on time and be maintained until the following conditions are satisfied.

- Access recalibration/tuning is complete.
- Spindle speed meets requirements for reliable operation.
- Self-check of drive is complete.

Appropriate error status is available to the host system if any of the following condition occur after the drive has once become ready:

- Spindle speed goes out of requirements for reliable operation.
- “Write fault” is detected.

---

## 4.2 WRITE Safety

The verification of write operation involves a read-back check of the CRC or ECC in conjunction with **write fault** detection circuits. The **write fault** detection circuits reveal conditions where write operation was intended and did not occur properly and the CRC or ECC verification occurred for old information, or cases where data is erroneously erased.

---

## 4.3 Data Buffer Test

The data buffers, a read buffer and a write buffer used as temporally data storages for read/write data transfer, are tested at a power-on-reset and when a drive self-test is requested by the host. The tests consist of write/read hex ‘00’ and hex ‘FF’ pattern for all bit position of the buffers.

---

## 4.4 Error Recovery

Errors occurring with the drive are handled by the error recovery procedure.

Errors that are uncorrectable after application of the error recovery procedures are reported to the host system as non-recoverable errors.

## 5.0 Physical Format

On manufacturing process, all sectors of hard disk drive are tested for the magnetical performance, so that only acceptable sectors are used.

In data area, accepted sectors are numbered sequentially for user data sectors.

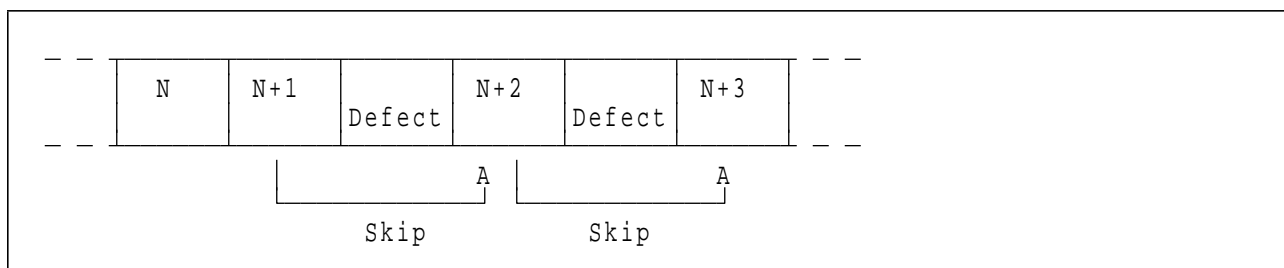
This mapping information is maintained at firmware level, and data block addressed by logical cylinder, head and sector is translated into physical location on disk(s) automatically. This operation is invisible from application level.

Low level format is **NOT ALLOWED** after normal manufacturing process passed.

---

### 5.1 After Formatting

- Data areas are optimally used after the drive is formatted in factory.
- A spare sector is located on each track spread on the user data area.



Defects are skipped without any constraint, such as track or cylinder boundary.



## 6.0 Specifications

This chapter provides the specifications of the drives.

### 6.1 Environment

The following table shows the environmental conditions.

#### 6.1.1 Temperature and Humidity

Operating Conditions	
Temperature	5 to 55[°C] (See note)
Relative Humidity	8 to 90 [% RH] non-condensing
Maximum Wet Bulb Temperature	29.4[°C] non-condensing
Maximum Temperature Gradient	15[°C / Hour]
Altitude	- 300 to 3000 [m]
Non-Operating Conditions(Shipping)	
Temperature	- 40 to 65[°C]
Relative Humidity	5 to 95 [% RH] non-condensing
Maximum Wet Bulb Temperature	35[°C] non-condensing
Maximum Temperature Gradient	15[°C / Hour]
Altitude	- 300 to 12,000 [m]
<b>Note:</b> The system has to provide sufficient ventilation to maintain a surface temperature below [60°C] at the center of the top cover of the drive.	

## 6.2 DC Power Requirements

Figure 11. DC Power Requirement		
Power	Requirement	Note
Nominal supply	+ 5 [V]    + 12 [V]	
Power supply ripple [mV](0– 10[MHz]P-P)	100 max    150 max	1
Tolerance	± 5 %    + 10 % , – 8 %	2
Supply Current (Populated Mean)	[A RMS]	
Idle (average)	0.26    0.12 / 0.16	3
Read / write (average)	0.62    0.24 / 0.28	
Seek (average)	0.46    0.34 / 0.37	
Standby	0.22    0.02	
Start up (peak)	0.64    1.20	

**Notes:**

1. The maximum ripple is measured at input of the drive.
2. The drive does not incur damage by an over-voltage condition of + 25% and the maximum duration of 20 [msec].
3. 0.12/0.16, 0.24/0.28 and 0.34/0.37 show that 0.12, 0.24 and 0.34 are applied for DPEA-30540 and 0.16, 0.28 and 0.37 are for DPEA-30810 and DPEA-31080.

---

## 6.3 Reliability

### 6.3.1 Mean Time To Failures (MTTF)

500,000 power-on hours (POH).

### 6.3.2 Product Life and Usage

The product life of the drive is 5 years.

The drive withstands 4000 POH (power on hour) per year. Drive access (seek, read,write) ratio is 20% of total power on time.

Note : The drive enters the standby mode or power off mode, at least once a day. The environment temperature is lower than 40 deg.C.

---

## 6.4 Contact Start Stop (CSS)

The drive meets the specified error rates after the following start/stop or power on/off cycles in the environment.

- 40,000 cycles under the temperature of 40°C

---

## 6.5 Warranty

The warranty will be covered by contracts.

---

## 6.6 Preventive Maintenance

Not Required.

---

## 6.7 Error rate

- Probability of not recovering data ..... 1 in  $10^{13}$  bits read
- ECC implementation  
128-bit Non-interleave Reed Solomon Code operating 10-bit symbol is used to cover the data fields.  
On-The-Fly correction covers up to four symbols of error in one sector.

## 6.8 Mechanical Specifications

### 6.8.1 Outline

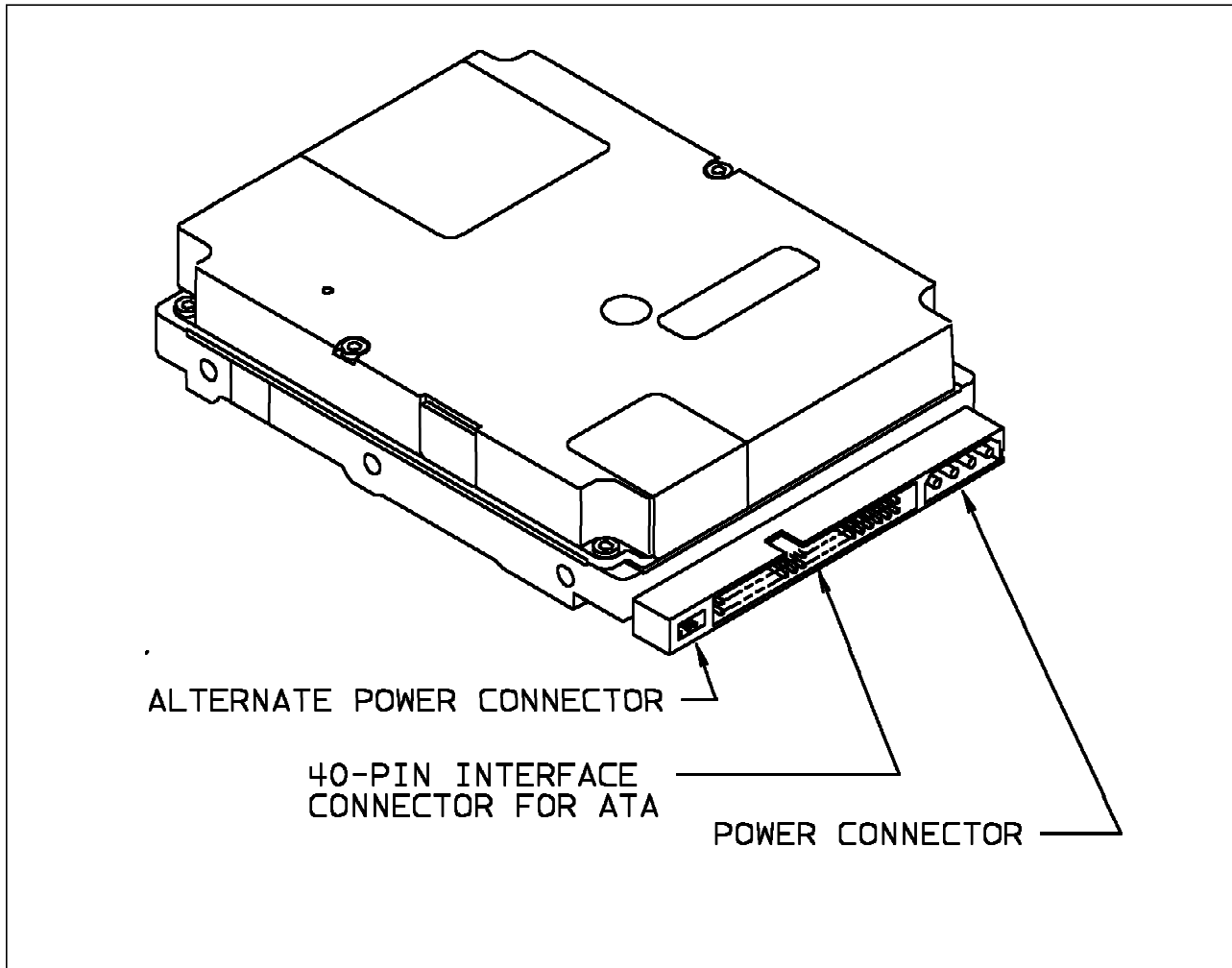


Figure 12. Outline of DPEA-3xxxx

### 6.8.2 Mechanical Dimensions

The following chart describes the dimensions for the 3.5-inch hard disk drive form factor by model.

Figure 13. Physical Dimension	
Height [mm]	25.4 ± 0.4
Width [mm]	101.6 ± 0.4
Length [mm]	146.0 ± 0.6
Weight [gram]	530 Max.

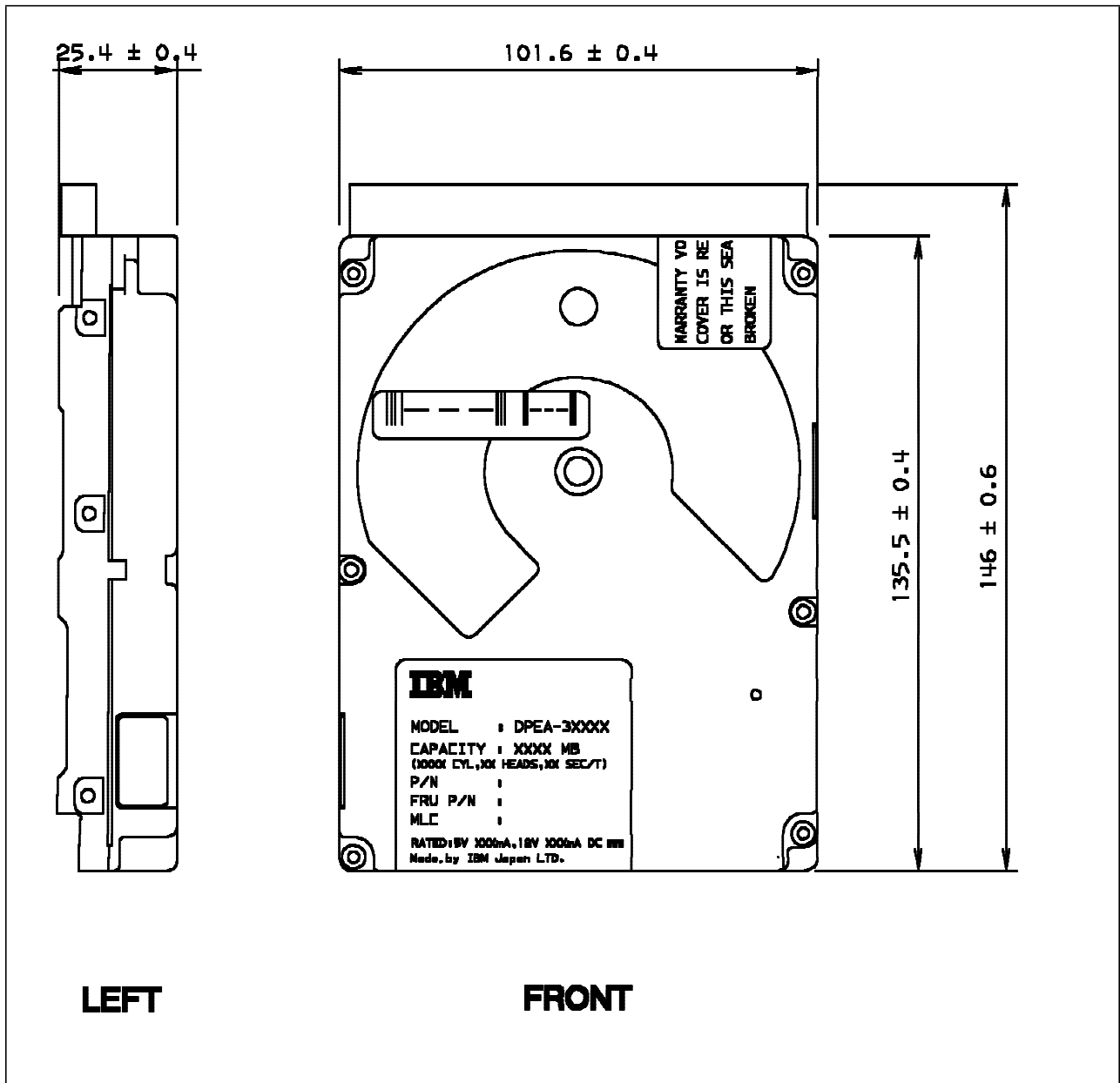


Figure 14. Mechanical Dimension

### 6.8.3 Mounting Positions and the Tappings

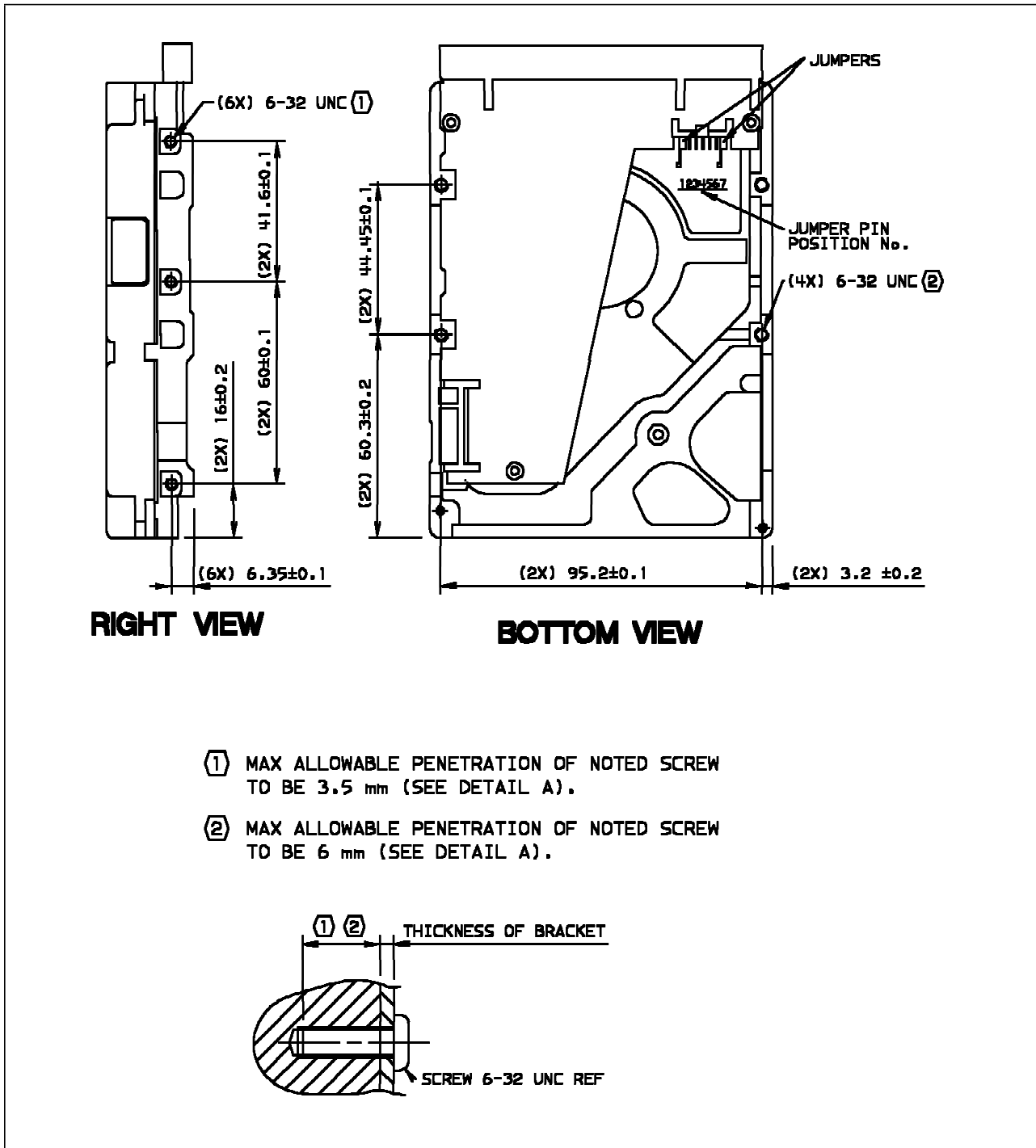


Figure 15. Mounting Positions and the Tappings

6.8.4 Connector Dimension

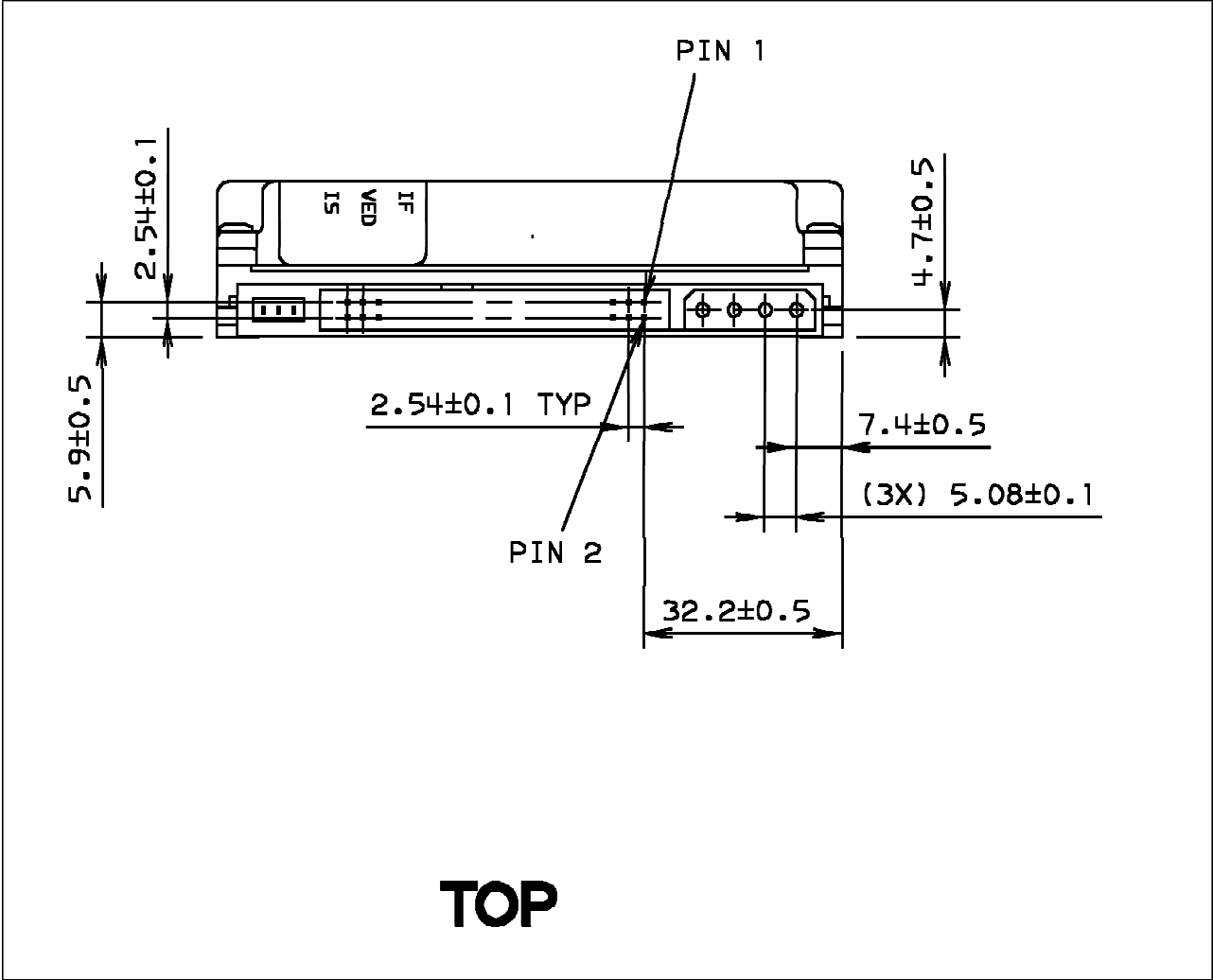


Figure 16. Connector Dimension

## 6.8.5 Connector and Jumper

Jumpers are used for drive address setting, write cache disabling and auto re-allocation disabling.

### 6.8.5.1 Connector and Jumper Location

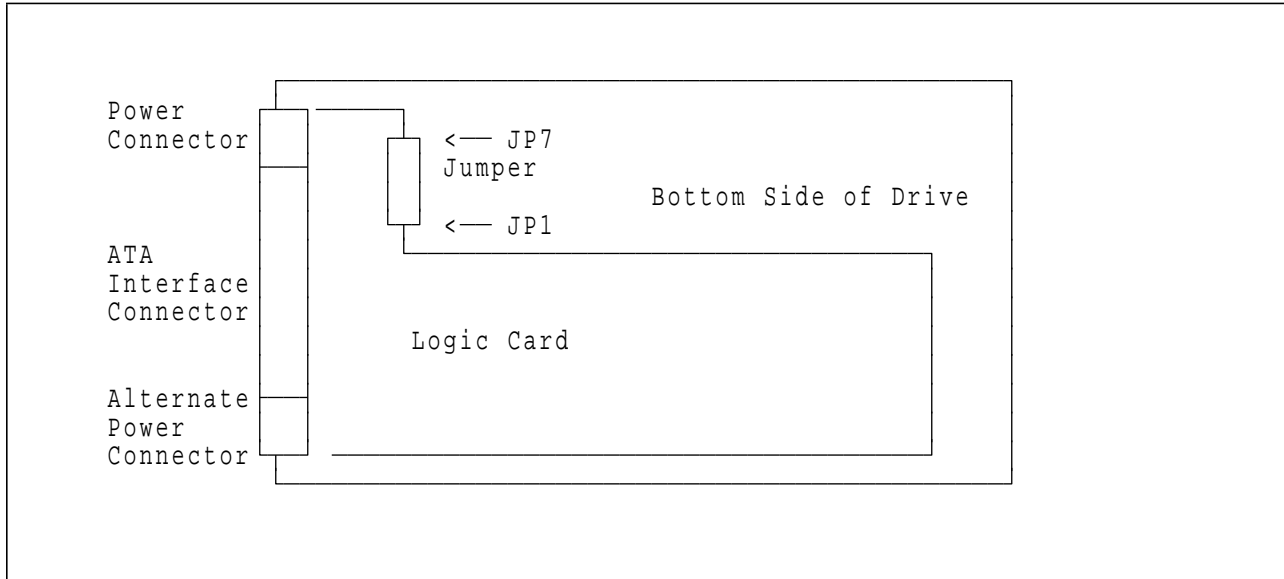


Figure 17. Connector and Jumper Location

## 6.8.5.2 Jumper Setting

Jumper position and the function are as shown below. Pin pitch is 2mm.

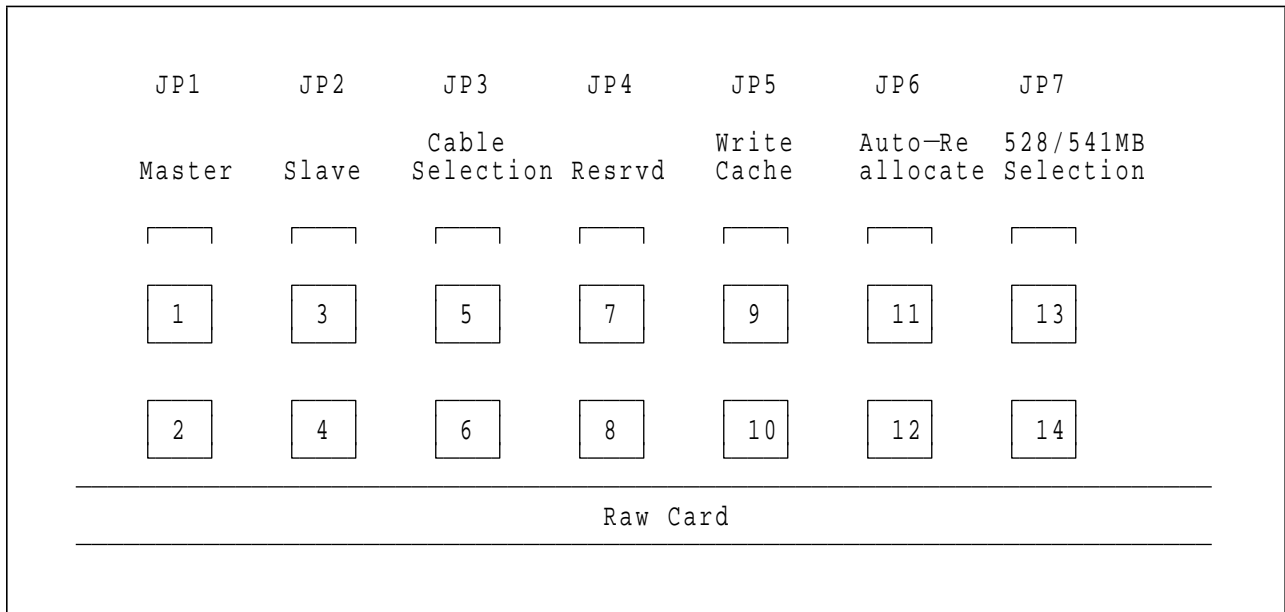


Figure 18. Jumper Pins

### Notes:

1. Jumpers for JP1, 2, and 3 should not be selected concurrently.
2. JP1 is a position for Master, and JP2 is for Slave and JP3 is for Cable selection mode.
3. To enable Cable Selection mode, the JP3 jumper must be installed. In the Cable Selection mode, the drive address is determined as follows:
  - When CSEL signal (pin 28) is grounded or at a low level, the drive address is 0 (master).
  - When CSEL signal is open or at a high level, the drive address is 1 (slave).
4. Position JP4 is not used.
5. A jumper for JP5 is used to disable write-cache.
6. A jumper for JP6 is used to disable write-cache and auto-reallocation.
7. A jumper for JP7 has a meaning when the model name is DPEA-30540. A jumper for JP7 is used to select 541MB i.e. when the jumper is removed, DPEA-30540 is set to 528 MB. This jumper has no meaning for DPEA-30810 and DPEA-31080.

### 6.8.5.3 Default Setting

The default jumper setting at shipment is as follows.

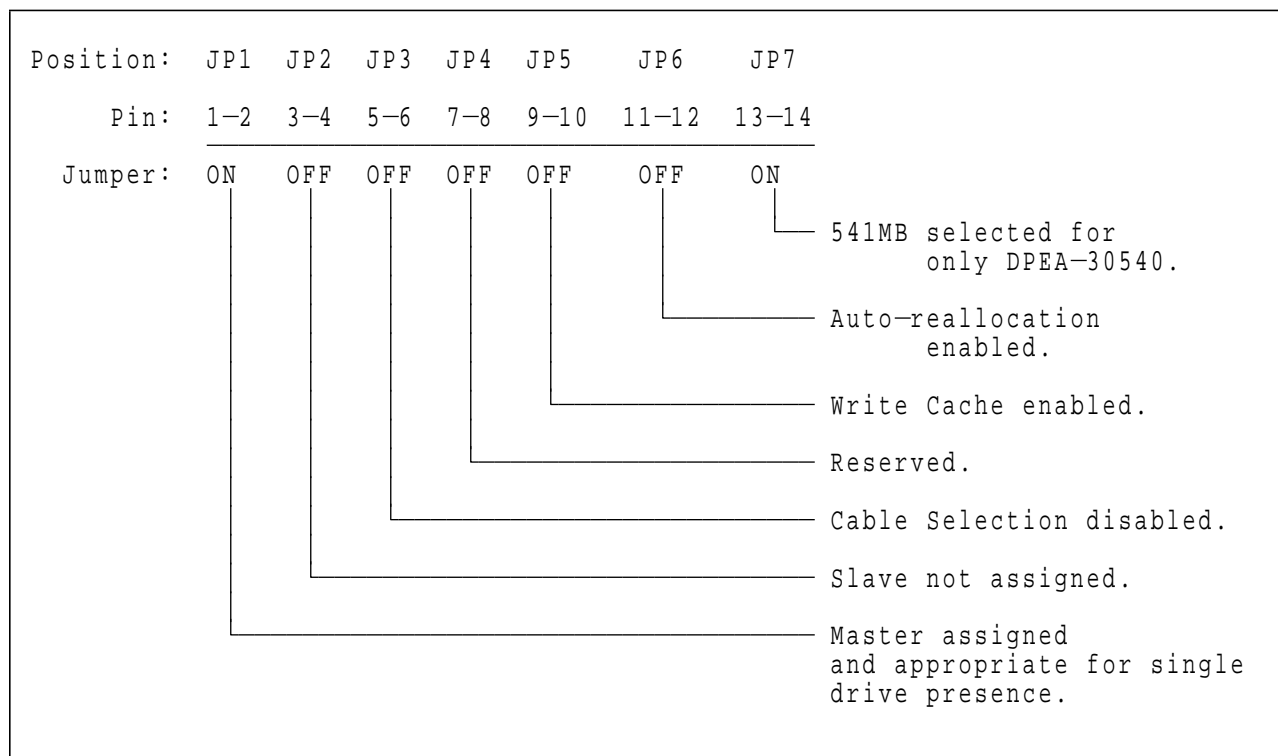


Figure 19. Default Jumper Setting

### 6.8.6 Mounting Orientation

The drive operates in all axes (6 directions). The drive operates within the specified error rates when tilted  $\pm 5$  degrees from these positions.

Performance and error rate stay within specification limits even if the drive is operated in other orientations from which it was formatted. Thus a drive formatted in the horizontal orientation operates in the vertical position without any degradation, and vice versa.

The recommended mounting screw torque is  $3 \pm 0.5$  [Kgf.cm] The recommended mounting screw depth is  $3.5 \pm 0.5$  [mm] for bottom and  $5.0 \pm 0.5$  [mm] for horizontal mounting.

The system is responsible for mounting the drive securely enough to prevent excessive motion or vibration of the drive at seek operation or spindle rotation, using appropriate screws or equivalent mounting hardware. Consult the issuer of this specification for actual application.

The vibration test and the shock test are to be conducted with the drive mounted to the table using four bottom screws.

### 6.8.7 Landing Zone and Lock

A landing zone on the disk, not the data area of the disk, is provided to protect the disk data during shipping, movement, or storage. After power down, a head locking mechanism secures the heads in this zone.

---

## 6.9 Vibration and Shock

All vibration and shock measurements in this section are made with the drive that has no mounting attachments for the systems. The input power for the measurements is applied to the normal drive mounting points.

### 6.9.1 Operating Vibration

The drive operates with no non-recoverable errors while being subjected to the following vibration levels.

The measurements are carried out during 30 minutes of random vibration using the power spectral density (PSD) levels. The vibration test level for V5L is 0.67G (RMS).

Figure 20. Random Vibration PSD Profile Breakpoints (Operating)									
Hz	Random Vibration PSD Profile Breakpoints (Operating)								
[Hz]	5	17	45	48	62	65	150	200	500
$\times 10^{-3}$ [G <sup>2</sup> /Hz]	0.02	1.1	1.1	8.0	8.0	1.0	1.0	0.5	0.5

**Note:** The specified levels are measured at the mounting points.

### 6.9.2 Non-Operating Vibrations

The drive does not sustain permanent damage or loss of recorded data after being subjected to the environment described below.

#### 6.9.2.1 Random Vibration

The test consists of a random vibration applied in each of three mutually perpendicular axes with the time duration of 10 minutes per axis. The PSD levels for the test simulates the shipping and relocation environment which is shown below.

Figure 21. Random Vibration PSD Profile Breakpoints (Non-Operating)							
Hz	Random Vibration PSD Profile Breakpoints (Non-Operating)						
Hz	2	4	8	40	55	70	200
[G <sup>2</sup> /Hz]	0.001	0.03	0.03	0.003	0.01	0.01	0.001

Overall RMS (Root Mean Square) level of vibration is 1.04G (RMS).

#### 6.9.2.2 Swept Sine Vibration

- 2 G (Zero to peak), 5 to 500 to 5 Hz sine wave
- 0.5 oct/min sweep rate
- 3 minutes dwell at two major resonances

### **6.9.3 Operating Shock**

The drive meets the following criteria.

- No data loss, seek errors, or permanent damages within shock pulses of 10G, 11 ms half-sine wave.
- No data loss or permanent damages at Idle, Seek and Read modes within shock pulses of 30G 4ms, or 15G 5ms half-sine wave.

The shock pulses of each level are applied to the drive, five pulses in each direction and in all three axes. There must be a minimum of a 3 seconds delay between each shock pulse. The input level is applied to the base plate where the drive is attached with four screws.

### **6.9.4 Non-Operating Shock**

The drive withstands without damage or degradation of performance, a 75G half-sine wave shock pulse of 11 ms duration on six sides when heads are parked. (When the power is not applied to the unit, the heads are automatically located on the parked position.)

All shocks are applied in each direction of the drive three mutually perpendicular axes, one axis at a time. Input levels are measured at the frame of the hard disk drive.

## 6.10 Acoustics

The following shows the acoustic levels.

### 6.10.1 Sound Power Levels

The upper limit criteria of the A-weighted sound power levels are given in bels relative to one pico watt and are shown in the following table.

Figure 22. A-weighted Sound Power Levels	
Mode	A-weighted Sound Power Level [Bel]
Idle	4.5
Operating	4.8

Background power levels of the acoustic test chamber for each octave band are to be recorded.

Sound power levels are measured with the drive supported by spacers so that the lower surface of the drive is located  $25 \pm 3$ mm height from the chamber floor. No sound absorbing material shall be used.

The acoustical characteristics of the drive subsystem are measured under the following conditions.

Idle mode:

Powered on, disks spinning, track following, unit ready to receive and respond to control line commands.

Operating mode:

Continuous random cylinder selection and seek operation of actuator with a dwell time at each cylinder. Seek rate for the drive can be calculated as shown below.

Dwell time =  $(0.5 + N) \times 60/\text{RPM}$

Seek rate =  $1/(\text{Average seek time} + \text{Dwell time})$

Where N = number of maximum data surfaces (N=4 for DPEA-31080)

### 6.10.2 Sound Power Acceptance Criteria

Statistical upper limit  $(L_{\text{Woct}})_{\text{stat}}$  is calculated with the following formula.

$$(L_{\text{Woct}})_{\text{stat}} = (L_{\text{Woct}})_m + k \times (s_t)_{\text{Woct}}$$

where:

$(L_{\text{Woct}})_m$  is the mean value of the sound power level for samples of N drives.

$(s_t)_{\text{Woct}}$  is the total standard deviation for sound power level at each octave band.

$$(s_t)_{\text{Woct}} = \text{SQRT}((s_R)_W^2 + (s_P)_{\text{Woct}}^2)$$

$(s_R)_W$  is the standard deviation of reproducibility for sound power level.

Assume  $(s_R)_W = 0.075$  B.

$(s_P)_{\text{Woct}}$  is the standard deviation of the samples for sound power level at each octave band.

k is a coefficient determined by number of samples (N) as shown below.

N	3	4	5	6	7	8	9	10	11	12	13	14	15
k	3.19	2.74	2.74	2.49	2.33	2.22	2.13	2.07	2.01	1.97	1.93	1.90	1.87

The calculated left hand side of the criterion equation above is referred to as LWU and rounded to the nearest 0.05 bel. The individual terms may be rounded to the nearest 0.01 bel before calculation.

---

## 6.11 Identification Labels

The following labels are affixed to every drive.

1. A label placed on the top of the HDA contains the statement “Made by IBM” or equivalent, Part number, and MLC number.
2. A bar code label placed on the disk drive is based on user request. The location is to be designated in the drawing.
3. Labels containing the vendor's name, disk drive model number, serial number, place of manufacture and UL/CSA logos.

Except for the bar code, the labels may be integrated.

---

## 6.12 Electromagnetic Compatibility

The drive, when installed in the host system and exercised with a random accessing routine at maximum data rate, meets the worldwide EMC requirements listed below.

IBM will provide technical support to meet the requirements to comply with the EMC specifications.

- United States Federal Communications Commission (FCC) Rules and Regulations (Class B), Part 15.
- European Economic Community (EEC) directive number 76/889 related to the control of radio frequency interference and the Verband Deutscher Elektrotechniker (VDE) requirements of Germany (GOP).

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## **6.13 Safety**

The following shows the safety standards for the different countries.

### **6.13.1 Underwriters Lab (UL) Approval**

All models, DPEA-30540, DPEA-30810 and DPEA-31080 comply with UL 1950.

### **6.13.2 Canadian Standards Authority (CSA) Approval**

All models,  
DPEA-30540, DPEA-30810 and DPEA-31080 comply with CSA C22.2 #950-M89.

### **6.13.3 IEC Compliance**

All models, DPEA-30540, DPEA-30810 and DPEA-31080 comply with IEC 380, IEC 435 and IEC 950.

### **6.13.4 German Safety Mark**

All models, DPEA-30540, DPEA-30810 and DPEA-31080 were approved by TÜV on Test Requirements: EN 60 950:1988/A2:1991.

### **6.13.5 Flammability**

The printed circuit boards used in this product is made of material with the UL recognized flammability rating of V-1 or better. The flammability rating is marked or etched on the board. All other parts not considered electrical components are made of material with the UL recognized flammability rating of V-1 or better, except minor mechanical parts.

### **6.13.6 Safe Handling**

The products are conditioned for safe handling in regards to sharp edges and corners.

## 6.13.7 Environment

The product does not contain any known or suspected carcinogens.

Environmental controls meet or exceed all applicable government regulations in the country of origin. Safe chemical usage and manufacturing control are used to protect the environment. An environmental impact assessment has been done on the manufacturing process used to build the drive, the drive itself, and the disposal of the drive at the end of its life.

Production also meets the requirements of the international treaty on chlorofluorocarbon (CFC) control known as the United Nations Environment Program Montreal Protocol, and as ratified by the member nations. Materials to be controlled include CFC-11, CFC-12, CFC-113, CFC-114, CFC-115, Halon 1211, Halon 1301 and Halon 2402. Although not specified by the Protocol, CFC-112 is also controlled. In addition to the above protocol, IBM controls the following:

- All packaging materials used for the shipment of the product do not use controlled CFCs in the manufacturing process.
- All manufacturing processes for parts or assemblies including printed circuit boards, will not use the controlled CFC materials after December 31, 1993.

## 6.13.8 Secondary Circuit Protection

The drive uses printed circuit wiring that protects the possibility of sustained combustion due to circuit or component failure. Adequate secondary over-current protection is the responsibility of the using system.

The host system must protect the drive from any electrical short circuit problem. A 10 [A] limit is required for safety purposes.

---

## 6.14 Packaging

The drives are packed in ESD protective bags for shipping.

Once opening the ESD bag, drive handling with following things are recommended.

- To put drives on ESD mat.
- To use a wrist strap
- Don't douch the logic / interface connector pins

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## 6.15 Electrical Interface Specifications

### 6.15.1 Power Connectors

One of two kinds of DC power connector is used for the drive to work.

One connector has four pins and the other has three pins.

### 6.15.1.1 Power Connector

The DC power connector is designed to mate with AMP (part 1-480424-0) using AMP pins (part 350078-4) strip or (part 61173-4) loose piece, or their equivalents. Pin assignments are shown below.

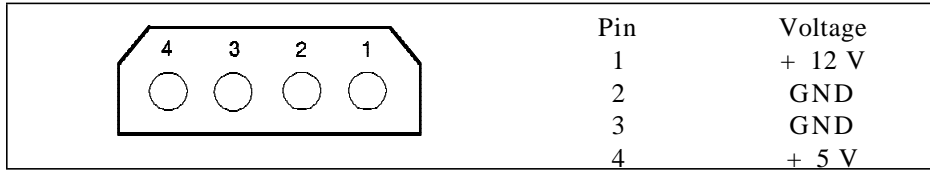


Figure 23. Power Connector Pin Assignments

### 6.15.1.2 Alternate Power Connector

The 3-pin DC power connector is designed to mate with the MOLEX (5480-03) using MOLEX pins (5479) or their equivalents. The pin assignments are shown in Figure 24.

Each line is connected to the corresponding voltage lines of the power connector as shown in Figure 23.



Figure 24. Alternate Power Connector Pin Assignments

## 6.15.2 Cabling

The maximum cable length from the host system to the drive, plus the circuit pattern length in the host system, cannot exceed 46 [cm].

### 6.15.3 Interface Connector

The DC 4-pin connector is designed to mate with AMP® 1-480424-0 or equivalent.

The AT signal connector is designed to mate with 3M® 3417-7000 or equivalent.

Figure 12 on page 18 shows the connector location.

### 6.15.4 Signal Definition

The pin assignments of interface signals are listed as follows:

PIN	SIGNAL	I/O	Type	PIN	SIGNAL	I/O	Type
01	-HRESET	I	TTL	02	GND		
03	HD07	I/O	3-state	04	HD08	I/O	3-state
05	HD06	I/O	3-state	06	HD09	I/O	3-state
07	HD05	I/O	3-state	08	HD10	I/O	3-state
09	HD04	I/O	3-state	10	HD11	I/O	3-state
11	HD03	I/O	3-state	12	HD12	I/O	3-state
13	HD02	I/O	3-state	14	HD13	I/O	3-state
15	HD01	I/O	3-state	16	HD14	I/O	3-state
17	HD00	I/O	3-state	18	HD15	I/O	3-state
19	GND			(20)	Key		
21	DMARQ	0	3-state	22	GND		
23	-HIOW	I	TTL	24	GND		
25	-HIOR	I	TTL	26	GND		
27	HIORDY	0	OC	28	CSEL	I	TTL
29	-DMACK	I	TTL	30	GND		
31	HIRQ	0	3-state	32	-HIOCS16	0	OC
33	HA01	I	TTL	34	-PDIAG	I/O	OC
35	HA00	I	TTL	36	HA02	I	TTL
37	-HCS0	I	TTL	38	-HCS1	I	TTL
39	-DASP	I/O	OC	40	GND		

Figure 25. Table of Signals

**Notes:**

1. "O" designates an output from the Drive.
2. "I" designates an input to the Drive.
3. "I/O" designates an input/output common.
4. "PWR" designates a power supply to the Drive.
5. "OC" designates Open-Collector or Open-Drain output.
6. "(Resv)" designates reserved pins and all of these have to be left unconnected.

**HD00-HD15** 16-bit bi-directional data bus between the host and the HDD. The lower 8 lines, HD00-07, are used for Register and ECC access. All 16 lines, HD00-15, are used for data transfer. These are 3-State lines have 24 mA current sink capability.

**HA00-HA02** Address used to select the individual register in the HDD.

**-HCS0** Chip select signal generated from the Host address bus. When active, one of the Command Block Registers (Data, Error{Features when written}, Sector Count, Sector Number, Cylinder Low, Cylinder High, Drive/Head and Status{Command when written} register) can be selected.  
(See Figure 31 on page 39.)

**-HCS1** Chip select signal generated from the Host address bus. When active, one of the Control Block Registers (Alternate Status{Device Control when written} and Drive Address register) can be selected.  
(See Figure 31 on page 39.)

**-HRESET** This line is used to reset the HDD. It shall be kept Low logic state during power up and kept High thereafter.

**-HIOW** Its rising edge holds data from the host data bus to a register or data register of the HDD.

- HIOR** When low, this signal enables data from a register or data register of the drive onto data bus. The data on the bus shall be latches on the rising edge of -HIOR.
- HIRQ** Interrupt is enabled only when the drive is selected, and the host activates the -IEN bit in the Device Control Reg. Otherwise, this signal is in high impedance state regardless of the state of the IRQ bit. The interrupt is set when the IRQ bit is set by the drive CPU. IRQ is reset to zero by a host read of the status register or a write to the Command Reg. This signal is a 3-State line with 24 mA sink capability.
- HIOCS16** Indication to the host that 16-bit wide data register has been addressed and that the drive is prepared to send or receive a 16-bit wide data word. This signal is an Open-Drain output with 24 mA sink capability and an external resistor is needed to pull this line to 5 Volt.
- DASP** This is a time-multiplexed signal which indicates that a drive is active, or that drive 1 is present. This signal is driven by Open-Drain driver and internally pulled-up to 5 Volt through 10Kohm resistor.  
 During Power-On initialization or after -HRESET is negated, -DASP shall be asserted by Drive 1 within 400 msec to indicate that drive 1 is present. Drive 0 shall allow up to 450msec for drive 1 to assert -DASP. If drive 1 is not present, drive 0 may assert -DASP to drive a LED indicator.  
 -DASP shall be negated following acceptance of the first valid command by drive 1. Anytime after negation of -DASP, either drive may assert -DASP to indicate that a drive is active. -DASP signal is immediately dropped if the command complete status is returned, even if the write cache is activated.
- PDIAG** This signal shall be asserted by drive 1 to indicate to drive 0 that it has completed diagnostics. This line is pulled-up to 5 Volt in the HDD through a 10Kohm resistor.  
 Following a Power On Reset, software reset or -HRESET, drive 1 shall negate -PDIAG within 1 msec (to indicate to drive 0 that it is busy). Drive 1 shall then assert -PDIAG within 30 seconds to indicate that it is no longer busy, and is able to provide status.  
 Following the receipt of a valid Execute Drive Diagnostics command, drive 1 shall negate -PDIAG within 1 msec to indicate to drive 0 that it is busy and has not yet passed its drive diagnostics. If drive 1 is present then drive 0 shall wait for up to 5 seconds from the receipt of a valid Execute Drive Diagnostics command for drive 1 to assert -PDIAG. Drive 1 should clear BSY before asserting -PDIAG, as -PDIAG is use to indicate that drive 1 has passed its diagnostics and is ready to post status.  
 If -DASP was not asserted by drive 1 during reset initialization, drive 0 shall post its own status immediately after it completes diagnostics, and clear the drive 1 Status register to 00h. Drive 0 may be unable to accept commands until it has finished its reset procedure and is ready (DRDY=1).
- CSEL (Cable Select) (Optional)**  
 The drive is configured as either Drive 0 or 1 depending upon the value of CSEL.
- If CSEL is grounded then the drive address is 0.
  - If CSEL is open then the drive address is 1.
- KEY** Pin position 20 has no connection pin. It is recommended to close respective position of the cable connector in order to avoid wrong insertion by mistake.
- HIORDY** This signal is negated to extend the host transfer cycle when a drive is not ready to respond to a data transfer request. This signal is an open-drain output with 24 mA sink capability and an external resistor is needed to pull this line to 5 volts.
- DMACK** This signal shall be used by the host in response to DMARQ to either acknowledge that data has been accepted, or that data is available.
- DMARQ** This signal, used for DMA data transfers between host and drive, shall be asserted by the drive when it is ready to transfer data to or from the host. The direction of data transfer is controlled by -HIOR and -HIOW. This signal is used on a handshake manner with

-DMACK. This signal is a 3-state line with 24mA sink capability and internally pulled-down to GND through 10 KOhm resistor.

#### 6.15.4.1 Interface Logic Signal Levels

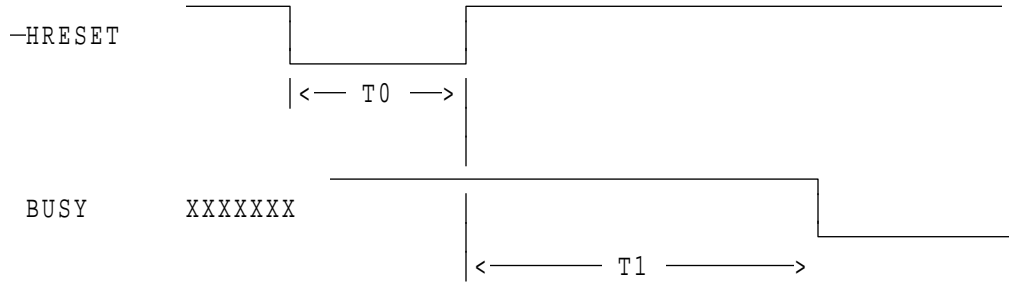
The interface logic signal have the following electrical specifications:

Inputs	Input High Voltage	2.0 V min.
	Input Low Voltage	0.8 V max.
Outputs	Output High Voltage	2.4 V min.
	Output Low Voltage	0.5 V max.

Figure 26. Logic Signal Levels

### 6.15.4.2 Reset timings

HDD reset timing.

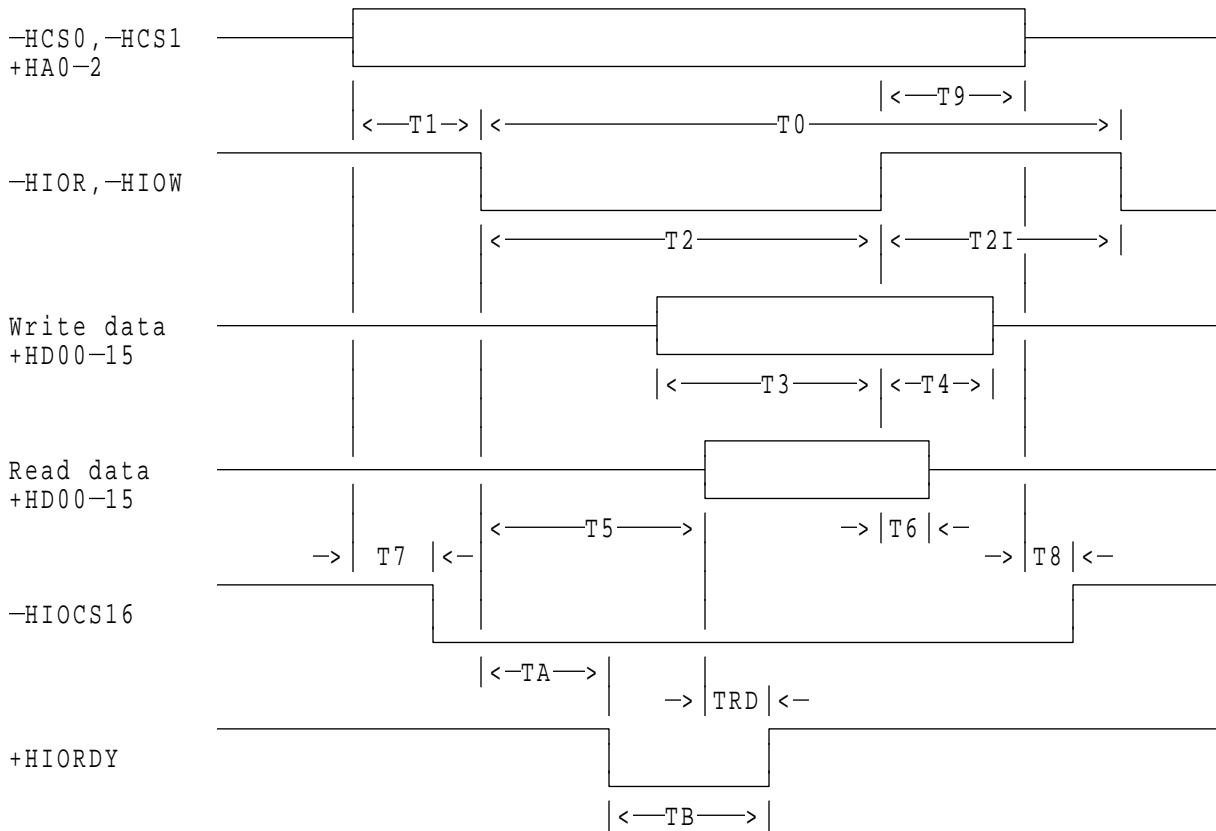


	PARAMETER DESCRIPTION	Min (usec)	Typ (sec)	Max (sec)
T0	-HRESET low width	25	—	—
T1	-HRESET high to Not BUSY	—	6	18

Figure 27. System Reset timing

### 6.15.4.3 PIO timings

The PIO cycle timings meet Mode-3 of the ATA description.



	PARAMETER DESCRIPTION	MIN (nsec)	MAX (nsec)	Note
T0	Cycle time	180	—	*1
T1	$\overline{\text{HCS0-1}}, +\text{HA00-02}$ valid to $\overline{\text{HIOR}}, \overline{\text{HIOW}}$ active	30	—	
T2	$\overline{\text{HIOR}}, \overline{\text{HIOW}}$ pulse width	80	—	
T2I	$\overline{\text{HIOR}}, \overline{\text{HIOW}}$ recovery	70	—	
T3	$+\text{HD00-15}$ setup to $\overline{\text{HIOW}}$ high	30	—	
T4	$\overline{\text{HIOW}}$ high to $+\text{HD00-15}$ hold	10	—	
T5	$\overline{\text{HIOR}}$ low to $+\text{HD00-15}$ valid	—	60	*2
T6	$\overline{\text{HIOR}}$ high to $+\text{HD00-15}$ hold	5	—	
T7	$\overline{\text{HCS0-1}}, +\text{HA00-02}$ valid to $\overline{\text{HIOCS16}}$ assertion	—	30	
T8	$\overline{\text{HCS0-1}}, +\text{HA00-02}$ invalid to $\overline{\text{HIOCS16}}$ negation	—	30	
T9	$\overline{\text{HIOR}}, \overline{\text{HIOW}}$ high to $\overline{\text{HCS0-1}}, +\text{HA00-02}$ hold	10	—	
TRD	$\overline{\text{READ}}$ data valid to $+\text{HIORDY}$ active	0	—	
TA	$\overline{\text{HIOR}}, \overline{\text{HIOW}}$ low to $+\text{HIORDY}$ low	—	35	
TB	$+\text{HIORDY}$ pulse width	—	1250	

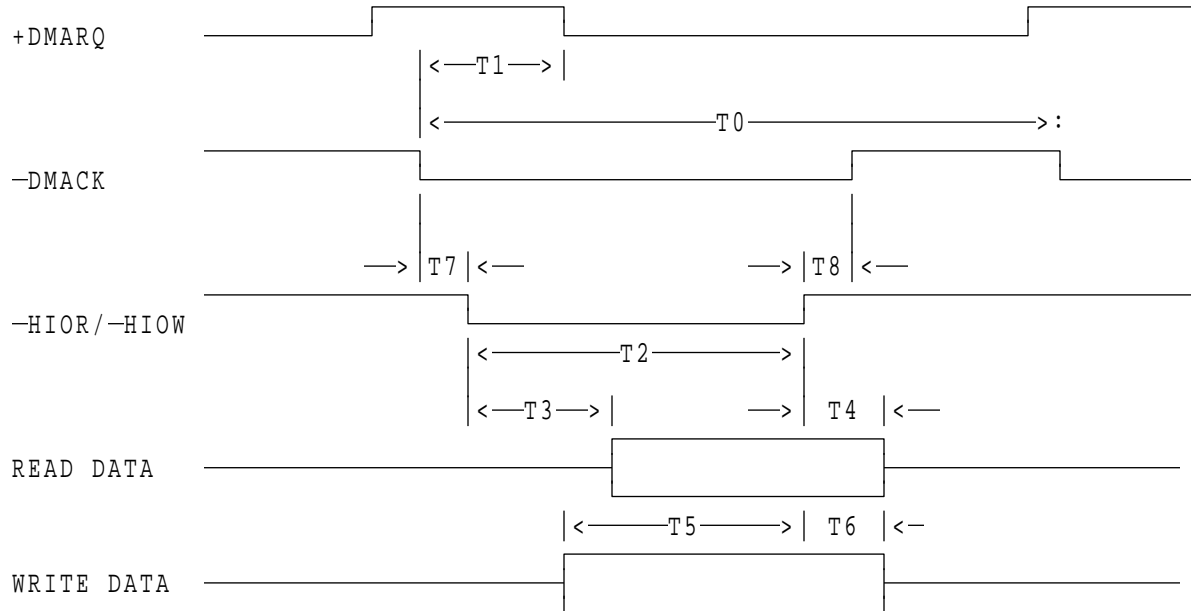
Note \*1)  $+\text{HIORDY}$  may be negated when a cycle time is less than 200 nsec.

Note \*2) When  $+\text{HIORDY}$  is negated, TRD is applied instead of this value.

Figure 28. PIO cycle timings

### 6.15.4.4 DMA timings (Single Word)

The Single Word DMA timing meet Mode 2 of the ATA description.

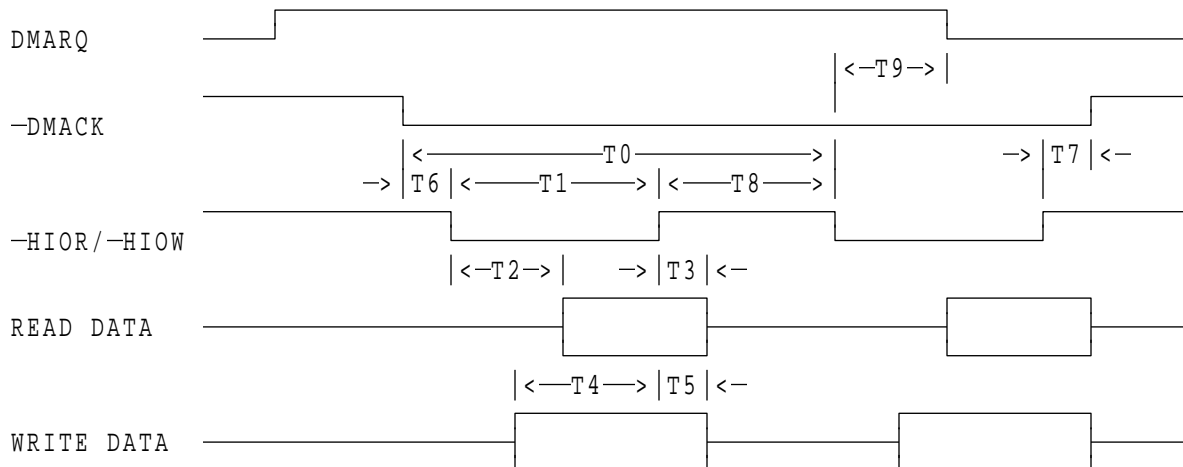


	PARAMETER DESCRIPTION	MIN (nsec)	MAX (nsec)	Note
T0	Cycle time	240	—	
T1	-DMA active to +DMARQ inactive	—	80	
T2	-HIOR, -HIOW pulse width	120	—	
T3	-HIOR data access	—	60	
T4	-HIOR data hold	5	—	
T5	-HIOW data setup	35	—	
T6	-HIOW data hold	20	—	
T7	-DMACK to -HIOR/-HIOW setup	0	—	
T8	-HIOR/-HIOW to -DMACK hold	0	—	

Figure 29. DMA (Single Word) cycle timings

### 6.15.4.5 DMA timings (Multiword)

The Multiword DMA timing meet Mode 1 of the ATA description.



	PARAMETER DESCRIPTION	MIN (nsec)	MAX (nsec)	Note
T0	Cycle time	180	—	
T1	-HIOR, -HIOW pulse width	80	—	
T2	-HIOR data access	—	60	
T3	-HIOR data hold	5	—	
T4	-HIOW data setup	30	—	
T5	-HIOW data hold	15	—	
T6	-DMACK to -HIOR/-HIOW setup	0	—	
T7	-HIOR/-HIOW to -DMACK hold	5	—	
T8	-HIOR/-HIOW negated pulse width	50	—	
T9	-HIOR/-HIOW to -DMARQ delay	—	40	

Figure 30. DMA (Multi Word) cycle timings

### 6.15.4.6 Addressing of HDD Registers

The host addresses the drive through a set of registers called the Task File. These registers are mapped into the host's I/O space. Two chip select lines (-HCS0 and -HCS1) and three address lines (HA00-02) are used to select one of these registers, while a -HIOR or -HIOW is provided at the specified time.

The -HCS0 is used to address Command Block registers. while the -HCS1 is used to address Control Block registers.

The following table shows the I/O address map.

Addr.	-CS0	-CS1	HA2	HA1	HA0	-IOR = 0 (Read)	-IOW = 0 (Write)
Command Block Registers							
1F0	0	1	0	0	0	Data Reg.	Data Reg.
1F1	0	1	0	0	1	Error Reg.	Features Reg.
1F2	0	1	0	1	0	Sector count Reg.	Sector count Reg.
1F3	0	1	0	1	1	Sector number Reg.	Sector number Reg.
1F4	0	1	1	0	0	Cylinder low Reg.	Cylinder low Reg.
1F5	0	1	1	0	1	Cylinder high Reg.	Cylinder high Reg.
1F6	0	1	1	1	0	Drive/Head Reg.	Drive/Head Reg.
1F7	0	1	1	1	1	Status Reg.	Command Reg.
Control Block Registers							
3F6	1	0	1	1	0	Alt. Status Reg.	Device control Reg
3F7	1	0	1	1	1	Drive address Reg.	—

Figure 31. Task File

**Note:** "Addr." field is shown just as an example.



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## 6.0 Interface Specification

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### 6.1 Conformance

The drive conforms to the referenced specifications, with the limitations described below.

**Automatic Power Down Sequence** A hard reset will disable the automatic power down sequence.

**Format Track** A drive will not perform a physical format. Instead it will simply write a data pattern of all zeros to the sectors which have been specified by the Format Track command. Bad sector flag which has been set by format track command will be cleared by write command.(ie. write sectors, write multiple, write DMA, write long) LBA mode for format track is not supported.

**Format Track Interleave Factor** The drive only supports an interleave factor of 1:1, and may ignore the sector number in format table without returning an error.

**Write long** Write long command should be executed for the same sector after Read long command execution. Otherwise, unexpected ECC correctable error may occur. Because of the limitation of the emulation technique to support 4 byte ECC mode which is implemented in the drive.

**Seek Overlap** The drive will wait for the seek to complete before interrupting the host. Therefore, no seek overlap can occur. This will be transparent to the host except that performance may be degraded in certain environments where the host could perform other work while waiting for seek complete, such as multitasking operating systems.

**Sleep Mode** During Sleep mode the drive will be activated by any command, including, but not limited to, a soft reset.

**Drive/Head Register** Bits 5 and 7 of Drive/Head Register are not written to 0. (These 2 bits are always read as '1' even after host writes to '0'.)

**Auto Reallocation Jumper** See Figure 32 on page 42 for relation with write cache. (+)Auto reallocation jumper is checked during the initial power on reset (POR) check. Write cache becomes off when a jumper for these pins is set automatically to keep data integrity. (+)Auto reallocation jumper position needs to be OPEN when a user system wants to use write cache.

**Write Cache Jumper** See Figure 32 on page 42 for relation among (+)auto reallocation jumper and set features command for write cache. (+)Write cache jumper is checked during the initial POR check.

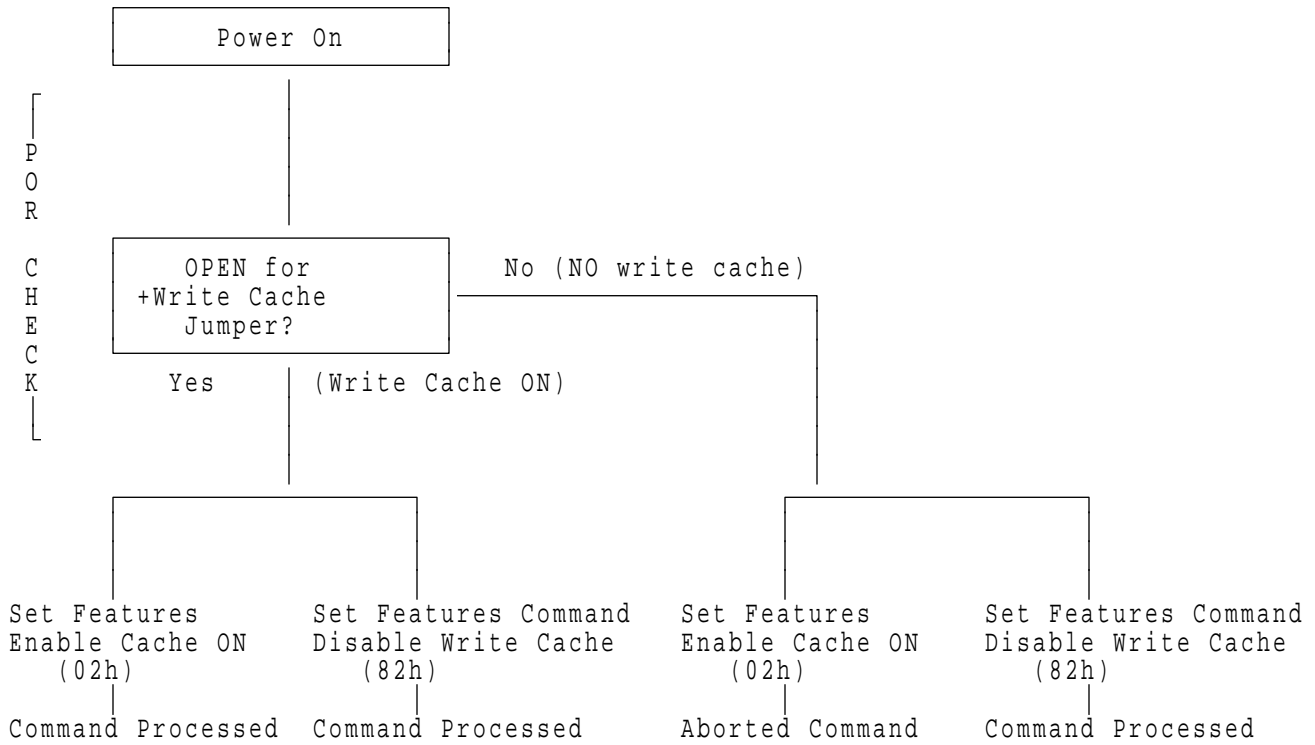


Figure 32. Relations Among Write Cache/Auto Reallocation Jumpers And Write Cache





## 7.0 Registers

Address	Input Register	Output Register
1F0h	Data	Data
1F1h	Error	Features
1F2h	Sector Count	Sector Count
1F3h	Sector Number *LBA Bits 0-7	Sector Number *LBA Bits 0-7
1F4h	Cylinder Low *LBA Bits 8-15	Cylinder Low *LBA Bits 8-15
1F5h	Cylinder High *LBA Bits 16-23	Cylinder High *LBA Bits 16-23
1F6h	Drive/Head /*LBA Bits 24-27	Drive/Head /*LBA Bits 24-27
1F7h	Status	Command
3F6h	Alternate Status	Device Control
3F7h	Drive Address	Not Used

Figure 33. Register Set

The host uses the register interface to communicate to and from the drive. The registers are accessed through the host port addresses shown.

The host should not read or write any registers when the Status Register BSY bit = 1.

Note: \* means meaning registers in LBA mode.

### 7.1 Alternate Status Register

Alternate Status Register							
7 BSY	6 RDY	5 DWF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR

Figure 34. Alternate Status Register

This register contains the same information as the Status Register. The only difference is that reading this register does not imply interrupt acknowledge or clear a pending interrupt. See 7.13, “Status Register” on page 49 for the definition of the bits in this register.

---

## 7.2 Command Register

This register contains the command code being sent to the drive. Command execution begins immediately after this register is written. The command set is shown in Figure 40 on page 57.

All other registers required for the command must be set up before writing the Command Register.

---

## 7.3 Cylinder High Register

In CHS mode, this register contains the high order bits of the starting cylinder address for any disk access. At the end of the command, this register is updated to reflect the current cylinder number.

In LBA mode, this register contains Bits 16-23 of the LBA. At the end of the command, this register is updated to reflect the correct LBA Bits 16-23.

---

## 7.4 Cylinder Low Register

In CHS mode, this register contains the low order 8 bits of the starting cylinder address for any disk access. At the end of the command, this register is updated to reflect the current cylinder number.

In LBA mode, this register contains Bits 8-15. At the end of the command, this register is updated to reflect the current LBA Bits 8-15.

---

## 7.5 Data Register

This register is used to transfer data blocks between the device data buffer and the host. It is also the register through which sector information is transferred on a Format command, and configuration information is transferred on an Identify Drive command.

All data transfers are 16 bits wide, except for ECC byte transfers, which are 8 bits wide. Data transfers are PIO only.

The register contains valid data only when DRQ=1 in the Status Register.

---

## 7.6 Device Control Register

Device Control Register							
7	6	5	4	3	2	1	0
—	—	—	—	1	SRST	—IEN	0

Figure 35. Device Control Register

## Bit Definitions

- SRST (RST)** Software Reset. The drive is held reset when RST=1. Setting RST=0 re-enables the drive.
- The host must set RST=1 and wait for at least 5 microseconds before setting RST=0, to ensure that the drive recognizes the reset.
- IEN** Interrupt Enable. When IEN=0, and the drive is selected, drive interrupts to the host will be enabled. When IEN=1, or the drive is not selected, drive interrupts to the host will be disabled.

---

## 7.7 Drive Address Register

Drive Address Register							
7	6	5	4	3	2	1	0
HIZ	-WTG	-H3	-H2	-H1	-H0	-DS1	-DS0

Figure 36. Drive Address Register

This register contains the inverted drive select and head select addresses of the currently selected drive.

### Bit Definitions

- HIZ** High Impedance. This bit is not driven and will always be in a high impedance state.
- WTG** -Write Gate. This bit is 0 when writing to the disk drive is in progress.
- H3,-H2,-H1,-H0** -Head Select. These four bits are the one's complement of the currently selected head. -H0 is the least significant.
- DS1** -Drive Select 1. Drive select bit for drive 1, active low. DS1=0 when drive 1 (slave) is selected and active.
- DS0** -Drive Select 0. Drive select bit for drive 0, active low. DS0=0 when drive 0 (master) is selected and active.

---

## 7.8 Drive/Head Register

Drive/Head Register							
7	6	5	4	3	2	1	0
1	L	1	DRV	HS3	HS2	HS1	HS0

Figure 37. Drive/Head Register

This register contains the drive and head numbers.

### Bit Definitions

- DRV** Drive. When DRV=0, drive 0 (master) is selected. When DRV=1, drive 1 (slave) is selected.

- HS3,HS2,HS1,HS0** If L=0, Head Select. These four bits select the head number. HS0 is the least significant. If L=1, HS0 through HS3 contain bit 24-27 of the LBA. At command completion, these bits are updated to reflect the current LBA bits 24-27.
- L** LBA mode. This bit selects the mode of operation. When L=0, addressing is by 'CHS' mode. When L=1, addressing is by 'LBA' mode.

---

## 7.9 Error Register

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDNF	0	ABRT	TK0NF	AMNF

Figure 38. Error Register

This register contains status from the last command executed by the drive, or a diagnostic code.

At the completion of any command except Execute Drive Diagnostic, the contents of this register are valid.

Following a power on, a reset, or completion of an Execute Drive Diagnostic command, this register contains a diagnostic code. See Figure 69 on page 96 for the definition.

### Bit Definitions

- BBK** Bad Block. BBK=1 indicates a bad block mark was detected in the requested sector's ID field.
- UNC** Uncorrectable Data Error. UNC=1 indicates an uncorrectable data error has been encountered.
- IDNF (IDN)** ID Not Found. IDN=1 indicates the requested sector's ID field could not be found.
- ABRT (ABT)** Aborted Command. ABT=1 indicates the requested command has been aborted due to a drive status error or an invalid parameter in an output register.
- TK0NF (T0N)** Track 0 Not Found. T0N=1 indicates track 0 was not found during a Recalibrate command.
- AMNF (AMN)** Address Mark Not Found. AMN=1 indicates the data address mark has not been found after finding the correct ID field for the requested sector.

---

## 7.10 Features Register

This register is used with the Set Features command to set the feature. See Set Features command description for parameters.

---

## 7.11 Sector Count Register

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the drive. If the value in the register is set to 0, a count of 256 sectors is specified.

If the register is zero at command completion, the command was successful. If not successfully completed, the register contains the number of sectors which need to be transferred in order to complete the request.

The contents of the register are defined otherwise on some commands. These definitions are given in the command descriptions.

---

## 7.12 Sector Number Register

This register contains the starting sector number for any disk data access for the subsequent command. The sector number may be from one to the maximum number of sectors per track.

See the command descriptions for contents of the register at command completion (whether successful or unsuccessful).

---

## 7.13 Status Register

Status Register							
7	6	5	4	3	2	1	0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

Figure 39. Status Register

This register contains the drive status. The contents of this register are updated whenever an error occurs and at the completion of each command.

If the host reads this register when an interrupt is pending, it is considered to be the interrupt acknowledge. Any pending interrupt is cleared whenever this register is read.

If BSY=1, no other bits in the register are valid.

### Bit Definitions

- BSY** Busy. BSY=1 whenever the drive is accessing the registers. The host should not read or write any registers when BSY=1. If the host reads any register when BSY=1, the contents of the Status Register will be returned.
- DRDY (RDY)** Drive Ready. RDY=1 indicates that the drive is capable of responding to a command. RDY will be set to 0 during power on until the drive is ready to accept a command.
- DWF** Drive Write Fault. DWF=1 indicates that the drive has detected a write fault condition. DWF is set to 0 after the Status Register is read by the host.

<b>DSC</b>	Drive Seek Complete. DSC=1 indicates that a seek has completed and the drive head is settled over a track. When an error occurs, this bit is not changed until the Status Register is read by the host, at which time the bit again indicates the current seek complete status.
<b>DRQ</b>	Data Request. DRQ=1 indicates that the drive is ready to transfer a word or byte of data between the host and the drive.
<b>CORR (COR)</b>	Corrected Data. COR=1 indicates that a correctable data error was encountered and the data has been corrected using the drive's ECC. The sector buffer contains the corrected data and multi-sector reads continue. The bit is set to 0 when a command is received.  During a multi-sector read verify operation, COR is set to 1 at the end of the operation if any of the verified sectors contained a correctable error.
<b>IDX</b>	Index. IDX=1 once per revolution. Since IDX=1 only for a very short time during each revolution, the host may not see it set to 1 even if the host is reading the Status Register continuously. Therefore the host should not attempt to use IDX for timing purposes.
<b>ERR</b>	Error. ERR=1 indicates that an error occurred during execution of the previous command. The Error Register should be read to determine the error type. The drive sets ERR=0 when the next command is received from the host.

---

## 8.0 Command Protocol

The commands are grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined below.

For all commands, the host must first check if BSY=1, and should proceed no further unless and until BSY=0. For all commands except Execute Drive Diagnostics and Initialize Drive Parameters the host must also wait for RDY=1 before proceeding.

Interrupts are cleared when the host reads the Status Register, issues a reset, or writes to the Command Register.

Figure 70 on page 99 shows the drive timeout values.

---

### 8.1 PIO Data In Commands

These commands are:

- Identify Drive
- Read Buffer
- Read Long
- Read Multiple
- Read Sectors

Execution includes the transfer of one or more 512 byte (>512 bytes on Read Long) sectors of data from the drive to the host.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Drive/Head Registers.
2. The host writes the command code to the Command Register.
3. For each sector (or block) of data to be transferred:
  - a. The drive sets BSY=1 and prepares for data transfer.
  - b. When a sector (or block) of data is available for transfer to the host, the drive sets BSY=0, sets DRQ=1, and interrupts the host.
  - c. In response to the interrupt, the host reads the Status Register.
  - d. The drive clears the interrupt in response to the Status Register being read.
  - e. The host reads one sector (or block) of data via the Data Register.
  - f. The drive sets DRQ=0 after the sector (or block) has been transferred to the host.
4. For the Read Long command:
  - a. The drive sets BSY=1 and prepares for data transfer.
  - b. When the sector of data and ECC bytes are available for transfer to the host, the drive sets BSY=0, sets DRQ=1, and interrupts the host.
  - c. In response to the interrupt, the host reads the Status Register.
  - d. The drive clears the interrupt in response to the Status Register being read.

- e. The host reads the sector of data and ECC bytes via the Data Register.
- f. The drive sets DRQ=0 after the ECC bytes have been transferred to the host.

The Read Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.

Note that the status data for a sector of data is available in the Status Register **before** the sector is transferred to the host.

If the drive detects an invalid parameter, then it will abort the command by setting BSY=0, ERR=1, ABT=1, and interrupting the host.

If an uncorrectable error occurs, the drive will set BSY=0, ERR=1, and DRQ=1. The drive will then store the error status in the Error Register, and interrupt the host. The registers will contain the location (CHS) of the sector in error.

If an Uncorrectable Data Error (UNC=1) occurs, the defective data will be transferred from the media to the sector buffer, and will be available to be transferred to the host, at the host's option. In case of Read Multiple command, the host should complete transfer the block which includes error data from the sector buffer and terminate whatever kind of type of error occurred.

If an error occurs that is correctable by using the ECC, the data will be corrected and the transfer will continue. The result will appear like a normal transfer except that the drive will set COR=1 in the Status Register.

If an error occurs that is correctable by retries, the data will be corrected and the transfer will continue normally. There will be no indication to the host that any retry occurred.

All data transfers to the host through the Data Register are 16 bits, except for the ECC bytes, which are 8 bits.

---

## 8.2 PIO Data Out Commands

These commands are:

- Format
- Write Buffer
- Write Long
- Write Multiple
- Write Sectors

Execution includes the transfer of one or more 512 byte (>512 bytes on Write Long) sectors of data from the host to the drive.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Drive/Head Registers.
2. The host writes the command code to the Command Register.
3. The drive sets BSY=1.
4. For each sector (or block) of data to be transferred:
  - a. The drive sets BSY=0 and DRQ=1 when it is ready to receive a sector (or block).

- b. The host writes one sector (or block) of data via the Data Register.
  - c. The drive sets BSY=1 after it has received the sector (or block).
  - d. When the drive has finished processing the sector (or block), it sets BSY=0, and interrupts the host.
  - e. In response to the interrupt, the host reads the Status Register.
  - f. The drive clears the interrupt in response to the Status Register being read.
5. For the Write Long command:
- a. The drive sets BSY=0 and DRQ=1 when it is ready to receive a sector.
  - b. The host writes one sector of data and ECC bytes via the Data Register.
  - c. The drive sets BSY=1 after it has received the sector and ECC bytes.
  - d. When the drive has finished processing the sector and ECC bytes, it sets BSY=0 and interrupts the host.
  - e. In response to the interrupt, the host reads the Status Register.
  - f. The drive clears the interrupt in response to the Status Register being read.

The Write Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.

If the drive detects an invalid parameter, then it will abort the command after the data transfer by setting BSY=0, ERR=1, ABT=1, and interrupting the host.

If an uncorrectable error occurs, the drive will set BSY=0 and ERR=1, store the error status in the Error Register, and interrupt the host. The registers will contain the location (CHS) of the sector in error.

All data transfers to the drive through the Data Register are 16 bits, except for the ECC bytes, which are 8 bits.

---

## 8.3 Non-Data Commands

These commands are:

- Check Power Mode
- Execute Drive Diagnostics
- Idle
- Initialize Drive Parameters
- Read Verify Sectors
- Recalibrate
- Seek
- Set Features
- Set Multiple
- Sleep
- Standby

Execution of these commands involves no data transfer.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Drive/Head Registers.
2. The host writes the command code to the Command Register.
3. The drive sets BSY=1.
4. When the drive has finished processing the command, it sets BSY=0, and interrupts the host.
5. In response to the interrupt, the host reads the Status Register.
6. The drive clears the interrupt in response to the Status Register being read.

---

## 8.4 DMA Data Transfer Commands

The Read/Write DMA protocol allows high performance multi-tasking operating systems to eliminate processor overhead associated with PIO transfers.

1. Command Phase
  - a. Host initialize the Slave-DMA channel
  - b. Host updates the Command Block Registers
  - c. Host writes command code to the Command Register
2. Data Phase
  - a. The Slave-DMA channel qualifies data transfers to and from drive with DMARQ
  - b. The Drive acknowledges a request with DMACK
  - c. Register contents are not valid during this phase
3. Status Phase
  - a. Drive generates an interrupt to the host (HIRQ=1)
  - b. Host resets the Slave-DMA Channel
  - c. Host reads the Status and Error Registers





## 9.0 Command Descriptions

Command	Hex Code	Binary Code								
		Bit	7	6	5	4	3	2	1	0
Check Power Mode	E5		1	1	1	0	0	1	0	1
Execute Drive Diagnostics	90		1	0	0	1	0	0	0	0
Format Track	50		0	1	0	1	0	0	0	0
Identify Drive	EC		1	1	1	0	1	1	0	0
Idle	E3		1	1	1	0	0	0	1	1
Idle Immediate	E1		1	1	1	0	0	0	0	1
Initialize Drive Parameters	91		1	0	0	1	0	0	0	1
Read Buffer	E4		1	1	1	0	0	1	0	0
Read DMA (retry)	C8		1	1	0	0	1	0	0	0
Read DMA (no retry)	C9		1	1	0	0	1	0	0	1
Read Long (retry)	22		0	0	1	0	0	0	1	0
Read Long (no retry)	23		0	0	1	0	0	0	1	1
Read Multiple	C4		1	1	0	0	0	1	0	0
Read Sectors (retry)	20		0	0	1	0	0	0	0	0
Read Sectors (no retry)	21		0	0	1	0	0	0	0	1
Read Verify Sectors (retry)	40		0	1	0	0	0	0	0	0
Read Verify Sectors (no retry)	41		0	1	0	0	0	0	0	1
Recalibrate	1x		0	0	0	1	—	—	—	—
Seek	7x		0	1	1	1	—	—	—	—
Set Features	EF		1	1	1	0	1	1	1	1
Set Multiple	C6		1	1	0	0	0	1	1	0
Sleep	E6		1	1	1	0	0	1	1	0
Standby	E2		1	1	1	0	0	0	1	0
Standby Immediate	E0		1	1	1	0	0	0	0	0
Write Buffer	E8		1	1	1	0	1	0	0	0
Write DMA (retry)	CA		1	1	0	0	1	0	1	0
Write DMA (no retry)	CB		1	1	0	0	1	0	1	1
Write Long (retry)	32		0	0	1	1	0	0	1	0
Write Long (no retry)	33		0	0	1	1	0	0	1	1
Write Multiple	C5		1	1	0	0	0	1	0	1
Write Sectors (retry)	30		0	0	1	1	0	0	0	0
Write Sectors (no retry)	31		0	0	1	1	0	0	0	1

Figure 40. Command Set

Figure 40 shows the commands that are supported by the drive. The following symbols are used in the command descriptions:

### Output Registers

- 0** Indicates that the bit must be set to 0.
- 1** Indicates that the bit must be set to 1.
- D** The drive number bit. Indicates that the drive number bit of the Drive/Head Register should be specified. Zero selects the master drive and one selects the slave drive.
- H** Head number. Indicates that the head number part of the Drive/Head Register is an output parameter and should be specified.
- R** Retry. Indicates that the Retry bit of the Command Register should be specified.

- V** Valid. Indicates that the bit is part of an output parameter and should be specified.
- L** This bit selects the mode of operation. When L=0, addressing is by 'CHS' mode. When L=1, addressing is by 'LBA' mode.
- x** Indicates that the hex character is not used.
- Indicates that the bit is not used.

**Input Registers**

- 0** Indicates that the bit is always set to 0.
- 1** Indicates that the bit is always set to 1.
- H** Head number. Indicates that the head number part of the Drive/Head Register is an input parameter and will be set by the drive.
- V** Valid. Indicates that the bit is part of an input parameter and will be set to 0 or 1 by the drive.
- Indicates that the bit is not part of an input parameter.

The command descriptions show the contents of the Status and Error Registers after the drive has completed processing the command and has interrupted the host.

## 9.1 Check Power Mode

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	0	1	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 41. Check Power Mode Command (E5h)

The Check Power Mode command will report whether the drive is spun up and the media is available for immediate access.

### Input Parameters From The Drive

**Sector Count** The power mode code. The command returns FFh in the Sector Count Register if the spindle motor is at speed and the drive is not in Standby or Sleep mode. Otherwise, the Sector Count Register will be set to 0.

## 9.2 Execute Drive Diagnostics

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	-	-	-	-	-
Command	1	0	0	1	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
V	V	V	V	V	V	V	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	0	0	-	-	0	-	0

Figure 42. Execute Drive Diagnostics Command (90h)

The Execute Drive Diagnostics command performs the internal diagnostic tests implemented by the drive. The results of the test are stored in the Error Register.

The normal Error Register bit definitions do not apply to this command. Instead, the register contains a diagnostic code. See Figure 69 on page 96 for the definition.

## 9.3 Format Track

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	1	0	1	D	H	H	H	H
Command	0	1	0	1	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 43. Format Track Command (50h)

The Format Track command formats a single track on the drive. Each sector of data on the track will be initialized to zero. Any data previously stored on the track will be lost.

The host writes a sector containing a format table to the drive. The format table should contain two bytes for each sector on the track to be formatted. The first byte should contain a descriptor value and the second byte is ignored. The descriptor value should be 0 for a good sector, and 80h for a bad sector. The descriptor value of 20h is to unassign the alternate location for this sector. And the descriptor value of 40h is for assign this sector to an alternate location. The remaining bytes of the sector following the format table are ignored.

### Output Parameters To The Drive

**Cylinder High/Low** The cylinder number of the track to be formatted.

**H** The head number of the track to be formatted.

### Input Parameters From The Drive

**Error** The Error Register. An Abort error (ABT=1) will be returned under the following conditions:

- The cylinder number is not valid.
- The head number is not valid.

## 9.4 Identify Drive

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	1	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 44. Identify Drive Command (ECh)

The Identify Drive command requests the drive to transfer configuration information to the host. The drive will transfer a sector to the host containing the information in Figure 45. The Identify Drive information is not affected by the Initialize Drive Parameters command.

Figure 45 (Page 1 of 3). Identify Drive Information

Word	Content	Description
00	045AH	<ul style="list-style-type: none"> <li>• Drive classification, bit assignments:               <ul style="list-style-type: none"> <li>– 15(=0): reserved for non-magnetic drives</li> <li>– 14(=0): format speed tolerance gap not required</li> <li>– 13(=0): track offset option not available</li> <li>– 12(=0): data strobe offset option not available</li> <li>– 11(=0): rotational speed tolerance &lt; = 0.5%</li> <li>– 10(=1): disk transfer rate &gt; 10 Mbps</li> <li>– 9(=0): disk transfer rate not ( &gt; 5 Mbps but &lt; = 10 Mbps )</li> <li>– 8(=0): disk transfer rate not ( &lt; = 5 Mbps )</li> <li>– 7(=0): not removable cartridge drive</li> <li>– 6(=1): fixed drive</li> <li>– 5(=0): spindle motor control option not implemented</li> <li>– 4(=1): head switch time &gt; 15 us</li> <li>– 3(=1): not MFM encoded</li> <li>– 2(=0): not soft sectored</li> <li>– 1(=1): hard sectored</li> <li>– 0(=0): reserved</li> </ul> </li> </ul>
01	1024	Number of Cylinders. (for drives of CHS=1024:16:63)
	1050	Number of Cylinders. (for drives of CHS=1050:16:63)
	1574	Number of Cylinders. (for drives of CHS=1574:16:63)
	2100	Number of Cylinders. (for drives of CHS=2100:16:63)
02	0	reserved
03	16	Number of heads. (for drives of CHS=1024:16:63)
	16	Number of heads. (for drives of CHS=1050:16:63)
	16	Number of heads. (for drives of CHS=1574:16:63)
	16	Number of heads. (for drives of CHS=2100:16:63)
04	34398	Number of unformatted bytes per track.
05	546	Number of unformatted bytes per sector
06	63	Number of sectors per track. (for drives of CHS=1024:16:63)
	63	Number of sectors per track. (for drives of CHS=1050:16:63)
	63	Number of sectors per track. (for drives of CHS=1574:16:63)
	63	Number of sectors per track. (for drives of CHS=2100:16:63)
07-09	0	Vendor Unique
10-19	XXXX	Serial number in ASCII
20	0003H	A dual ported, multi-sector buffer capable of simultaneous transfers with a read caching.
21	0380H	Buffer size in 512-byte increments
22	0010H	Number of ECC bytes

Figure 45 (Page 2 of 3). Identify Drive Information

<b>Word</b>	<b>Content</b>	<b>Description</b>
23-26	XXXX	Microcode revision (ASCII)
27-46	DPEA-30540	Model number in ASCII. (for drives of CHS=1024:16:63)
	DPEA-30540	Model number in ASCII. (for drives of CHS=1050:16:63)
	DPEA-30810	Model number in ASCII. (for drives of CHS=1574:16:63)
	DPEA-31080	Model number in ASCII. (for drives of CHS=2100:16:63)
47	0020H	Number of sectors that can be transferred per interrupt on Read and Write Multiple commands
48	0000H	cannot perform doubleword I/O
49	0F00H	IORDY, LBA and DMA are supported
50	0000H	Reserved
51	0300H	PIO data transfer cycle timing mode 3 is supported
52	0200H	DMA data transfer cycle timing mode 2 is supported
53	0003H	Words 54-58 are valid.
54		Number of current cylinders
55		Number of current heads
56		Number of current sectors per track
57		Low Word of Current capacity in sectors
58		High Word of Current capacity in sectors
59	01xxH	Multiple Sector Setting is Valid. xx = current setting for multiple commands.
	0000H	Multiple Sector Setting is no valid.
60	26C0H	Low Word of Number of LBAs. (for drives of CHS=1024:16:63)
	26C0H	Low Word of Number of LBAs. (for drives of CHS=1050:16:63)
	35E8H	Low Word of Number of LBAs. (for drives of CHS=1574:16:63)
	4D80H	Low Word of Number of LBAs. (for drives of CHS=2100:16:63)

Figure 45 (Page 3 of 3). Identify Drive Information		
Word	Content	Description
61	0010H	High Word of Number of LBAs. (for drives of CHS=1024:16:63)
	0010H	High Word of Number of LBAs. (for drives of CHS=1050:16:63)
	0018H	High Word of Number of LBAs. (for drives of CHS=1574:16:63)
	0020H	High Word of Number of LBAs. (for drives of CHS=2100:16:63)
62	0x07H	Single word DMA Mode 2 is supported. The high order byte contains bit sets to indicate which mode is active.
63	0x03H	Multiword DMA Mode 1 is supported. The high order byte contains bit sets to indicate which mode is active.
64	0001H	PIO mode 3 is supported.
65	00B4H	Minimum multiword DMA cycle time is 180ns.
66	0096H	Recommended multiword DMA cycle time is 150ns.
67	00C8H	Minimum PIO transfer cycle time without flow control is 200ns.
68	00B4H	Minimum PIO transfer cycle time with IORDY flow control is 180ns.
69-128	0000H	reserved
129	000xH	<ul style="list-style-type: none"> <li>• Vendor unique bit assignments for current set features and other setting status: <ul style="list-style-type: none"> <li>– Bit 15-4: (=0) reserved</li> <li>– Bit 3: auto reallocation (0=OFF, 1=ON)</li> <li>– Bit 2: reverting power on default (0=OFF, 1=ON)</li> <li>– Bit 1: read look ahead (0=OFF, 1=ON)</li> <li>– Bit 0: write cache (0=OFF, 1=ON)</li> </ul> </li> </ul>
130-255	0000H	reserved

## 9.5 Idle

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	0	0	1	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 46. Idle Command (E3h)

The Idle command causes the drive to enter Idle mode. The drive is spun up to operating speed. If the drive is already spinning, the spin up sequence is not executed. The timeout parameter may be used to enable the automatic power down sequence.

During Idle mode the drive is spun up and ready to respond to host commands, but execution may take slightly longer because some drive circuitry must be reactivated.

### Output Parameters To The Drive

**Sector Count** Timeout Parameter. If zero, then the automatic power down sequence is disabled. If non-zero, then the automatic power down sequence is enabled, and the timeout interval is set to the Timeout Parameter times 5, in seconds, for the value range from 12 to 255. If the value is 1 to 11, the Timeout Parameter is 60 seconds.

When the automatic power down sequence is enabled, the drive will enter Standby mode automatically if the timeout interval expires with no drive access from the host. The timeout interval will be reinitialized if there is a drive access before the timeout interval expires.

## 9.6 Idle Immediate

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	0	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 47. Idle Immediate Command (E1h)

The Idle Immediate command causes the drive to set BSY, enter the Idle Mode, clear BSY, and generate an interrupt. When the Idle Immediate command is received during the Standby mode, the drive will spin up to become ready to execute drive access command without delay.

## 9.7 Initialize Drive Parameters

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	H	H	H	H
Command	1	0	0	1	0	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	0	0	-	-	0	-	V

Figure 48. Initialize Drive Parameters Command (91h)

The Initialize Drive Parameters command enables the host to set the number of sectors per track and the number of heads minus 1, per cylinder. However when the drive of DPEA-30540 is set to 528 MB by removing a jumper for JP7, a number of cylinder is fixed to 1024.

### Output Parameters To The Drive

**Sector Count** The number of sectors per track. 0 does not mean there are 256 sectors per track, but there is no sector per track.

**H** The number of heads minus 1 per cylinder. The minimum is 0 and the maximum is 15.

## 9.8 Read Buffer

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	0	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 49. Read Buffer Command (E4h)

The Read Buffer command transfers a sector from the sector buffer to the host. The sector is transferred through the Data Register 16 bits at a time.

The sector transferred will be from the same part of the buffer written to by the last Write Buffer command. The contents of the sector may be different if any reads or writes have occurred since the Write Buffer command was issued.

## 9.9 Read DMA

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	1	0	0	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
V	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 50. Read DMA Command (C8h/C9h)

This command executes in a similar manner to the Read Sectors command except for the following:

- The host initialize a slave-DMA channel prior to issuing the command.
- data tranfers are qualified by DMARQ and are performed by the slave-DMA channel.
- the drive issues only one interrupt per command to indicate that data transfer has terminated and status is available.

Any unrecoverable error encountered during execution of a Read DMA command results in the termination of data transfer. The Drive issues an interrupt to indicate that data transfer has terminated and Status is available in the Error register. The error posting is the same as that for the read sectors command.

### Output Parameters To The Drive

- Sector Count**            The number of contiguous sectors to be transferred. If zero is specified, then 256 sectors are transferred.
- Sector Number**        The sector number of the first sector to be transferred.
- Cylinder High/Low**    The cylinder number of the first sector to be transferred.
- H**                        The head number of the first sector to be transferred.
- R**                        The retry bit. If set to one, then retries are disabled.

### **Input Parameters From The Drive**

<b>Sector Count</b>	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
<b>Sector Number</b>	The sector number of the last sector transferred.
<b>Cylinder High/Low</b>	The cylinder number of the last sector transferred.
<b>H</b>	The head number of the last sector transferred.

## 9.10 Read Long

Command Block Output Registers							
Register	7	6	5	4	3	2	1 0
Data	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-
Sector Count	0	0	0	0	0	0	1
Sector Number	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H
Command	0	0	1	0	0	0	1 R

Command Block Input Registers							
Register	7	6	5	4	3	2	1 0
Data	-	-	-	-	-	-	-
Error	...See Below...						
Sector Count	-	-	-	-	-	-	V
Sector Number	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V
Drive/Head	-	-	-	-	H	H	H
Status	...See Below...						

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
V	0	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 51. Read Long Command (22h/23h)

The Read Long command requests the file to transfer the data and ECC bytes of the designated sector from the drive to the host.

After 512 bytes of data have been transferred, the drive will set DRQ=1 to indicate that the drive is ready to transfer the ECC bytes to the host. The data is transferred 16 bits at a time, and the ECC bytes are transferred 8 bits at a time.

### Output Parameters To The Drive

- Sector Count** The number of contiguous sectors to be transferred. The Sector Count must be set to one.
- Sector Number** The sector number of the sector to be transferred.
- Cylinder High/Low** The cylinder number of the sector to be transferred.
- H** The head number of the sector to be transferred.
- R** The retry bit. If set to one, then retries are disabled.

### Input Parameters From The Drive

- Sector Count** The number of requested sectors not transferred.
- Sector Number** The sector number of the sector transferred.
- Cylinder High/Low** The cylinder number of the sector transferred.

**H** The head number of the sector transferred.

## 9.11 Read Multiple

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	0	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	V	-	V

Figure 52. Read Multiple Command (C4h)

The Read Multiple command transfers one or more sectors from the drive to the host. The sectors are transferred through the Data Register 16 bits at a time. Command execution is identical to the Read Sectors command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

### Output Parameters To The Drive

**Sector Count** The number of contiguous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

**Sector Number** The sector number of the first sector to be transferred.

**Cylinder High/Low** The cylinder number of the first sector to be transferred.

**H** The head number of the first sector to be transferred.

### Input Parameters From The Drive

**Sector Count** The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.

**Sector Number** The sector number of the last sector transferred.

**Cylinder High/Low** The cylinder number of the last sector transferred.

**H** The head number of the last sector transferred.

## 9.12 Read Sectors

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H	H
Command	0	0	1	0	0	0	0	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	V	-	V

Figure 53. Read Sectors Command (20h/21h)

The Read Sectors command transfers one or more sectors from the drive to the host. The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

### Output Parameters To The Drive

- Sector Count** The number of contiguous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
- Sector Number** The sector number of the first sector to be transferred.
- Cylinder High/Low** The cylinder number of the first sector to be transferred.
- H** The head number of the first sector to be transferred.
- R** The retry bit. If set to one, then retries are disabled.

### Input Parameters From The Drive

- Sector Count** The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
- Sector Number** The sector number of the last sector transferred.
- Cylinder High/Low** The cylinder number of the last sector transferred.
- H** The head number of the last sector transferred.

## 9.13 Read Verify Sectors

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H	H
Command	0	0	1	0	0	0	0	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	V	-	V

Figure 54. Read Verify Sectors Command (40h/41h)

The Read Verify Sectors verifies one or more sectors on the drive. No data is transferred to the host.

If an uncorrectable error occurs, the read verify will be terminated at the failing sector.

### Output Parameters To The Drive

**Sector Count** The number of contiguous sectors to be verified. If zero is specified, then 256 sectors will be verified.

**Sector Number** The sector number of the first sector to be verified.

**Cylinder High/Low** The cylinder number of the first sector to be verified.

**H** The head number of the first sector to be verified.

**R** The retry bit. If set to one, then retries are disabled.

### Input Parameters From The Drive

**Sector Count** The number of requested sectors not verified. This will be zero, unless an unrecoverable error occurs.

**Sector Number** The sector number of the last sector verified.

**Cylinder High/Low** The cylinder number of the last sector verified.

**H** The head number of the last sector verified.

## 9.14 Recalibrate

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	0	0	0	1	-	-	-	-

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	V	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 55. Recalibrate Command (1xh)

The Recalibrate command moves the read/write heads from anywhere on the disk to cylinder 0. If the drive cannot reach cylinder 0, T0N (Track 0 Not Found) will be set in the Error Register.

## 9.15 Seek

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H	H
Command	0	1	1	1	-	-	-	-

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 56. Seek Command (7xh)

The Seek command initiates a seek to the designated track and selects the designated head. The drive will wait for the seek to complete before setting BSY=0, DSC=1, and issuing the interrupt.

### Output Parameters To The Drive

**Cylinder High/Low** The cylinder number of the seek.

**H** The head number of the seek.

## 9.16 Set Features

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	V	V	V	V	V	V	V	V
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	1	1	1	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 57. Set Features Command (EFh)

The Set Features command is used by the host to establish the following parameters which affect the execution of certain drive features as shown in Figure 58. If the value in the register is other than one defined in the table, the drive posts an Aborted Command Error.

Figure 58. Set Feature Parameters	
	Description
02h	Enable Write Cache
03h	Set Transfer Mode based on value in Sector Counter Register
44h	Vendor unique length of ECC on Read Long/Write Long command
55h	Disable read look-ahead feature
66h	Disable reverting to power on defaults
82h	Disable Write Cache
AAh	Enable read look-ahead feature
BBh	4 bytes of ECC apply on Read Long/Write Long commands
CCh	Enable reverting to power on defaults

At power on, or after a hardware reset, the default mode is 02h,66h,0AAh and 0BBh. A setting of 66h allows settings which may have been modified since power on to remain at the same setting after a soft reset.

A host can choose the transfer mechanism by Set Transfer Mode and specifying a value in the Sector Count Register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value:

PIO Default Transfer Mode	00000	000
PIO Default Transfer Mode, Disable IORDY	00000	001
PIO Flow Control Transfer Mode x	00001	nnn (nnn=000,001,010 or 011)
Single word DMA mode x	00010	nnn (nnn=000,001 or 010)
Multiword DMA mode x	00100	nnn (nnn=000 or 001)

where 'nnn' is a valid mode number in binary bit for the associated transfer type.

## 9.17 Set Multiple

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	0	0	0	1	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	TON	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 59. Set Multiple Command (C6h)

The Set Multiple command enables the drive to perform Read and Write Multiple commands and establishes the block size for these commands. The block size is the number of sectors to be transferred for each interrupt.

At power on, or after a hardware reset, the default mode is Read and Write Multiple disabled. If Disable Default has been set in the Features Register then the mode remains the same as that last established prior to a soft reset, otherwise it reverts to the default of disabled.

If an invalid block size is specified, an Abort error will be returned to the host, and Read Multiple and Write Multiple commands will be disabled.

### Output Parameters To The Drive

**Sector Count.** The block size to be used for Read Multiple and Write Multiple commands. Valid block sizes are 0, 2, 4, 8, 16, and 32. If 0 is specified, then Read Multiple and Write Multiple commands are disabled.

## 9.18 Sleep

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	0	1	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 60. Sleep Command (E6h)

The Sleep command causes the drive to enter Sleep mode, which is its minimal power mode. If the drive is not already spun down, the spin down sequence is executed. After the drive has stopped, BSY is set to 0, and the host is interrupted.

During the Sleep mode the drive will respond to commands, but there may be a delay while waiting for the spindle to reach operating speed.

## 9.19 Standby

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	0	0	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 61. Standby Command (E2h)

The Standby command causes the drive to enter the Standby Mode.

When the Standby mode is entered, the drive is spun down but the interface remains active. If the drive is already spun down, the spin down sequence is not executed.

During the Standby mode the drive will respond to commands, but there may be a delay while waiting for the spindle to reach operating speed.

If the Sector Count Register is non-zero then the automatic power down sequence shall be enabled and the timer will begin counting down when the drive returns to Idle mode. If the Sector Count Register is zero then the automatic power down sequence shall be disabled.

### Output Parameters To The Drive

**Sector Count** Timeout Parameter. If zero, then the automatic power down sequence is disabled. If non-zero, then the automatic power down sequence is enabled, and the timeout interval is set to the Timeout Parameter times 5, in seconds, for the value range from 12 to 255. If the value is 1 to 11, the Timeout Parameter is 60 seconds.

When the automatic power down sequence is enabled, the drive will enter Standby mode automatically if the timeout interval expires with no drive access from the host. The timeout interval will be reinitialized if there is a drive access before the timeout interval expires.

## 9.20 Standby Immediate

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 62. Standby Immediate Command (E0h)

The Standby Immediate command causes the drive to set BSY, enter the Standby Mode, clear BSY, and generate an interrupt. The spindle will be stopped to reduce the power usage. The Host interface is always ready to receive a command from the host. Any media access command will cancel the Standby mode. The host is required to resend the Standby Immediate command to spin down the drive.

## 9.21 Write Buffer

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	1	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 63. Write Buffer Command (E8h)

The Write Buffer command transfers a sector of data from the host to the sector buffer. The sectors are transferred through the Data Register 16 bits at a time.

The Read Buffer and Write Buffer commands are synchronized such that sequential Write Buffer and Read Buffer commands access the same 512 byte within buffer.

## 9.22 Write DMA

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	1	0	1	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
V	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 64. Write DMA Command (CAh/CBh)

This command executes in a similar manner to the Write Sectors command except for the following:

- The host initialize a slave-DMA channel prior to issuing the command.
- data tranfers are qualified by DMARQ and are performed by the slave-DMA channel.
- the drive issues only one interrupt per command to indicate that data

transfer has terminated and status is available.

Any unrecoverable error encountered during execution of a Write DAM command results in the termination of data transfer. The Drive issues an interrupt to indicate that data transfer has terminated and Status is available in the Error register. The error posting is the same as that for the write sectors command.

### Output Parameters To The Drive

- Sector Count**            The number of contiguous sectors to be transferred. If zero is specified, then 256 sectors are transferred.
- Sector Number**        The sector number of the first sector to be transferred.
- Cylinder High/Low**    The cylinder number of the first sector to be transferred.
- H**                        The head number of the first sector to be transferred.
- R**                        The retry bit. If set to one, then retries are disabled.

### **Input Parameters From The Drive**

<b>Sector Count</b>	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
<b>Sector Number</b>	The sector number of the last sector transferred.
<b>Cylinder High/Low</b>	The cylinder number of the last sector transferred.
<b>H</b>	The head number of the last sector transferred.

## 9.23 Write Long

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	0	0	0	0	0	0	0	1
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H	H
Command	0	0	1	1	0	0	1	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
V	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 65. Write Long Command (32h/33h)

The Write Long command requests the file to transfer the data and ECC bytes of the designated sector from the host to the drive.

The data is transferred 16 bits at a time, and the ECC bytes are transferred 8 bits at a time.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

### Output Parameters To The Drive

**Sector Count** The number of contiguous sectors to be transferred. The Sector Count must be set to one.

**Sector Number** The sector number of the sector to be transferred.

**Cylinder High/Low** The cylinder number of the sector to be transferred.

**H** The head number of the sector to be transferred.

**R** The retry bit. If set to one, then retries are disabled.

### Input Parameters From The Drive

**Sector Count** The number of requested sectors not transferred.

**Sector Number** The sector number of the sector transferred.

**Cylinder High/Low** The cylinder number of the sector transferred.

**H** The head number of the sector transferred.

## 9.24 Write Multiple

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	0	1	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
V	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 66. Write Multiple Command (C5h)

The Write Multiple command transfers one or more sectors from the host to the drive. Command execution is identical to the Write Sectors command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector. The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

### Output Parameters To The Drive

**Sector Count** The number of contiguous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

**Sector Number** The sector number of the first sector to be transferred.

**Cylinder High/Low** The cylinder number of the first sector to be transferred.

**H** The head number of the first sector to be transferred.

### Input Parameters From The Drive

**Sector Count** The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.

**Sector Number** The sector number of the last sector transferred.

**Cylinder High/Low** The cylinder number of the last sector transferred.

**H** The head number of the last sector transferred.

## 9.25 Write Sectors

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H	H
Command	0	0	1	1	0	0	0	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
V	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 67. Write Sectors Command (30h/31h)

The Write Sectors command transfers one or more sectors from the host to the drive. The sectors are transferred through the Data Register 16 bits at a time.

When write cache is disable, the write will be terminated at the failing sector if an uncorrectable error occurs.

When write cache is enable, automatic reallocation will be invoked at the failing sector if an uncorrectable error occurs and the write will be completed normally.

### Output Parameters To The Drive

**Sector Count** The number of contiguous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

**Sector Number** The sector number of the first sector to be transferred.

**Cylinder High/Low** The cylinder number of the first sector to be transferred.

**H** The head number of the first sector to be transferred.

**R** The retry bit. If set to one, then retries are disabled.

### Input Parameters From The Drive

**Sector Count** The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.

**Sector Number** The sector number of the last sector transferred.

**Cylinder High/Low**    The cylinder number of the last sector transferred.  
**H**                        The head number of the last sector transferred.





---

## 10.0 Reset

---

### 10.1 Power On Reset

After power on, the drive performs hardware initialization and executes its internal diagnostics. During this time the spindle is spun up to its operating speed.

The registers are initialized as shown in Figure 68 on page 96.

---

### 10.2 Hard Reset

A hard reset will cause any task currently in progress to be aborted. The drive will then re-initialize its internal variables and execute its internal diagnostics.

A hard reset occurs when the host asserts the bus RESET signal.

The registers are initialized as shown in Figure 68 on page 96.

---

### 10.3 Software Reset

A software reset will cause any task currently in progress to be aborted. The drive will then re-initialize its internal variables and execute its internal diagnostics.

The registers are initialized as shown in Figure 68 on page 96.

The host must set Device Control register bit RST=1 and wait for at least 5 microseconds before setting RST=0, to ensure that the drive recognizes the reset.

---

### 10.4 Register Initialization

Register	Default Value
Error	Diagnostic Code
Sector Count	01h
Sector Number	01h
Cylinder Low	00h
Cylinder High	00h
Drive/Head	A0h
Status	50h
Alternate Status	50h

Figure 68. Default Register Values

After power on, hard reset, or software reset, the register values are initialized as shown in Figure 68.

Code	Description
01h	No error detected
02h	Formatter device error
03h	Sector buffer error
04h	ECC circuitry error
05h	Controller microprocessor error
8xh	Slave drive failed

Figure 69. Diagnostic Codes

The meaning of the Error Register diagnostic codes resulting from power on, hard reset or the Execute Drive Diagnostic command are shown in Figure 69.





## 11.0 Timings

FUNCTION	INTERVAL	START	STOP	TIMEOUT
Power On	Drive Busy After Power On	Power On	Status Register BSY=1	400 ns
	Drive Ready After Power On	Power On	Status Register BSY=0 and RDY=1	31 sec
Software Reset	Drive Busy After Software Reset	Device Control Register RST=1	Status Register BSY=1	400 ns
	Drive Ready After Software Reset	Device Control Register RST=1	Status Register BSY=0 and RDY=1	6 sec
Hard Reset	Drive Busy After Hard Reset	Bus RESET Signal Asserted	Status Register BSY=1	400 ns
	Drive Ready After Hard Reset	Bus RESET Signal Asserted	Status Register BSY=0 and RDY=1	31 sec
Data In Command	Drive Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns
	Interrupt, DRQ For Data Transfer In	Status Register BSY=1	Status Register BSY=0 and DRQ=1, Interrupt	10 sec
	Drive Busy After Data Transfer In	256th Read From Data Register	Status Register BSY=1	10 us
Data Out Command	Drive Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns
	Data Request For Data Transfer Out	Status Register BSY=1	Status Register BSY=0 and DRQ=1	1 ms
	Drive Busy After Data Transfer Out	256th Write From Data Register	Status Register BSY=1	5 us
	Interrupt For Data Transfer Out	Status Register BSY=1	Interrupt	10 sec
Non-Data Command	Drive Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	700 us
	Interrupt For Command Complete	Status Register BSY=1	Interrupt	6 sec

Figure 70. Timeout Values

The host must always give the drive sufficient time to perform each command or command phase. Figure 70 shows the commands and command phases, and the minimum timeout intervals that the host should wait before reporting an error. The abbreviations "ns", "us", "ms" and "sec" mean nanoseconds, microseconds, milliseconds and seconds, respectively.

The timeout values shown do not relate to normal drive performance. They are based on worst case conditions, with an added safety margin. Since timeout conditions will be very rare events, host performance will not be affected by the added safety margin.

It is recommended that the host use processor-independent timing loops, so that the timeout intervals will still be valid when faster processors are implemented.

When issuing a software reset, the host must set Device Control register bit RST=1 and wait for at least 5 microseconds before setting RST=0, to ensure that the drive recognizes the reset.

---

## Appendix A. Cache

---

### A.1 Read Look-Ahead

The drive keeps the adaptive segmented buffers as read cache.

- Least Frequent Used buffer is discarded to save the newly requested data.

---

### A.2 Write Cache

When the write cache is enabled, write cache uses an adaptive segmented buffer. (The write cache is enabled by checking jumper setting at power-on-reset period. And if the jumper setting is for enabling write cache, this can be enabled or disabled by sending set features commands.)

- If the previous command is WRITE, and the block requested is consecutive to the previous, the drive will return "COMPLETE" after all data is received in the drive buffer.
- Soft reset is recommended to check the actual data writing to media, i.e., soft reset is processed after the previous write command (with cache) completes the actual writing to media.
- Certain power down during Write Cache operation may result in Non-recoverable error later. Write to the broken sector will recover this sector.
- Automatic reallocation will be invoked at the failing sector if a non-recoverable error occurs and the write will be completed normally.
- If the drive runs out of spares for reallocation, write cache and reallocation will be turned off.
- If the drive is unable to complete a cached write and/or reallocation after good status has been returned, the drive will not process any commands including a soft reset. This condition will be cleared at power on, or a hardware reset.



## Appendix B. Index

### A

ABRT 48  
ABT 48  
Alternate Status Register 45  
AMN 48  
AMNF 48  
Auto Reallocation Jumper 41  
Automatic Power Down Sequence 41, 66, 83

### B

BBK 48  
BSY 49

### C

Check Power Mode 53, 59  
Command  
    Check Power Mode 59  
    Execute Drive Diagnostics 60  
    Format Track 41, 61  
    Identify Drive 62  
    Idle 66  
    Idle Immediate 67  
    Initialize Drive Parameters 68  
    Read Buffer 69  
    Read DMA 70  
    Read Long 72  
    Read Multiple 74  
    Read Sectors 75  
    Read Verify Sectors 76  
    Recalibrate 77  
    Seek 41, 78  
    Set Features 79  
    Set Multiple 81  
    Sleep 82  
    Sleep Mode 41  
    Standby 83  
    Standby Immediate 84  
    Write Buffer 85  
    Write DMA 86  
    Write long 41, 88  
    Write Multiple 90  
    Write Sectors 91  
Command Register 45  
COR 50  
CORR 50

Cylinder High Register 46  
Cylinder Low Register 46

### D

D 57  
Data Register 46  
Device Control Register 46  
Diagnostic Codes 48, 60, 96  
DRDY 49  
Drive Address Register 47  
Drive/Head Register 41, 47  
DRQ 50  
DRV 47  
DS0 47  
DS1 47  
DSC 49  
DWF 49

### E

ERR 50  
Error Register 48  
    Diagnostic Codes 96  
Execute Drive Diagnostics 53, 60

### F

Features Register 48  
Format 52  
Format Track 41, 61

### H

H 57, 58  
H0 47  
H1 47  
H2 47  
H3 47  
Hard Reset 95  
HS0 47  
HS1 47  
HS2 47  
HS3 47

### I

Identify Drive 51, 62  
Idle 53, 66

Idle Immediate 67  
IDN 48  
IDNF 48  
IDX 50  
IEN 47  
Initialize Drive Parameters 53, 68

## L

L 48, 58

## M

Master 47

## P

Power On Reset 95

## R

R 57  
RDY 49  
Read Buffer 51, 69  
Read DMA 70  
Read Long 51, 72  
Read Multiple 51, 74  
Read Sectors 51, 75  
Read Verify Sectors 53, 76  
Recalibrate 53, 77  
Register  
    Alternate Status Register 45  
    Command Register 45  
    Cylinder High Register 46  
    Cylinder Low Register 46  
    Data Register 46  
    Device Control Register 46  
    Drive Address Register 47  
    Drive/Head Register 47  
    Error Register 48  
    Features Register 48  
    Register Initialization 95  
    Sector Count Register 48  
    Sector Number Register 49  
    Status Register 49  
Register Initialization 95  
Reset 41  
    Hard Reset 95  
    Power On Reset 95  
    Register Initialization 95  
    Software Reset 95  
RST 47

## S

Seek 41, 53, 78  
Set Features 53, 79  
Set Multiple 53, 81  
Slave 47  
Sleep 53, 82  
Sleep Mode 41  
Software Reset 95  
SRST 47  
Standby 53, 83  
Standby Immediate 84  
Status Register 49

## T

T0N 48  
Timeout Interval 47, 95, 97  
Timeout Parameter 66, 83  
TKONF 48

## U

UNC 48

## V

V 57, 58

## W

Write Buffer 52, 85  
Write Cache 79, 91, 101  
Write Cache Jumper 41  
Write DMA 86  
Write long 41, 52, 88  
Write Multiple 52, 90  
Write Sectors 52, 91  
    Write Cache 79, 91, 101  
WTG 47

## X

x 58





S85G-2534-02