



OEM HARD DISK DRIVE SPECIFICATIONS

for

DAQA-32160/32700/33240 (2160/2700/3240 MB)

3.5-Inch Hard Disk Drive with ATA Interface

Revision (2.0)



OEM HARD DISK DRIVE SPECIFICATIONS

for

DAQA-32160/32700/33240 (2160/2700/3240 MB)

3.5-Inch Hard Disk Drive with ATA Interface

Revision (2.0)

1st Edition (1.0) S46H-3342-00 (Jan. 31, 1996)
2nd Edition (1.1) S46H-3342-01 (Apr. 01, 1996)
3rd Edition (1.2) S46H-3342-02 (Apr. 15, 1996)
4th Edition (1.3) S46H-3342-03 (May. 31, 1996)
5th Edition (1.4) S46H-3342-04 (Jun. 21, 1996)
6th Edition (2.0) S46H-3342-05 (Sep. 10, 1996)

The following paragraph does not apply to the United Kingdom or any country where such provisions are inconsistent with local law: INTERNATIONAL BUSINESS MACHINES CORPORATION PROVIDES THIS PUBLICATION "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Some states do not allow disclaimer or express or implied warranties in certain transactions, therefore, this statement may not apply to you.

This publication could include technical inaccuracies or typographical errors. Changes are periodically made to the information herein; these changes will be incorporated in new editions of the publication. IBM may make improvements and/or changes in the product(s) and/or the program(s) described in this publication at any time.

It is possible that this publication may contain reference to, or information about, IBM products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that IBM intends to announce such IBM products, programming, or services in your country.

Technical information about this product is available by contacting with local IBM representative or the following.

Tel:+1-507-253-4110 / Fax:+1-507-253-4111 ----- U.S.A
Tel:+81-466-45-1441 / Fax:+81-466-45-1045 ----- Japan
Tel:+44-1705-486363 / Fax:+44-1705-498930 ----- England
Tel:+49-6131-845050 / Fax:+49-6131-846442 ----- Germany

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Armonk, NY 10577.

© Copyright International Business Machines Corporation 1996. All rights reserved.

Note to U.S. Government Users — Documentation related to restricted rights — Use, duplication or disclosure is subject to restrictions set forth in GSA ADP Schedule Contract with IBM Corp.

Contents

1.0 General	1
1.1 Glossary	1
1.2 General Caution	1
2.0 General Features	3
<hr/>	
Part 1. Functional Specification	5
3.0 Drive Characteristics	7
3.1 Logical Drive Format	7
3.2 Data Sheet	7
3.3 Performance Characteristics	8
3.3.1 Command Overhead	8
3.3.2 Mechanical Positioning	9
3.3.3 Drive Ready Time	11
3.3.4 Data Transfer Speed	11
3.3.5 Throughput	12
3.3.6 Operating Mode Definition	13
4.0 Data Integrity	15
4.1 Data loss at Power Off	15
4.2 Write Cache	15
4.3 Equipment Status	15
5.0 Physical Format	17
5.1 Shipped Format	17
6.0 Specification	19
6.1 Electrical interface specification	19
6.1.1 Connectors	19
6.1.2 Signal Definition	20
6.1.3 Interface Logic Signal Levels	22
6.1.4 Reset Timings	23
6.1.5 PIO Timings	24
6.1.6 DMA Timings (Single Word)	26
6.1.7 DMA Timings (Multiword)	27
6.1.8 Addressing of HDD Registers	28
6.1.9 Cabling	28
6.1.10 Jumper Settings	29
6.2 Environment	32
6.3 DC Power Requirements	33
6.4 Reliability	35
6.4.1 Contact Start Stop (CSS)	35
6.4.2 Preventive Maintenance	35
6.4.3 Data Reliability	35
6.4.4 Cable Noise Interference	35
6.5 Mechanical Specifications	36
6.5.1 Outline	36
6.5.2 Mechanical Dimensions and Weight	36
6.5.3 Connector Locations	38

6.5.4	Hole Locations	39
6.5.5	Mounting Orientation	40
6.5.6	Shipping Zone and Lock	40
6.6	Vibration and Shock	41
6.6.1	Operating Vibration	41
6.6.2	Non-Operating Vibration	41
6.6.3	Operating Shock	42
6.6.4	Non-Operating Shock	42
6.7	Acoustics	43
6.7.1	Sound Power	43
6.8	Identification	44
6.8.1	Labels	44
6.9	Electromagnetic Compatibility	44
6.9.1	CE Mark	44
6.10	Safety	45
6.10.1	Underwriters Lab(UL) Approval	45
6.10.2	Canadian Standards Authority(CSA) Approval	45
6.10.3	IEC Compliance	45
6.10.4	German Safety Mark	45
6.10.5	Flammability	45
6.10.6	Secondary Circuit Protection	45
6.11	Packaging	45

Part 2. ATA Interface Specification 47

7.0	Interface	49
7.1	Deviation from Standard	49
8.0	Registers	51
8.1	Alternate Status Register	51
8.2	Command Register	52
8.3	Cylinder High Register	52
8.4	Cylinder Low Register	52
8.5	Data Register	52
8.6	Device Control Register	53
8.7	Drive Address Register	53
8.8	Device/Head Register	53
8.9	Error Register	54
8.10	Features Register	55
8.11	Sector Count Register	55
8.12	Sector Number Register	55
8.13	Status Register	55
9.0	General Operation Descriptions	57
9.1	Reset Response	57
9.1.1	Register Initialization	58
9.2	Diagnostic and Reset considerations	59
9.3	Sector Addressing Mode	60
9.3.1	Logical CHS Addressing Mode	60
9.3.2	LBA Addressing Mode	60
9.4	Power Management Feature	61
9.4.1	Power Mode	61
9.4.2	Power Management Commands	61
9.4.3	Standby timer	61

9.4.4	Interface Capability for Power Modes	62
9.5	S.M.A.R.T. Function	63
9.5.1	Attributes	63
9.5.2	Attribute values	63
9.5.3	Attribute thresholds	63
9.5.4	Threshold exceeded condition	63
9.5.5	S.M.A.R.T. commands	63
9.6	Reassign Function	64
9.6.1	Auto Reassign Function	64
9.7	Write Cache Function	65
9.8	Write Cache Jumper	65
10.0	Command Protocol	67
10.1	Data In Commands	67
10.2	Data Out Commands	69
10.3	Non-Data Commands	71
10.4	DMA Data Transfer Commands	72
11.0	Command Descriptions	73
11.1	Check Power Mode (E5h/98h)	77
11.2	Execute Device Diagnostic (90h)	78
11.3	Format Track (50h: Vendor Specific)	79
11.4	Identify Device (ECh)	82
11.5	Identify Device DMA (EEh)	86
11.6	Idle (E3h/97h)	87
11.7	Idle Immediate (E1h/95h)	88
11.8	Initialize Device Parameters (91h)	89
11.9	Read Buffer (E4h)	90
11.10	Read DMA (C8h/C9h)	91
11.11	Read Long (22h/23h)	93
11.12	Read Multiple (C4h)	95
11.13	Read Sectors (20h/21h)	97
11.14	Read Verify Sectors (40h/41h)	99
11.15	Recalibrate (1xh)	101
11.16	Seek (7xh)	102
11.17	Set Features (EFh)	103
11.18	Set Multiple (C6h)	105
11.19	Sleep (E6h/99h)	106
11.20	S.M.A.R.T. Function Set (B0h)	107
11.20.2	Device Attributes Data Structure	109
11.20.3	Device Attribute Thresholds Data Structure	114
11.20.4	Error Reporting	115
11.21	Standby (E2h/96h)	117
11.22	Standby Immediate (E0h/94h)	118
11.23	Write Buffer (E8h)	119
11.24	Write DMA (CAh/CBh)	120
11.25	Write Long (32h/33h)	122
11.26	Write Multiple (C5h)	124
11.27	Write Sectors (30h/31h)	126
12.0	Timings	129
13.0	Appendix	131
13.1	Commands Support Coverage	131
13.2	SET FEATURES Command Support Coverage	133

Index 135

1.0 General

This document describes the specifications of the following IBM 3.5-inch, ATA interface hard disk drives:

- DAQA-32160 (2160 MB)
- DAQA-32700 (2700 MB)
- DAQA-33240 (3240 MB)

Note: The specifications are subject to change without notice.

1.1 Glossary

<i>Word</i>	<i>Meaning</i>
Kbpi	1 000 Bit Per Inch
Mbps	1 000 000 Bit per second
MB	1 000 000 bytes
KB	1 000 bytes
32 KB	32 x 1 024 bytes
64 KB	64 x 1 024 bytes
Mb/sq.in	1 000 000 bits per square inch
MLC	Machine Level Control
S.M.A.R.T.	Self Monitoring and Analysis Reporting Technology

1.2 General Caution

The drive can be easily damaged by shocks or ESD (Electric Static Discharge), so any damages applied to the drive after taking out from shipping package and opening ESD protective bag are user's responsibilities.

2.0 General Features

- Sector format of 512 bytes/sector
- Closed-loop actuator servo (Embedded Sector Servo)
- Dedicated head landing zone
- Automatic Actuator lock
- Interleave factor 1:1
- Seek time of 9.4 msec in Read Operation
- Size of sector buffer is 96 Kbytes
- Write Cache
- Advanced ECC On The Fly
 - On The Fly correction : 6 Bytes
 - Offline correction : 9 Bytes
- Automatic Error Recovery procedures for read and write commands
- Self Diagnostics on Power on and resident diagnostics
- PIO Data Transfer - Mode 4 (16.6 MB/sec)
- DMA Data Transfer
 - Single Word mode : Mode 2
 - Multiword mode : Mode 2 version / Mode 1 version¹
- CHS and LBA mode
- Transparent Defect Management with ADR (Automatic Defect Reallocation)
- Power Saving modes
- Spindle 5400 rpm
- S.M.A.R.T. function support

¹ See Note 2 in 11.4, “Identify Device (ECh)” on page 82.

Part 1. Functional Specification

3.0 Drive Characteristics

This chapter provides the characteristics of the drives.

3.1 Logical Drive Format

The customer usable data capacity is as shown below.

Descriptions	DAQA-32160	DAQA-32700	DAQA-33240
Logical Head Number	16	16	16
Logical Sectors/Track	63	63	63
Logical Cylinder Number	4200	5248	6296
Logical Sector Size	512	512	512
Total Customer Usable Data Sectors	4 233 600	5 289 984	6 346 368
Total Customer Usable Data Bytes	2160 MB (2,167,603,200)	2700 MB (2,708,471,808)	3240 MB (3,249,340,416)

3.2 Data Sheet

Media transfer rate [Mb/sec]	56.3 - 88.4
Interface transfer rate [MB/sec]	16.6 MB/sec Max
Data buffer size [KB]	96 KB
Rotational speed [RPM]	5400
Average latency [msec]	5.56
Recording density [Kbpi]	120.9 Maximum
Track density [TPI]	7257 Maximum
Areal density [Mb/sq.in.]	878 Maximum
Number of zone	8
Number of disks DAQA-32160	2
DAQA-32700 / DAQA-33240	3
Servo design method	Embedded sector servo

3.3 Performance Characteristics

A file performance is characterized by the following parameters:

- Command Overhead
- Mechanical Positioning
 - Seek Time
 - Latency
- Data Transfer Speed
- Buffering Operation (Lookahead/Write cache)

Note: All the above parameters contribute to file performance. There are other parameters that contribute to the performance of the actual system. This specification tries to define the bare file characteristics, not the system throughput which will depend on the system and the application.

3.3.1 Command Overhead

Command overhead is defined as the time required:

- From the time that the drive is selected
- to the time available for the first data byte of a READ command when the requested data is not in the buffer
- exclude
 - Physical seek time
 - Latency time

Command Case (File is in quiescence state)	Time
Read (Cache not hit)	< 0.6 [msec]
Read (Cache hit)	< 0.02 [msec]
Write	< 0.015 [msec]
Seek	< 0.5 [msec]

Note: The above table gives an average time.

3.3.2 Mechanical Positioning

3.3.2.1 Average Seek Time (Including Settling)

Figure 4. Mechanical Positioning Performance		
Command Type	Typical	Max
Read	8.8 [msec]	9.5 [msec]
Write	9.5 [msec]	10.5 [msec]

“Typical” and “Max” are given throughout the performance specification by;

Typical Average of the drive population tested at nominal environmental and voltage conditions.
Max Maximum value measured on any one drive over the full range of the environmental and voltage conditions. (See 6.2, “Environment” on page 32 and 6.3, “DC Power Requirements” on page 33 for ranges.)

The seek time is measured from the start of actuator's motion to the start of a **reliable read or write operation**. Reliable read or write implies that error correction/recovery is not used to correct arrival problems. The average seek time is measured as the weighted average of all possible seek combinations.

$$\text{Weighted Average} = \frac{\sum_{n=1}^{\max} (\max + 1 - n) (T_{n.in} + T_{n.out})}{(\max + 1) (\max)}$$

Where:

max = Maximum seek length
n = Seek length (1 to max)
Tn.in = Inward measured seek time for an n track seek
Tn.out = Outward measured seek time for an n track seek

3.3.2.2 Single Track Seek Time

Figure 5. Single Track Seek Time		
Function	Typical	Max.
Read [msec]	1.7	2.4
Write [msec]	2.2	2.9

Single track seek is measured as the average of one (1) single track seek from every track with a **random head switch** in both direction (inward and outward).

The single track seek time is the average of the 1000 single track seeks.

3.3.2.3 Full Stroke Seek

Figure 6. Full Stroke Seek Time		
Function	Typical	Max.
Read [msec]	15	18
Write [msec]	15.5	19

Full stroke seek is measured as the average of 1000 full stroke seeks with a **random head switch** from both directions (inward and outward).

3.3.2.4 Cylinder Switch Time (Cylinder Skew)

Figure 7. Cylinder Skew	
	Typical
Cylinder Skew	3.2 [msec]

A cylinder switch time is defined as the amount of time required by the fixed disk access the next sequential block after reading the last sector in the current cylinder.

The measured method is given in 3.3.5, “Throughput” on page 12.

3.3.2.5 Head Switch Time (Head Skew)

Figure 8. Head Skew	
	Typical
Head Skew	2.3 [msec]

3.3.2.6 Average Latency

Figure 9. Latency Time		
Rotation	Time for a revolution	Average Latency
5400 [RPM]	11.1 [msec]	5.56 [msec]

3.3.3 Drive Ready Time

Figure 10. Drive Ready Time		
Condition	Typical	Max.
DAQA-32160	8 [sec]	31 [sec]
DAQA-33240/32700	11 [sec]	31 [sec]

Ready The condition in which the drive is able to perform a media access command (eg. read, write) immediately.

Power On This includes the time required for the internal self diagnostics.

3.3.4 Data Transfer Speed

Figure 11. Data Transfer Speed	
Description	Typical
Disk-Buffer Transfer (Zone 0)	
(Instantaneous)	8.48 [Mbyte/sec]
(Sustained)	6.9 [Mbyte/sec]
Disk-Buffer Transfer (Zone 7)	
(Instantaneous)	5.39 [Mbyte/sec]
(Sustained)	4.4 [Mbyte/sec]
Buffer-Host	16.6 [Mbyte/sec] (Max)

- Instantaneous disk-buffer transfer rate (Mbyte/sec) is derived by:
 $(\text{Number of sectors on a track}) * 512 * (\text{revolution/sec})$

Note: Number of sectors per track will vary because of the linear density recording.

- Sustained disk-buffer transfer rate (Mbyte/sec) is defined by considering head/cylinder change time. This gives a local average data transfer rate. It is derived by:

$$(\text{Sustained Transfer Rate}) = A / (B + C + D)$$

$$A = (\text{Number of data sectors per cylinder}) * 512$$

$$B = ((\text{\# of Surface per cylinder}) - 1) * (\text{Head switch time})$$

$$C = (\text{Cylinder change time})$$

$$D = (\text{\# of Surface}) * (\text{One revolution time})$$

- Instantaneous Buffer-Host Transfer Rate (Mbyte/sec) defines the maximum data transfer rate on AT Bus. It also depends on the speed of the host.

The measurement method is given in 3.3.5, "Throughput" on page 12.

3.3.5 Throughput

3.3.5.1 Simple Sequential Access

Figure 12. Simple Sequential Access Performance (DAQA-32160 case)		
Operation	Typical	Max
Sequential Read/Write (Zone 0)	3.2 [sec]	3.4 [sec]
Sequential Read/Write (Zone 7)	4.7 [sec]	4.9 [sec]

The above table gives the time required to read/write for a total of 8000x consecutive blocks (16,777,216 bytes) accessed by 128 read/write commands. Typical and Max values are given by 105% and 110% of T respectively throughputs following performance description.

Note: Assumes a host system responds instantaneously.

$$T = (A * 128) + B + C + 16,777,216/D + 512/E * 128 + DRQ * 32768 \text{ (READ)}$$

$$T = (A * 128) + B + C + 16,777,216/D + DRQ * 32768 \text{ (WRITE)}$$

where:

T = Calculated Time (sec)

A = Command Process Time (Pre/Post Command overhead)

B = Average Seek Time

C = Average Latency

D = Sustained Disk-Buffer Transfer Rate (Mbyte/sec)

E = Buffer-Host Transfer Rate (Mbyte/sec)

3.3.5.2 Random Access

Figure 13. Random Access Performance		
Operation	Typical	Max
Random Read	65 [sec]	68 [sec]
Random Write	67 [sec]	70 [sec]

The above table gives the time required to execute a total of 1000x read/write commands which access a random LBA.

$$T = (A + B + C + 512/D + 512/E + DRQ) * 4096 \text{ (READ)}$$

$$T = (A + B + C + 512/D) * 4096 \text{ (WRITE)}$$

where:

T = Calculated Time (sec)

A = Command Process Time (Pre/Post Command overhead)

B = Average Seek Time

C = Average Latency

D = Sustained Disk-Buffer Transfer Rate (Mbyte/sec)

E = Buffer-Host Transfer Rate (Mbyte/sec)

DRQ = Data ReQuest interval (micro second)

3.3.6 Operating Mode Definition

Operating Mode	Description
Spin-Up	Start up time period from spindle stop or power down.
Seek	Seek operation mode
Write	Write operation mode
Read	Read operation mode
Idle	Spindle motor and servo system are working normally. Commands can be received and processed immediately.
Standby	Spindle motor is stopped. Commands can be received immediately, but write or read operations cannot begin until the spindle is spun-up and the Servo system is ready.

Notes:

1. Upon Power down or Spindle stopped, a head locking mechanism will secure the heads in the ID parking position.
2. Recovering from Standby mode does not need soft reset nor hard reset.
3. Sleep command is handled as Standby command.

3.3.6.1 Mode Transition Time

Figure 14. Mode Transition Time			
From	To	Typical	Max
Standby	Idle	10 [sec]	16 [sec]
Idle	Standby	Immediate	N/A

Note: The actual spin down time will exist, however the command will be processed immediately.

4.0 Data Integrity

4.1 Data loss at Power Off

- The drive retains recorded data under all non-write operation.
- No more than one sector can be lost by power down during write operation while write cache is disabled.
- Power off during write operation may make an incomplete sector which will report hard data error when read. The sector can be recovered by a re-write operation.
- Hard reset does not cause any data loss.

4.2 Write Cache

- Power off while write cache is enabled may cause loss of data which are remaining in the cache and have not been flushed onto the disk media.
This means that there is a possibility that power off even after write command completion may cause loss of data.
- There are three ways to check if all data in the write cache have been flushed onto the disk. Checking just before power off is recommended to prevent data loss.
 - To confirm negation of -DASP signal.
 - To confirm successful completion of Software Reset.
 - To confirm successful completion of Check Power Mode commands.

4.3 Equipment Status

Equipment status is available to the host system any time the drive is not ready to read, write, or seek. This status normally exists at power-on time and will be maintained until the following conditions are satisfied:

- Access recalibration/tuning is complete.
- Spindle speed meets requirements for reliable operation.
- Self-check of drive is complete.

Appropriate error status is made available to the host system if any of the following conditions occur after the drive has once become ready:

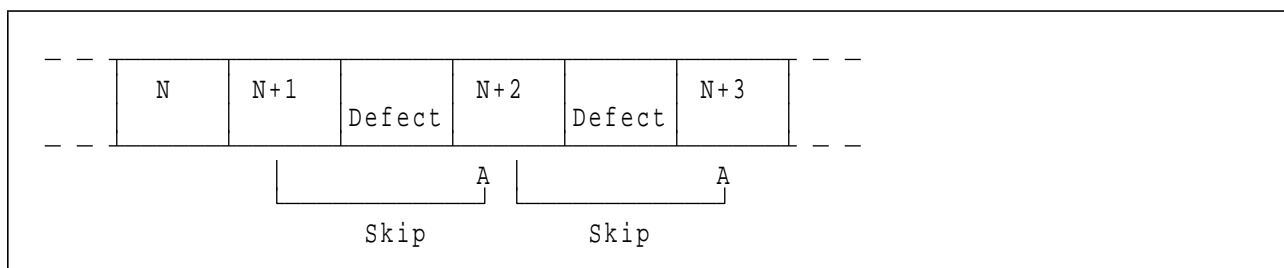
- Spindle speed outside requirements for reliable operation.
- Occurrence of a WRITE FAULT condition.

5.0 Physical Format

Media defects are remapped to the next available sector during Format Process in manufacturing. The mapping from LBA to the physical locations is calculated by an internal maintained table.

5.1 Shipped Format

- Data areas are optimally used.
- No extra sector is wasted as a spare throughout user data areas.
- All pushes generated by defects are absorbed by spare tracks of inner zone.



Defects are skipped without any constraint, such as track or cylinder boundary. The calculation from LBA to physical is done automatically by internal table.

6.0 Specification

6.1 Electrical interface specification

6.1.1 Connectors

6.1.1.1 Power

The DC power connector is designed to mate with AMP (part 1-480424-0) using AMP pins (part 350078-4) strip or (part 61173-4) loose piece, or their equivalents. Pin assignments are shown below.

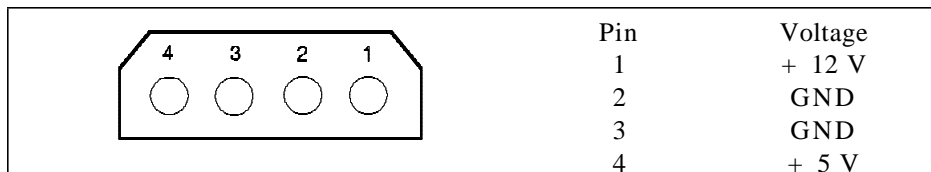


Figure 15. Power Connector Pin Assignments

6.1.1.2 AT Signal Connector

The AT signal connector is a 40-pin connector.

6.1.2 Signal Definition

The pin assignments of interface signals are listed as follows:

PIN	SIGNAL	I/O	Type	PIN	SIGNAL	I/O	Type
01	-RESET	I	TTL	02	GND		
03	DD07	I/O	3-state	04	DD08	I/O	3-state
05	DD06	I/O	3-state	06	DD09	I/O	3-state
07	DD05	I/O	3-state	08	DD10	I/O	3-state
09	DD04	I/O	3-state	10	DD11	I/O	3-state
11	DD03	I/O	3-state	12	DD12	I/O	3-state
13	DD02	I/O	3-state	14	DD13	I/O	3-state
15	DD01	I/O	3-state	16	DD14	I/O	3-state
17	DD00	I/O	3-state	18	DD15	I/O	3-state
19	GND			(20)	Key		
21	DMARQ	0	3-state	22	GND		
23	-DIOW	I	TTL	24	GND		
25	-DIOR	I	TTL	26	GND		
27	IORDY	0	OC	28	CSEL	I	TTL
29	-DMACK	I	TTL	30	GND		
31	INTRQ	0	3-state	32	-HIOCS16	0	OC
33	DA01	I	TTL	34	-PDIAG	I/O	OC
35	DA00	I	TTL	36	DA02	I	TTL
37	-CS0	I	TTL	38	-CS1	I	TTL
39	-DASP	I/O	OC	40	GND		

Figure 16. Table of signals

Notes:

1. "O" designates an output from the Drive.
2. "I" designates an input to the Drive.
3. "I/O" designates an input/output common.
4. "OC" designates Open-Collector or Open-Drain output.

- DD00-DD15** 16-bit bi-directional data bus between the host and the HDD. The lower 8 lines, DD00-07, are used for Register and ECC access. All 16 lines, DD00-15, are used for data transfer. These are 3-State lines with 24 mA current sink capability.
- DA00-DA02** Address used to select the individual register in the HDD.
- CS0** Chip select signal generated from the Host address bus. When active, one of the Command Block Registers (Data, Error{Features when written}, Sector Count, Sector Number, Cylinder Low, Cylinder High, Drive/Head and Status{Command when written} register) can be selected.
(See Figure 21 on page 28.)
- CS1** Chip select signal generated from the Host address bus. When active, one of the Control Block Registers (Alternate Status{Device Control when written} and Drive Address register) can be selected.
(See Figure 21 on page 28.)
- RESET** This line is used to reset the HDD. It shall be kept Low logic state during power up and kept High thereafter.
- DIOW** Its rising edge holds data from the host data bus to a register or data register of the HDD.
- DIOR** When low, this signal enables data from a register or data register of the drive onto data bus. The data on the bus shall be latched on the rising edge of -DIOR.
- INTRQ** Interrupt is enabled only when the drive is selected, and the host activates the -IEN bit in the Device Control Reg. Otherwise, this signal is in high impedance state regardless of the state of the IRQ bit. The interrupt is set when the IRQ bit is set by the drive CPU. IRQ is reset to zero by a host read of the status register or a write to the Command Reg. This signal is a 3-State line with 24 mA sink capability.
- HIOCS16** Indication to the host that a 16-bit wide data register has been addressed and that the drive is prepared to send or receive a 16-bit wide data word. This signal is an Open-Drain output with 24 mA sink capability and an external resistor is needed to pull this line to 5 volts.
- DASP** This is a time-multiplexed signal which indicates that a drive is active, or that device 1 is present. This signal is driven by Open-Drain driver and internally pulled-up to 5 volts through a 10k Ω resistor.
During Power-On initialization or after -RESET is negated, -DASP shall be asserted by Device 1 within 400 msec to indicate that device 1 is present. Device 0 shall allow up to 450msec for device 1 to assert -DASP. If device 1 is not present, device 0 may assert -DASP to drive a LED indicator.
-DASP shall be negated following acceptance of the first valid command by device 1. Anytime after negation of -DASP, either drive may assert -DASP to indicate that a drive is active.
- PDIAG** This signal shall be asserted by device 1 to indicate to device 0 that it has completed diagnostics. This line is pulled-up to 5 volts in the HDD through a 10k Ω resistor.
Following a Power On Reset, software reset or -RESET, drive 1 shall negate -PDIAG within 1 msec (to indicate to device 0 that it is busy). Drive 1 shall then assert -PDIAG within 30 seconds to indicate that it is no longer busy, and is able to provide status.
Following the receipt of a valid Execute Drive Diagnostics command, device 1 shall negate -PDIAG within 1 msec to indicate to device 0 that it is busy and has not yet passed its drive diagnostics. If device 1 is present then device 0 shall wait up to 6 seconds from the receipt of a valid Execute Drive Diagnostics command for drive 1 to assert -PDIAG. Device 1 should clear BSY before asserting -PDIAG, as -PDIAG is used to indicate that device 1 has passed its diagnostics and is ready to post status.
If -DASP was not asserted by device 1 during reset initialization, device 0 shall post its own status immediately after it completes diagnostics, and clear the device 1 Status register to

00h. Device 0 may be unable to accept commands until it has finished its reset procedure and is ready (DRDY=1).

CSEL (Cable Select) (Optional)

The drive is configured as either Device 0 or 1 depending upon the value of CSEL.

- If CSEL is grounded then the device address is 0.
- If CSEL is open then the device address is 1.

KEY

Pin position 20 has no connection pin. It is recommended to close the respective position of the cable connector in order to avoid incorrect insertion by mistake.

IORDY

This signal is negated to extend the host transfer cycle when a drive is not ready to respond to a data transfer request, and may be negated when the host transfer cycle is less than 240 nsec for PIO data transfer. This signal is an open-drain output with 24 mA sink capability and an external resistor is needed to pull this line to 5 volts.

-DMACK

This signal shall be used by the host in response to DMARQ to either acknowledge that data has been accepted, or that data is available. This line is internally pulled-up to 5 Volts through 15 k Ω +100%, -50% resistor.

DMARQ

This signal, used for DMA data transfers between host and drive, shall be asserted by the drive when it is ready to transfer data to or from the host. The direction of data transfer is controlled by -HIOR and -HIOW. This signal is used on a handshake manner with -DMACK. This signal is a 3-state line with 24mA sink capability and internally pulled-down to GND through 10 k Ω resistor.

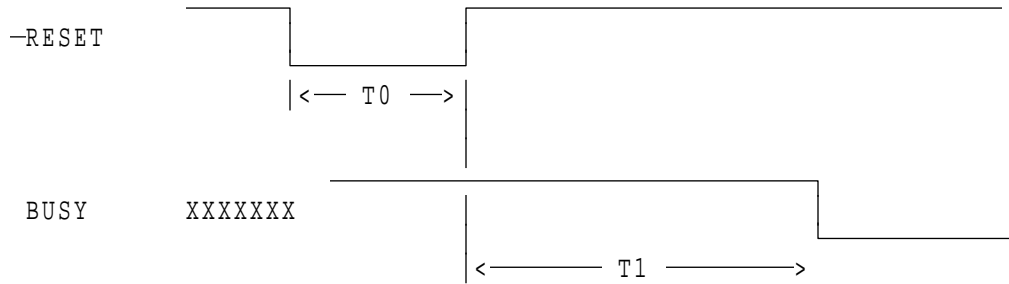
6.1.3 Interface Logic Signal Levels

The interface logic signal has the following electrical specifications:

Inputs :	Input High Voltage	—	2.0 V min.
	Input Low Voltage	—	0.8 V max.
Outputs :	Output High Voltage	—	2.4 V min.
	Output Low Voltage	—	0.5 V max.

6.1.4 Reset Timings

HDD reset timing.

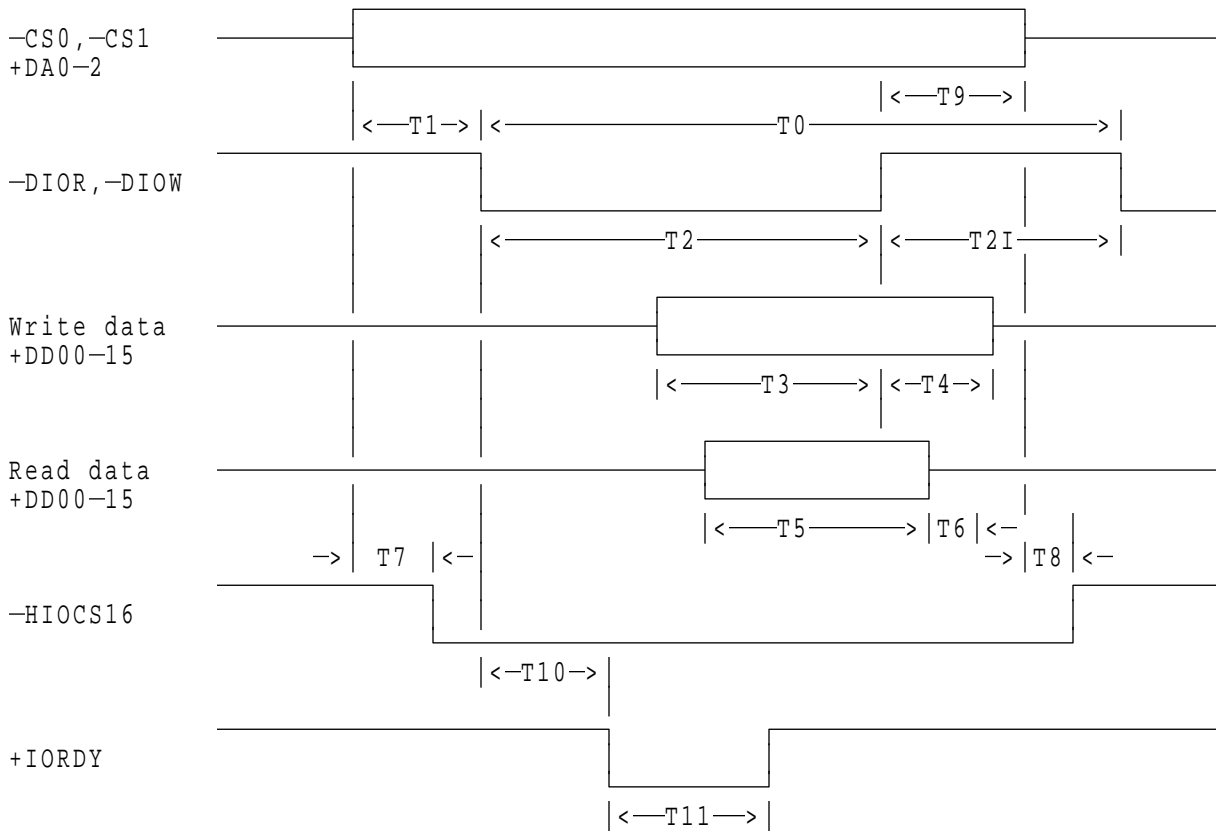


	PARAMETER DESCRIPTION	Min (usec)	Max (sec)
T0	<code>-RESET</code> low width	25	
T1	<code>-RESET</code> high to not <code>BUSY</code>	—	31

Figure 17. System Reset timing

6.1.5 PIO Timings

The PIO cycle timings meet Mode 4 of the ATA-3 description.



	PARAMETER DESCRIPTION	MIN (nsec)	MAX (nsec)	Note
T0	Cycle time	120	—	
T1	$\overline{\text{CS0-1}}, +\text{DA00-02}$ valid to $\overline{\text{DIOR}}, \overline{\text{DIOW}}$ active	25	—	
T2	$\overline{\text{DIOR}}, \overline{\text{DIOW}}$ pulse width	70	—	
T2I	$\overline{\text{DIOR}}, \overline{\text{DIOW}}$ recovery	25	—	
T3	$+\text{DD00-15}$ setup to $\overline{\text{DIOW}}$ high	20	—	
T4	$\overline{\text{DIOW}}$ high to $+\text{DD00-15}$ hold	10	—	
T5	$+\text{DD00-15}$ setup to $\overline{\text{DIOR}}$ high	20	—	
T6	$\overline{\text{DIOR}}$ high to $+\text{DD00-15}$ hold	5	—	
T7	$\overline{\text{CS0-1}}, +\text{DA00-02}$ valid to $\overline{\text{HIOCS16}}$ assertion	—	30	
T8	$\overline{\text{CS0-1}}, +\text{DA00-02}$ invalid to $\overline{\text{HIOCS16}}$ negation	—	30	
T9	$\overline{\text{DIOR}}, \overline{\text{DIOW}}$ high to $\overline{\text{CS0-1}}, +\text{DA00-02}$ hold	10	—	
T10	$\overline{\text{DIOR}}, \overline{\text{DIOW}}$ low to $+\text{IORDY}$ low	—	35	
T11	$+\text{IORDY}$ pulse width	—	1250	

Figure 18. PIO cycle timings

6.1.5.1 Write DRQ Interval Time

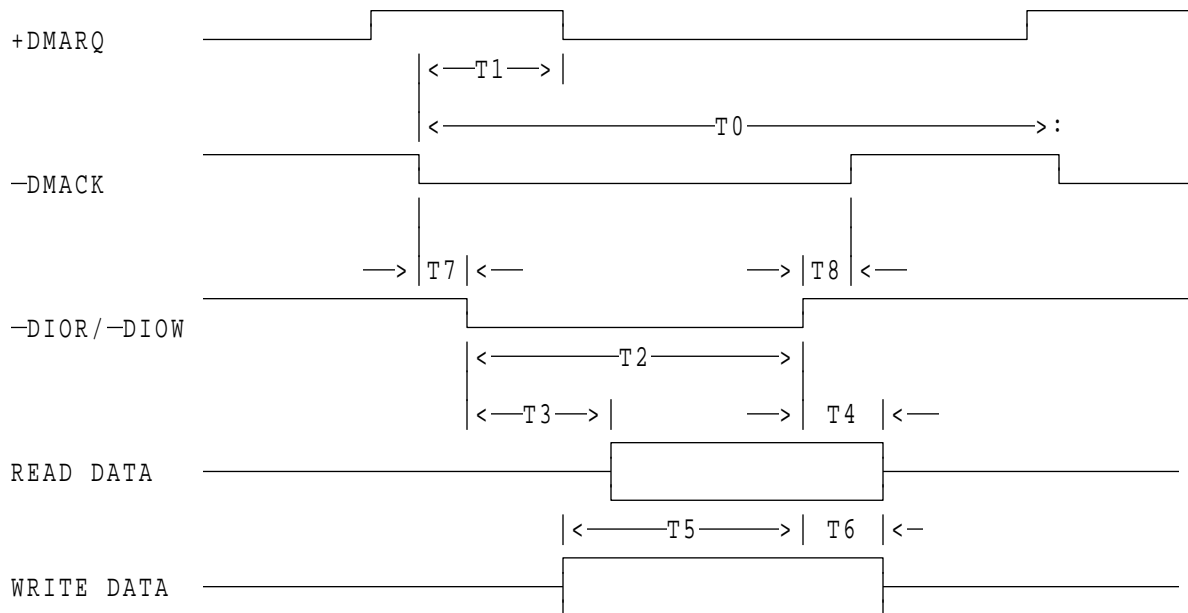
For write sectors and write multiple operations, 16 μ sec is inserted from the end of negation of the DRQ bit until setting of the next DRQ bit.

6.1.5.2 Read DRQ Interval Time

For read sectors and read multiple operations, the interval from the end of negation of the DRQ bit until setting of the next DRQ bit is 16 μ sec.

6.1.6 DMA Timings (Single Word)

The Single Word DMA timing meets Mode 2 of the ATA-2 description.

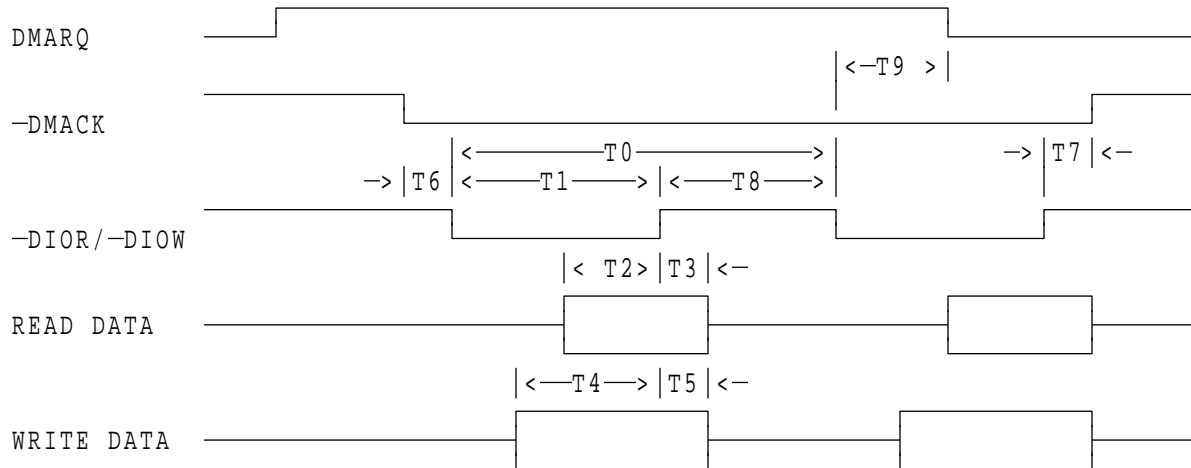


	PARAMETER DESCRIPTION	MIN (nsec)	MAX (nsec)	Note
T0	Cycle time	240	—	
T1	-DMA active to +DMARQ inactive	—	80	
T2	-DIOR, -DIOW pulse width	120	—	
T3	-DIOR data access	—	60	
T4	-DIOR data hold	5	—	
T5	-DIOW data setup	35	—	
T6	-DIOW data hold	20	—	
T7	-DMACK to -DIOR/-DIOW setup	0	—	
T8	-DIOR/-DIOW to -DMACK hold	0	—	

Figure 19. DMA (Single Word) cycle timings

6.1.7 DMA Timings (Multiword)

- | DAQA-3xxxx has two versions on Multiword DMA.
- | • Multiword DMA Mode 2 support version. (minimum cycle time 120ns)
 - | • Multiword DMA Mode 1 support version. (minimum cycle time 240ns)



	PARAMETER DESCRIPTION	MIN (nsec)	MAX (nsec)	
T0	Cycle time	120 / 240	—	Note
T1	-DIOR,-DIOW pulse width	70	—	
T2	-DIOR data setup	20	—	
T3	-DIOR data hold	5	—	
T4	-DIOW data setup	20	—	
T5	-DIOW data hold	10	—	
T6	-DMACK to -DIOR/-DIOW setup	0	—	
T7	-DIOR/-DIOW to -DMACK hold	5	—	
T8	-DIOR/-DIOW negated pulse width	25	—	
T9	-DIOR/-DIOW to -DMARQ delay	—	35	

Figure 20. DMA (Multi Word) cycle timings

- | **Note:** The cycle time is specified in word 65 of Identify Device data.
 | See 11.4, “Identify Device (ECh)” on page 82 for details.

6.1.8 Addressing of HDD Registers

The host addresses the drive through a set of registers called the Task File. These registers are mapped into the host's I/O space. Two chip select lines (-CS0 and -CS1) and three address lines (DA00-02) are used to select one of these registers, while a -DIOR or -DIOW is provided at the specified time.

The -CS0 is used to address Command Block registers. while the -CS1 is used to address Control Block registers.

The following table shows the I/O address map.

-CS0	-CS1	DA02	DA01	DA00	-DIOR = 0 (Read)	-DIOW = 0 (Write)
					Command Block Registers	
0	1	0	0	0	Data Reg.	Data Reg.
0	1	0	0	1	Error Reg.	Features Reg.
0	1	0	1	0	Sector count Reg.	Sector count Reg.
0	1	0	1	1	Sector number Reg.	Sector number Reg
0	1	1	0	0	Cylinder low Reg.	Cylinder low Reg.
0	1	1	0	1	Cylinder high Reg.	Cylinder high Reg.
0	1	1	1	0	Drive/Head Reg.	Drive/Head Reg.
0	1	1	1	1	Status Reg.	Command Reg.
					Control Block Registers	
1	0	1	1	0	Alt. Status Reg.	Device control Reg
1	0	1	1	1	Drive address Reg.	-

Figure 21. Task File

Note: "Addr." field is shown just as an example.

During DMA operation (from writing to the command register until an interrupt), all registers are not accessible.

For example, the host is not supposed to read status register contents before interrupt (the value is invalid).

6.1.9 Cabling

The maximum cable length from the host system to the HDD plus circuit pattern length in the host system shall not exceed 18 inches.

For higher data transfer application(>8.3MB/sec), the cable length should be shorter than 18 inches since data transfer characteristics depends on the driver circuits of the system and hard drive, and/or cabling.

6.1.10 Jumper Settings

The 7 positions jumper block shown below is used to select Device 0 or Device 1, Cable Selection and Write Cache.

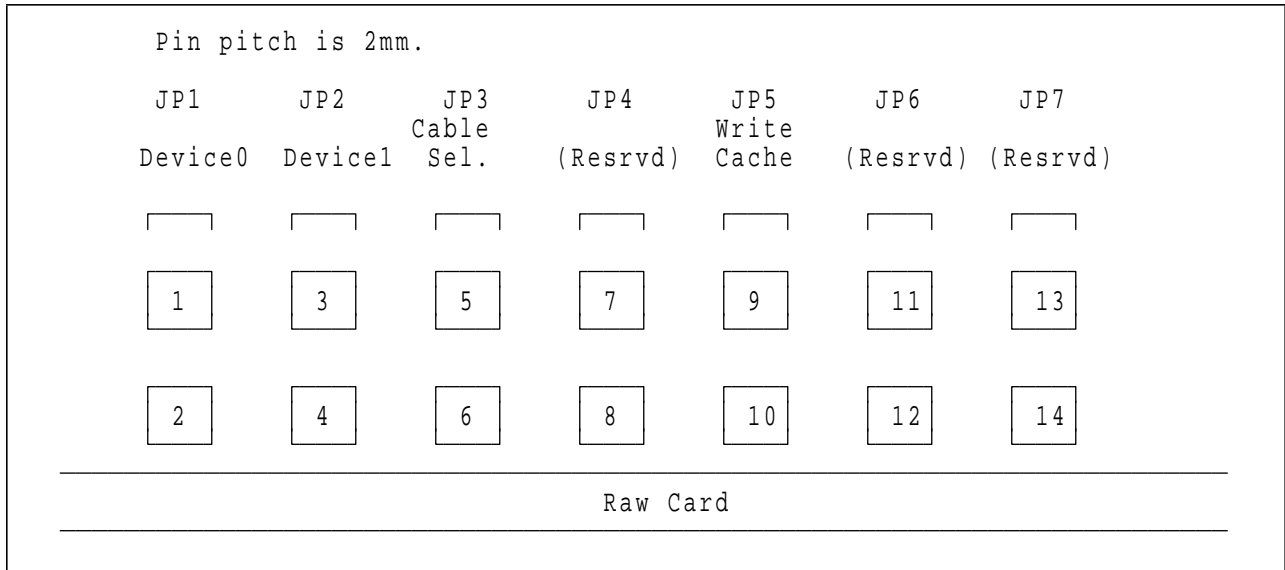


Figure 22. Jumper Pins

Notes:

1. The jumper position of JP1, 2, and 3 should not be selected concurrently.
2. JP1 is the position for Device0, JP2 is for Device1, and JP3 is for Cable Selection mode.
3. To enable the CSEL mode (cable selection mode), the JP3 jumper must be installed. In the CSEL mode, the drive address is determined as follows:
 - When CSEL is grounded or at a low level, the drive address is 0 (Device0).
 - When CSEL is open or at a high level, the drive address is 1 (Device1).
4. When JP5 jumper is installed, write cache function is disabled.

6.1.10.1 The Pin Assignment

JP#	Pin #	Status	Description
1	1	—	GND
	2	In	-Device Address Select Line
2	3	—	NC (Device1 Position)
	4	—	NC
3	5	In	Cable Selection (28 PIN)
	6	In	-Device Address Select Line
4	7	—	GND
	8	—	(Reserved)
5	9	—	GND
	10	In	+Write Cache ON (If Open)
6	11	—	GND
	12	—	(Reserved)
7	13	—	GND
	14	—	(Reserved)

Figure 23. Jumper Pins Assignment

6.1.10.2 Shipping Default Condition

The default shipping conditions are, device ID set to Device 0, write cache on and auto reallocation on.

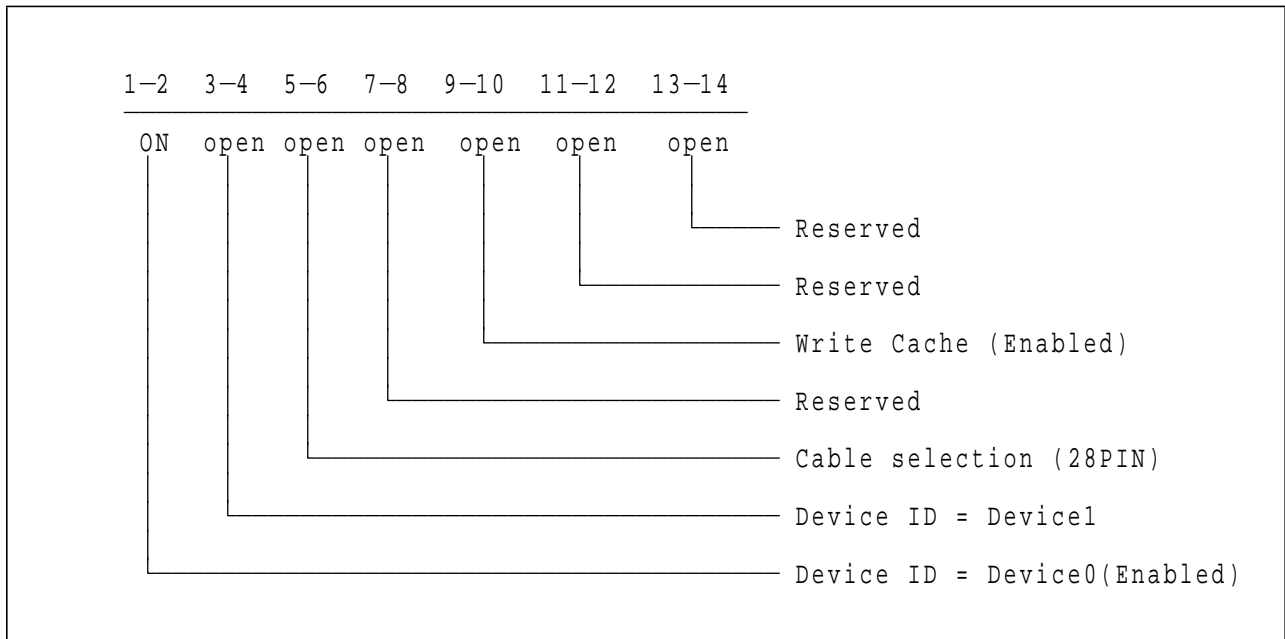


Figure 24. AT Jumper Default Condition

6.1.10.3 Mechanical Outline

The card with disk enclosure mechanical outline is as follows.

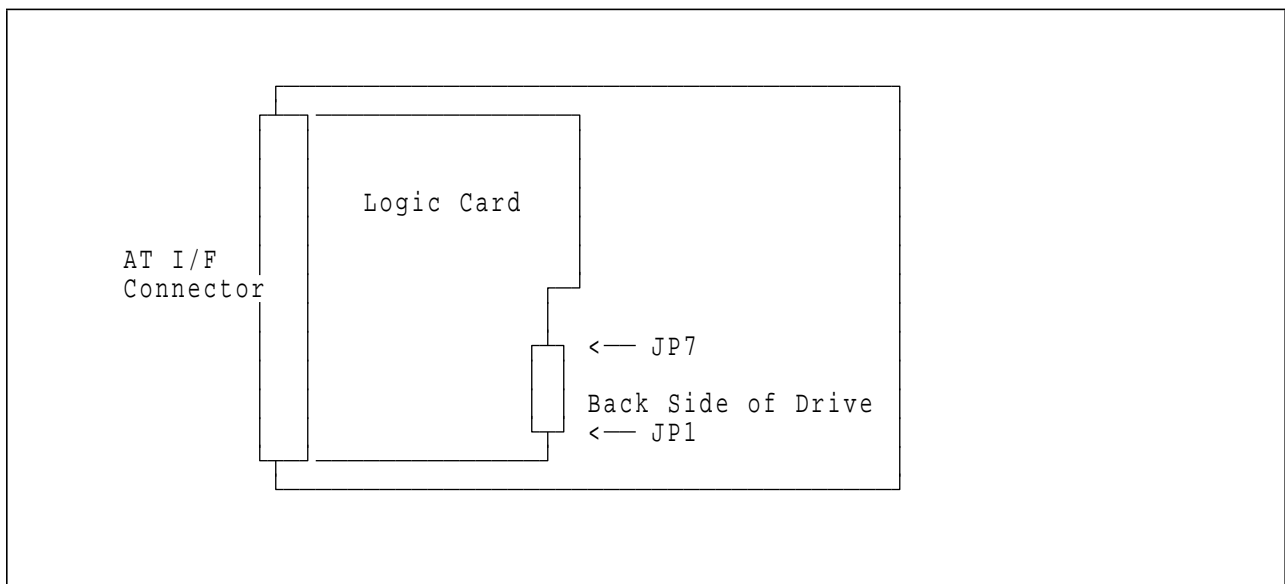


Figure 25. Mechanical Outline

6.2 Environment

Figure 26. Environmental Condition	
Operating Conditions	
Temperature	5 to 55[°C] (See note)
Relative Humidity	8 to 90 [% RH] non-condensing
Maximum Wet Bulb Temperature	29.4[°C] non-condensing
Maximum Temperature Gradient	15[°C / Hour]
Altitude	– 300 to 3048 [m]
Non-Operating Conditions	
Temperature	– 40 to 65[°C]
Relative Humidity	5 to 95 [% RH] non-condensing
Maximum Wet Bulb Temperature	35[°C] non-condensing
Maximum Temperature Gradient	15[°C / Hour]
Altitude	– 300 to 12,000 [m]
Note:	
The system has to provide sufficient ventilation to maintain a surface temperature below 60[°C] at the center of the top cover of the drive.	
Non-operating condition should not continue beyond one year.	

6.3 DC Power Requirements

Connection to the product should be made in isolated secondary circuits (SELV). The following voltage specification is applied at the power connector of the drive. Damage to the file electronics may result if the power supply cable is connected or disconnected while power is being applied to the file (**Hot plug/unplug is not allowed**). There is no special power on/off sequencing required.

Figure 27. Input Voltage		
	During run and spin up	Absolute max voltage
+ 5 Volts Supply	5V +/- 5%	7V
+12 Volts Supply	12V +10% , - 8%	15V

Figure 28. Power Supply Current of DAQA-33240 / DAQA-32700					
(All values in Amps.)	+5Volts		+12Volts		Total (W)
	Pop Mean	Std.Dev	Pop Mean	Std.Dev	
Idle Average	0.15	0.03	0.21	0.03	3.3
Idle ripple (peak-to-peak)	0.30	0.03	0.30	0.04	
Seek peak (*1)	0.35	0.06	0.90	0.15	
Seek average (*1)	0.19	0.06	0.31	0.03	4.7
Start up (max)	0.46	0.06	1.10	0.12	
RND R/W peak (*2)	0.50	0.04	0.90	0.18	
RND R/W average (*2)	0.30	0.04	0.30	0.03	5.1
Standby/Sleep average	0.10	0.02	0.01	0.02	0.6

Figure 29. Power Supply Current of DAQA-32160					
(All values in Amps.)	+5Volts		+12Volts		Total (W)
	Pop Mean	Std.Dev	Pop Mean	Std.Dev	
Idle Average	0.15	0.03	0.16	0.03	2.7
Idle ripple (peak-to-peak)	0.30	0.03	0.30	0.04	
Seek peak (*1)	0.35	0.06	0.90	0.15	
Seek average (*1)	0.19	0.06	0.27	0.03	4.2
Start up (max)	0.46	0.06	1.10	0.12	
RND R/W peak (*2)	0.50	0.04	0.90	0.18	
RND R/W average (*2)	0.30	0.04	0.26	0.03	4.6
Standby/Sleep average	0.10	0.02	0.01	0.02	0.6

Notes:

1. Random Seeks at 40% duty cycle.
2. Seek Duty = 30%, W/R Duty = 45%, Idle Duty = 25%.

Figure 30. Power Supply Generated Ripple as seen at file power connector		
	Maximum	Notes
+5 V DC	100 [mV pp]	0-10 [MHz]
+12 V DC	150 [mV pp]	0-10 [MHz]

During file start up and seeking, 12 volt ripple is generated by the file (referred to as dynamic loading). If several files have their power daisy chained together then the power supply ripple plus other file's dynamic loading must remain within the regulation tolerance of +10/-8%. A common supply with separate power leads to each file is a more desirable method of power distribution.

To prevent external electrical noise from interfering with the file's performance, the file must be held by four screws in a user system frame which has no electrical level difference at the four screws position, and has less than +/-300 millivolts peak to peak level difference to the file power connector ground.

6.4 Reliability

6.4.1 Contact Start Stop (CSS)

The drive is designed to withstand a minimum of 40,000 contact start/stop cycles under 40°C.

6.4.2 Preventive Maintenance

None.

6.4.3 Data Reliability

- Probability of not recovering data 1 in 10^{13} bits read
- ECC implementation
 - On-The-Fly correction, performed as a part of read channel function, recovers up to 6 symbols of error in 1 sector. (1 symbol is 8 bits.)
 - Off-line correction, performed as a part of retry procedure in the drive, recovers up to 9 symbols of error in 1 sector.

6.4.4 Cable Noise Interference

To avoid any degradation of performance throughput or error when the interface cable is routed on top or comes in contact with the HDA assembly, the drive must be grounded electrically to the system frame by four screws. The common mode noise or voltage level difference between the system frame and power cable ground or AT interface cable ground should be in the allowable level specified in the power requirement section.

6.5 Mechanical Specifications

6.5.1 Outline

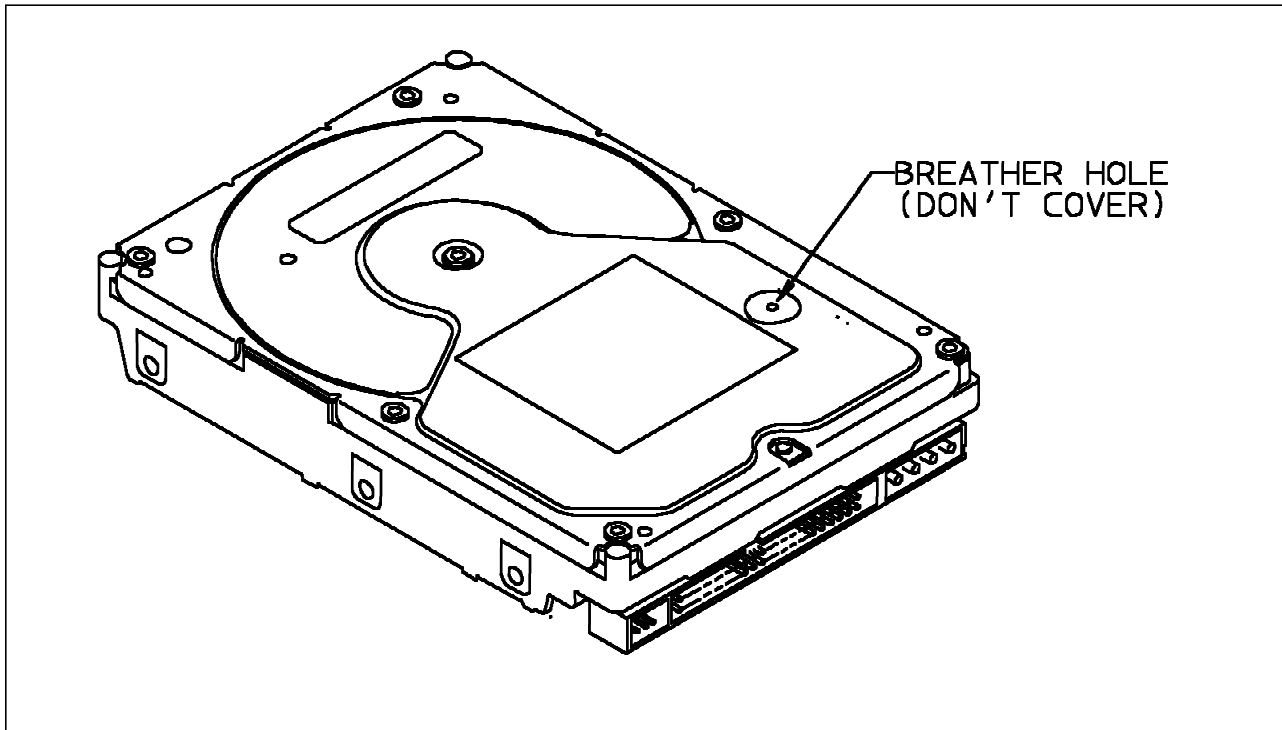


Figure 31. Outline of DAQA-32160/32700/33240

6.5.2 Mechanical Dimensions and Weight

The following chart describes the dimensions for the 3.5" hard disk drive form factor.

	DAQA-32160/32700/33240	
Height (mm)		25.4 ± 0.4
Width (mm)		101.6 ± 0.4
Length (mm)		146.0 ± 0.6
Weight (gram)		610 Max

Figure 32. Physical Dimension and Weight

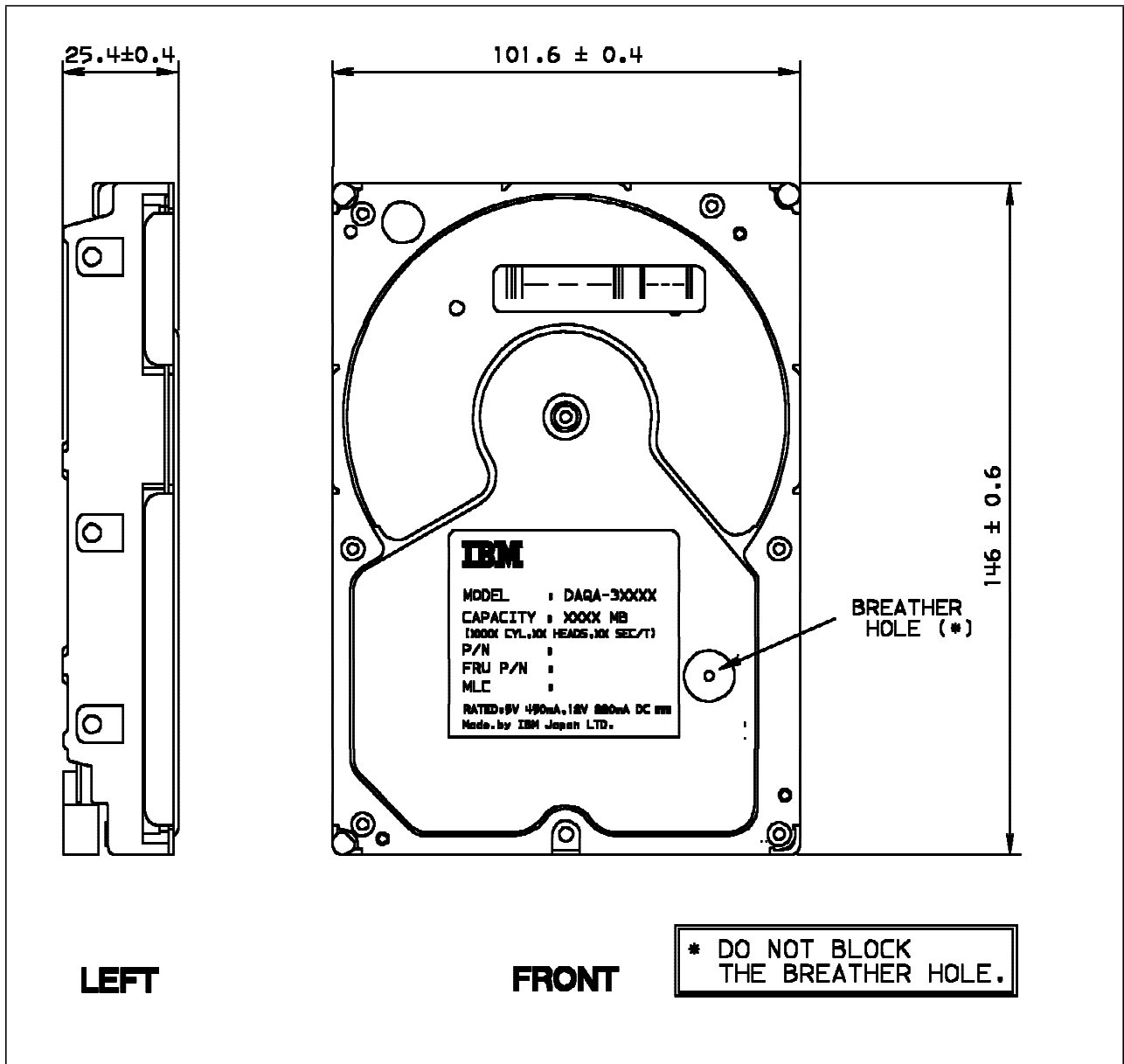


Figure 33. Mechanical Dimension

6.5.3 Connector Locations

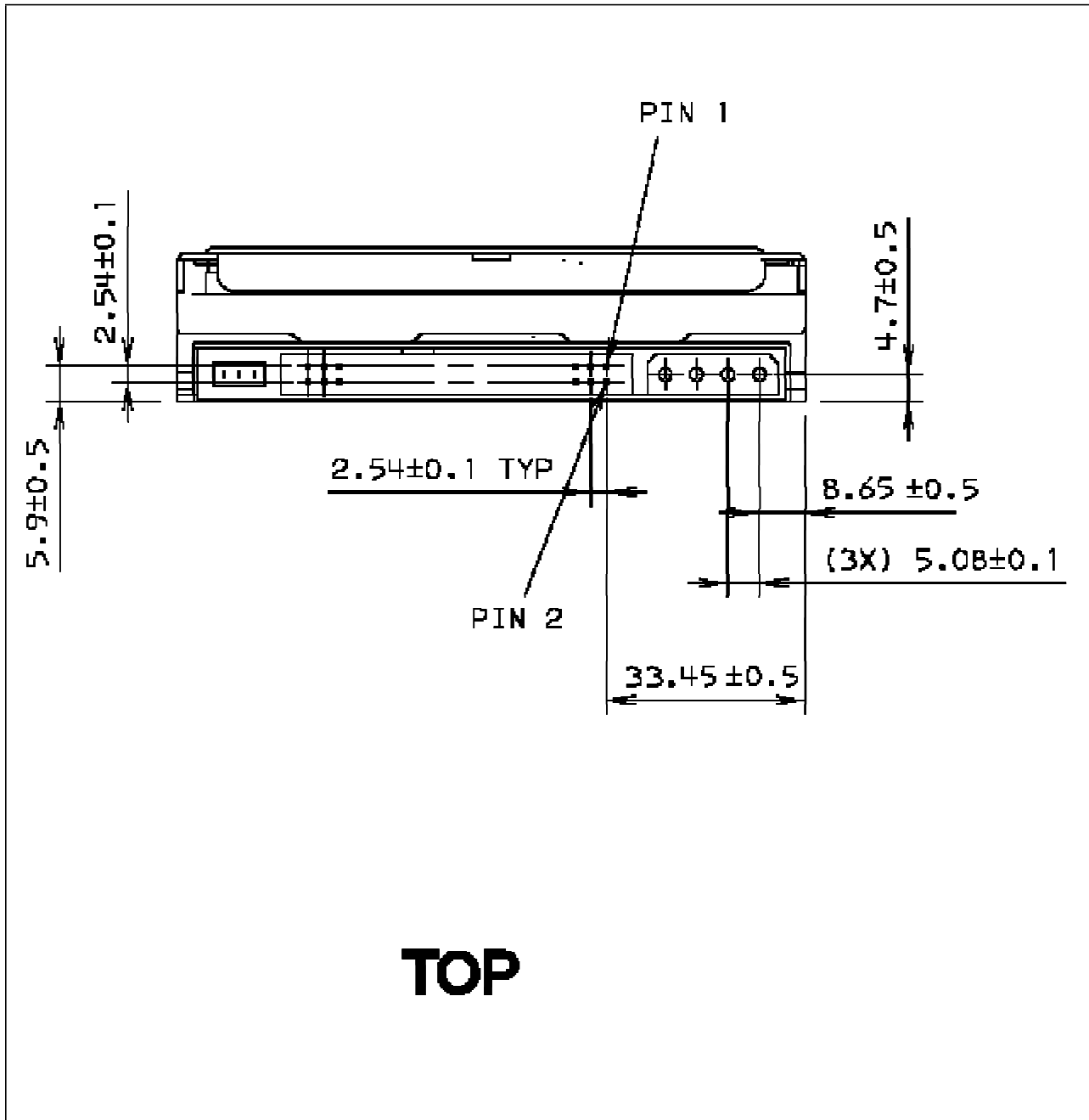


Figure 34. Connector Locations

6.5.4 Hole Locations

The Figure 35 on page 39 shows the outline of DAQA-32160/32700/33240 which includes the hole locations.

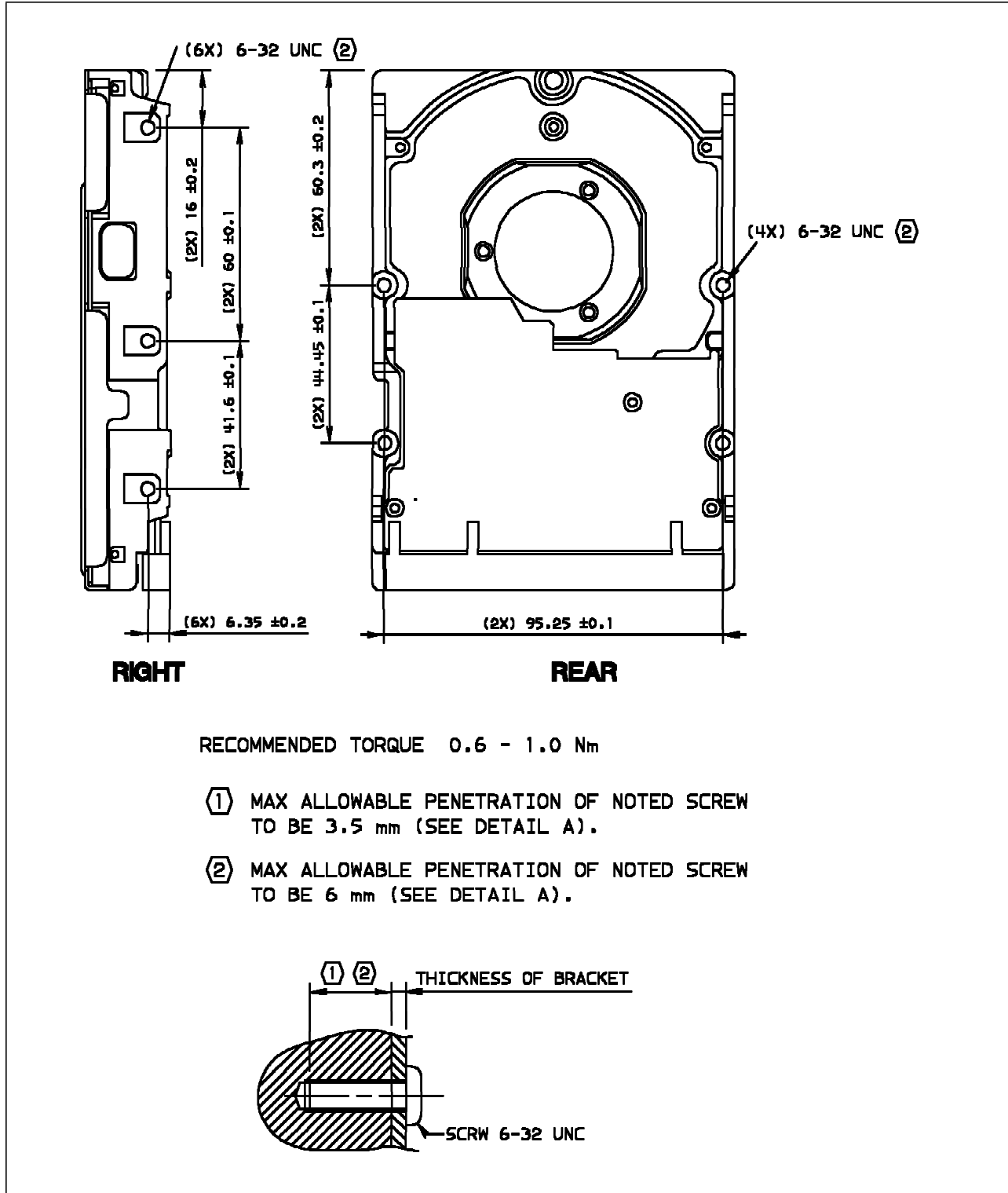


Figure 35. Mounting Positions and the Tappings

6.5.5 Mounting Orientation

The drive will operate in all axes (6 directions). The drive will operate within the specified error rates when tilted ± 5 degree from these positions.

Performance and error rate will stay within specification limits if the drive is operated in the other permissible orientations from which it was formatted. Thus a drive formatted in a horizontal orientation will be able to run vertically and vice versa.

The recommended mounting **screw torque** is **0.6 - 1.0** [Nm] (6 - 10 [Kgf.cm]).

The recommended mounting screw depth is 6 [mm] Max for bottom and 3.5 [mm] Max for horizontal mounting.

The system is responsible for mounting the drive securely enough to prevent from excessive motion or vibration of the drive at seek operation or spindle rotation, using appropriate screws or equivalent mounting hardware.

Vibration test and shock test are to be conducted by mounting the drive to the table using bottom four screws.

6.5.6 Shipping Zone and Lock

A "shipping" (or "landing") zone on the disk, not on the data area of the disk, is provided to protect the disk data during shipping, movement, or storage. Upon power down, a head locking mechanism will secure the heads in this zone. See Non-Operating Shock section for additional details.

6.6 Vibration and Shock

All vibration and shock measurements in this section shall be for the disk drive without the mounting attachments for the systems. The input level shall be applied to the normal drive mounting points.

6.6.1 Operating Vibration

6.6.1.1 Random Vibration

The test is 30 minutes of random vibration using the power spectral density (PSD) levels shown below in each of three mutually perpendicular axes. The disk drive will operate without non-recoverable errors when subjected to the above random vibration levels.

Figure 36. Random vibration PSD profile breakpoints (Operating)									
5	17	45	48	62	65	150	200	500	Hz
0.02	1.1	1.1	8.0	8.0	1.0	1.0	0.5	0.5	$\times 10^{-3} \text{ G}^2/\text{Hz}$
Note: Overall RMS (root mean square) level of vibration is 0.67 G rms.									

6.6.1.2 Swept Sine Vibration

The hard disk drive will meet the criteria shown below while operating in respective conditions.

No errors 0.5 G 0-peak, 5-300-5 Hz sine wave, 0.5 oct/min sweep rate
with 3 minutes dwells at 2 major resonances

No data loss 1 G 0-peak, 5-300-5 Hz sine wave, 0.5 oct/min sweep rate
with 3 minutes dwells at 2 major resonances

6.6.2 Non-Operating Vibration

The disk drive does not sustain permanent hardware damage or loss of previously recorded data after being subjected to the environment described below.

6.6.2.1 Random Vibration

The test consists of a random vibration applied in each of three mutually perpendicular axes with the time duration of 10 minutes per axis. The PSD levels for the test simulating the shipping and relocation environment is shown below.

Figure 37. Random vibration PSD profile breakpoints (Non-operating)							
2	4	8	40	55	70	200	Hz
0.001	0.03	0.03	0.003	0.01	0.01	0.001	G^2/Hz
Note: Overall RMS (root mean square) level of vibration is 1.04 G rms.							

6.6.2.2 Swept Sine Vibration

- 2 G 0-peak, 5-500-5 Hz sine wave
- 0.5 oct/min sweep rate
- 3 minutes dwells at 2 major resonances

6.6.3 Operating Shock

The hard disk drive meets the following criteria while operating in respective conditions described below. The shock test consists of ten shocks inputs in each axis and direction for total of 60. There must be a delay between shock pulses, long enough to allow the drive to complete all necessary error recovery procedure.

No errors 5 G, 11 ms half-sine shock pulse

No data loss, seek errors or permanent damage
10 G, 11 ms half-sine shock pulse

No data loss or permanent damage
15 G, 5 ms half-sine shock pulse
30 G, 4 ms half-sine shock pulse

6.6.4 Non-Operating Shock

The drive will operate with no degradation of performance or permanent damage after subjected to shock pulses with the following characteristics.

6.6.4.1 Trapezoidal Shock Wave

- Approximate square (trapezoidal) pulse shape.
- Approximate rise and fall time of pulse = 1 ms.
- Averaged acceleration level = 50 G.
(Averaged response curve value during the time following the 1 ms rise time and before the 1 ms fall with a time "duration of 11 msec")
- Minimum velocity change = 4.23 meters/sec

6.6.4.2 Sinusoidal Shock Wave

- Approximate half-sine pulse shape.
- Maximum acceleration level and duration
 - 75 G, 11 msec (note 1)
 - 125 G, 2 msec (note 2)

Notes:

1. All shock input shall be applied in each direction of the drive's three mutually perpendicular axes.
2. Shock input shall be applied in the direction of file insertion.

The heads are not displaced from the landing zone as a result of this test.

6.7 Acoustics

6.7.1 Sound Power

6.7.1.1 Unit Sound Power Level Testing

Sound power emission levels are measured according to ISO 7779. The upper limit criteria of the octave sound power levels are given in Bels relative to 1 pico Watt and are shown in the following table.

Figure 38. Octave band sound power levels								
	Octave Band Center Frequency (Hz)							
Mode	125	250	500	1k	2k	4k	8k	LwAu
Idle	4.8	4.1	3.6	3.6	3.9	3.9	3.6	4.5
Operating	5.0	4.3	4.2	4.2	4.2	4.2	3.8	4.8

Mode definition

Idle mode Power on, disks spinning, track following, unit ready to receive and respond to interface command.

Operating mode

Continuous random cylinder selection and seek operation of the actuator with a dwell time at each cylinder. Seek rate for the drive can be calculated as shown below.

$$\text{Dwell time} = (0.5 + N) \times 60/\text{RPM}$$

$$\text{Seek rate} = 1 / (\text{Average seek time} + \text{Dwell time})$$

$$\text{where } N = \text{number of maximum data surfaces (} N=6 \text{ for DAQA-3xxxx)}$$

6.7.1.2 Sound Power Acceptance Criteria

Statistical upper limit $(L_{\text{Woct}})_{\text{stat}}$ is calculated with the following formula.

$$(L_{\text{Woct}})_{\text{stat}} = (L_{\text{Woct}})_m + k \times (s_t)_{\text{Woct}}$$

where:

$(L_{\text{Woct}})_m$ is the mean value of the sound power level for samples of N drives.

$(s_t)_{\text{Woct}}$ is the total standard deviation for sound power level at each octave band.

$$(s_t)_{\text{Woct}} = \text{SQRT}((s_R)_W^2 + (s_P)_{\text{Woct}}^2)$$

$(s_R)_W$ is the standard deviation of reproducibility for sound power level.

Assume $(s_R)_W = 0.075 \text{ B}$.

$(s_P)_{\text{Woct}}$ is the standard deviation of the samples for sound power level at each octave band.

k is a coefficient determined by number of samples (N) as shown below.

N	3	4	5	6	7	8	9	10	11	12	13	14	15
k	3.19	2.74	2.74	2.49	2.33	2.22	2.13	2.07	2.01	1.97	1.93	1.90	1.87

6.8 Identification

6.8.1 Labels

The following labels are affixed to every disk drive .

1. A label containing IBM logo, IBM part number and the statement 'Made by IBM' or equivalent.
2. A label containing drive model number, date code, formatted capacity, place of manufacture, and UL/CSA/TUV/CE mark logos.
3. A bar code label containing the drive serial number.

The labels may be integrated with other labels.

6.9 Electromagnetic Compatibility

The drive, when installed in a suitable enclosure and exercised with a random accessing routine at maximum data rate, shall meet the worldwide EMC requirements listed below.

IBM will provide technical support to assist users in complying with the EMC requirements.

- United States Federal Communications Commission (FCC) Rules and Regulations (Class B), Part 15.
- European Economic Community (EEC) directive number 76/889 related to the control of radio frequency interference and the Verband Deutscher Elektrotechniker (VDE) requirements of Germany (GOP).

6.9.1 CE Mark

The product is declared to be in conformity with the requirements of following EC directives under the sole responsibility of IBM United Kingdom Ltd.

Council Directive 89/336/EEC on the approximation of laws of the Member States relating to electromagnetic compatibility.

6.10 Safety

6.10.1 Underwriters Lab(UL) Approval

DAQA-32160/32700/33240 complies with UL 1950.

6.10.2 Canadian Standards Authority(CSA) Approval

DAQA-32160/32700/33240 complies with CSA C22.2, #950-M89.

6.10.3 IEC Compliance

DAQA-32160/32700/33240 complies with IEC 950.

6.10.4 German Safety Mark

DAQA-32160/32700/33240 are approved by TUV on Test Requirement:

EN 60 950:1988/A1:1990/A2:1991.

6.10.5 Flammability

Printed Circuit boards used in this product are made of material with a UL recognized flammability rating of V-1 or better. The flammability rating is marked or etched on the board. All other parts not considered electrical components are made of material with a UL recognized flammability rating of V-1 or better except minor mechanical parts.

6.10.6 Secondary Circuit Protection

Fuses are provided in 12V input of the hard disk drive for over current protection.

6.11 Packaging

Drives are shipped in ESD protective bags.

Part 2. ATA Interface Specification

7.0 Interface

This part describes the host interface of DAQA-3xxxx.

The interface conforms to the Working Document of Information technology - AT Attachment-3 Interface (ATA-3) Revision 6 dated on Oct. 26, 1995. with deviations described below.

7.1 Deviation from Standard

BBK(Bad Block)	Bit7 of Error Register is supported as BAD BLOCK bit. This bit will be set when BAD BLOCK is reported on Read commands.
Check Power Mode	CHECK POWER MODE command returns FFh to Sector Count Register when the device is in Idle mode. This command does not support 80h as the return value.
Sleep Mode	During Sleep mode the drive will be activated by any command, including, but not limited to, a soft reset.
Hard Reset	Hard reset response is not the same as that of power on reset. Refer to section 9.1, “Reset Response” on page 57 for detail.

8.0 Registers

Addresses					Functions	
CS0-	CS1-	DA2	DA1	DA0	READ(DIOR-)	WRITE(DIOW-)
N	N	x	x	x	Data bus high imped*1	Not used
					Control block registers	
N	A	0	x	x	Data bus high imped	Not used
N	A	1	0	x	Data bus high imped	Not used
N	A	1	1	0	Alternate Status	Device Control
N	A	1	1	1	Device Address	Not used
					Command block registers	
A	N	0	0	0	Data	Data
A	N	0	0	1	Error Register	Features
A	N	0	1	0	Sector Count	Sector Count
A	N	0	1	1	Sector Number	Sector Number
A	N	0	1	1	*2 LBA bits 0-7	*2 LBA bits 0-7
A	N	1	0	0	Cylinder Low	Cylinder Low
A	N	1	0	0	*2 LBA bits 8-15	*2 LBA bits 8-15
A	N	1	0	1	Cylinder High	Cylinder High
A	N	1	0	1	*2 LBA bits 16-23	*2 LBA bits 16-23
A	N	1	1	0	Device/Head	Device/Head
A	N	1	1	0	*2 LBA bits 24-27	*2 LBA bits 24-27
A	N	1	1	1	Status	Command
A	A	x	x	x	Invalid address	Invalid address

*1 "imped" stands for "impedance".
 *2 Mapping of registers in LBA mode

Logic conventions : A = signal asserted
 N = signal negated
 x = does not matter which it is

Figure 39. Register Set

Communication to or from the device is through an I/O Register that routes the input or output data to or from registers addressed by the signals from the host (CS0-, CS1-, DA2, DA1, DA0, DIOR- and DIOW-).

The Command Block Registers are used for sending commands to the device or posting status from the device.

The Control Block Registers are used for device control and to post alternate status.

8.1 Alternate Status Register

Alternate Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR

Figure 40. Alternate Status Register

This register contains the same information as the Status Register. The only difference is that reading this register does not imply interrupt acknowledge or clear a pending interrupt. See 8.13, “Status Register” on page 55 for the definition of the bits in this register.

8.2 Command Register

This register contains the command code being sent to the device. Command execution begins immediately after this register is written. The command set is shown in Figure 51 on page 73.

All other registers required for the command must be set up before writing the Command Register.

8.3 Cylinder High Register

This register contains the high order bits of the starting cylinder address for any disk access. At the end of the command, this register is updated to reflect the current cylinder number.

In LBA Mode this register contains Bits 16-23. At the end of the command, this register is updated to reflect the current LBA Bits 16-23.

The cylinder number may be from zero to the number of cylinders minus one.

8.4 Cylinder Low Register

This register contains the low order 8 bits of the starting cylinder address for any disk access. At the end of the command, this register is updated to reflect the current cylinder number.

In LBA Mode this register contains Bits 8-15. At the end of the command, this register is updated to reflect the current LBA Bits 8-15.

The cylinder number may be from zero to the number of cylinders minus one.

8.5 Data Register

This register is used to transfer data blocks between the device data buffer and the host. It is also the register through which sector information is transferred on a Format Track command, and configuration information is transferred on an Identify Device command.

All data transfers are 16 bits wide, except for ECC byte transfers, which are 8 bits wide. Data transfers are PIO only.

The register contains valid data only when DRQ=1 in the Status Register.

8.6 Device Control Register

Device Control Register							
7	6	5	4	3	2	1	0
—	—	—	—	1	SRST	—IEN	0

Figure 41. Device Control Register

Bit Definitions

SRST (RST) Software Reset. The device is held reset when RST=1. Setting RST=0 re-enables the device.

The host must set RST=1 and wait for at least 5 microseconds before setting RST=0, to ensure that the device recognizes the reset.

—IEN Interrupt Enable. When IEN=0, and the device is selected, device interrupts to the host will be enabled. When IEN=1, or the device is not selected, device interrupts to the host will be disabled.

8.7 Drive Address Register

Drive Address Register							
7	6	5	4	3	2	1	0
HIZ	—WTG	—H3	—H2	—H1	—H0	—DS1	—DS0

Figure 42. Drive Address Register

This register contains the inverted drive select and head select addresses of the currently selected drive.

Bit Definitions

HIZ High Impedance. This bit is not device and will always be in a high impedance state.

—WTG -Write Gate. This bit is 0 when writing to the disk device is in progress.

—H3,—H2,—H1,—H0 -Head Select. These four bits are the one's complement of the binary coded address of the currently selected head. —H0 is the least significant.

—DS1 -Drive Select 1. Drive select bit for device 1, active low. DS1=0 when device 1 (slave) is selected and active.

—DS0 -Drive Select 0. Drive select bit for device 0, active low. DS0=0 when device 0 (master) is selected and active.

8.8 Device/Head Register

Device/Head Register							
7	6	5	4	3	2	1	0
1	L	1	DRV	HS3	HS2	HS1	HS0

Figure 43. Device/Head Register

This register contains the device and head numbers.

Bit Definitions

- L** Binary encoded address mode select. When L=0, addressing is by CHS mode. When L=1, addressing is by LBA mode.
- DRV** Device. When DRV=0, device 0 (master) is selected. When DRV=1, device 1 (slave) is selected.
- HS3,HS2,HS1,HS0** Head Select. These four bits indicate binary encoded address of the head. HS0 is the least significant bit. At command completion, these bits are updated to reflect the currently selected head.
- The head number may be from zero to the number of heads minus one.
- In LBA mode, HS3 through HS0 contain bits 24-27 of the LBA. At command completion, these bits are updated to reflect the current LBA bits 24-27.

8.9 Error Register

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDNF	0	ABRT	TK0NF	AMNF

Figure 44. Error Register

This register contains status from the last command executed by the device, or a diagnostic code.

At the completion of any command except Execute Device Diagnostic, the contents of this register are valid always even if ERR=0 in the Status Register.

Following a power on, a reset, or completion of an Execute Device Diagnostic command, this register contains a diagnostic code. See Figure 48 on page 58 for the definition.

Bit Definitions

- BBK** Bad Block. BBK=1 indicates a bad block mark was detected in the requested sector's ID field.
- UNC** Uncorrectable Data Error. UNC=1 indicates an uncorrectable data error has been encountered.
- IDNF (IDN)** ID Not Found. IDN=1 indicates the requested sector's ID field could not be found.
- ABRT (ABT)** Aborted Command. ABT=1 indicates the requested command has been aborted due to a device status error or an invalid parameter in an output register.

TK0NF (T0N)	Track 0 Not Found. T0N=1 indicates track 0 was not found during a Recalibrate command.
AMNF (AMN)	Address Mark Not Found. AMN=1 indicates the data address mark has not been found after finding the correct ID field for the requested sector.

8.10 Features Register

This register is command specific. This is used with the Set Features command.

8.11 Sector Count Register

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the device. If the value in the register is set to 0, a count of 256 sectors is specified.

If the register is zero at command completion, the command was successful. If not successfully completed, the register contains the number of sectors which need to be transferred in order to complete the request.

The contents of the register are defined otherwise on some commands. These definitions are given in the command descriptions.

8.12 Sector Number Register

This register contains the starting sector number for any disk data access for the subsequent command. The sector number is from one to the maximum number of sectors per track.

In LBA mode, this register contains Bits 0-7. At the end of the command, this register is updated to reflect the current LBA Bits 0-7.

8.13 Status Register

Status Register							
7	6	5	4	3	2	1	0
BSY	DRDY	DF	DSC	DRQ	CORR	IDX	ERR

Figure 45. Status Register

This register contains the device status. The contents of this register are updated whenever an error occurs and at the completion of each command.

If the host reads this register when an interrupt is pending, it is considered to be the interrupt acknowledge. Any pending interrupt is cleared whenever this register is read.

If BSY=1, no other bits in the register are valid.

Bit Definitions

BSY	Busy. BSY=1 whenever the device is accessing the registers. The host should not read or write any registers when BSY=1. If the host reads any register when BSY=1, the contents of the Status Register will be returned.
DRDY (RDY)	Device Ready. RDY=1 indicates that the device is capable of responding to a command. RDY will be set to 0 during power on until the device is ready to accept a command. If the device detects an error while processing a command, RDY is set to 0 until the Status Register is read by the host, at which time RDY is set back to 1.
DF	Device Fault. DF=1 indicates that the device has detected a write fault condition. DF is set to 0 after the Status Register is read by the host.
DSC	Device Seek Complete. DSC=1 indicates that a seek has completed and the device head is settled over a track. DSC is set to 0 by the device just before a seek begins. When an error occurs, this bit is not changed until the Status Register is read by the host, at which time the bit again indicates the current seek complete status. When the device enters into or is in Standby mode or Sleep mode, this bit is set by device in spite of not spinning up.
DRQ	Data Request. DRQ=1 indicates that the device is ready to transfer a word or byte of data between the host and the device. The host should not write the Command register when DRQ=1.
CORR (COR)	Corrected Data. Always 0.
IDX	Index. IDX=1 once per revolution. Since IDX=1 only for a very short time during each revolution, the host may not see it set to 1 even if the host is reading the Status Register continuously. Therefore the host should not attempt to use IDX for timing purposes.
ERR	Error. ERR=1 indicates that an error occurred during execution of the previous command. The Error Register should be read to determine the error type. The device sets ERR=0 when the next command is received from the host.

9.0 General Operation Descriptions

9.1 Reset Response

There are three types of reset in ATA as follows:

Power On Reset (POR)

The device executes a series of electrical circuitry diagnostics, spins up the HDA, tests speed and other mechanical parameters, and sets default values.

Hard Reset (Hardware Reset)

RESET- signal is negated in ATA Bus.

The device resets the interface circuitry as well as Soft Reset.

Soft Reset (Software Reset)

SRST bit in the Device Control Register is set, then is reset.

The device resets the interface circuitry according to the Set Features requirement.

The actions of each reset is shown in Figure 46

	POR	hard reset	soft reset
Aborting Host interface	—	0	0
Aborting Device operation	—	(*1)	(*1)
Initialization of hardware	0	x	x
Internal diagnostic	0	x	x
Spinning spindle	0	x	x
Initialization of registers (*2)	0	0	0
DASP handshake	0	(*4)	x
PDIAG handshake	0	0	0
Reverting programmed parameters to default	0	(*3)	(*3)
— Number of CHS (set by Initialize Device Parameter)			
— Multiple mode			
— Write cache			
— Read look-ahead			
— ECC bytes			
Disable Standby timer	0	x	x
Power mode	Idle	x	x

0 — execute
x — not execute

Figure 46. Reset Response Table

Note.

- (*1) Execute after the data in write cache has been written.
- (*2) Default value on POR is shown in Figure 47 on page 58.
- (*3) The Set Features command with Feature register = CCh enables the device to revert these parameters to the power on defaults.

- (*4) In case of master drive setting, DASP is not checked and slave presence is assumed to be unchanged. In case of slave drive setting, this operation is the same as that of power on reset. In other case, the device does not change current mode.

9.1.1 Register Initialization

Register	Default Value
Error	Diagnostic Code
Sector Count	01h
Sector Number	01h
Cylinder Low	00h
Cylinder High	00h
Device/Head	A0h
Status	50h
Alternate Status	50h

Figure 47. Default Register Values

After power on, hard reset, or software reset, the register values are initialized as shown in Figure 47.

Code	Description
01h	No error detected
02h	Formatter device error
03h	Sector buffer error
04h	ECC circuitry error
05h	Controller microprocessor error
8xh	Device 1 failed

Figure 48. Diagnostic Codes

The meaning of the Error Register diagnostic codes resulting from power on, hard reset or the Execute Device Diagnostic command are shown in Figure 48.

9.2 Diagnostic and Reset considerations

For each Reset and Execute Device Diagnostic, the diagnostic is done as follows:

Power On Reset

DASP- is read by Device 0 to determine if Device 1 is present. If Device 1 is present Device 0 shall read PDIAG- to determine when it is valid to clear the BSY bit and whether Device 1 has powered on or reset without error, otherwise Device 0 clears the BSY bit whenever it is ready to accept commands. Device 0 may assert DASP- to indicate device activity.

Soft Reset, Hard Reset

If Device 1 is present Device 0 shall read PDIAG- to determine when it is valid to clear the BSY bit and whether Device 1 has reset without any errors, otherwise Device 0 shall simply reset and clear the BSY bit. DASP- is asserted by Device 0 (and Device 1 if it is present) in order to indicate device active.

Execute Device Diagnostic

If Device 1 is present, Device 0 shall read PDIAG- to determine when it is valid to clear the BSY bit and if Device 1 passed or failed the EXECUTE DEVICE DIAGNOSTIC command, otherwise Device 0 shall simply execute its diagnostics and then clear the BSY bit. DASP- is asserted by Device 0 (and Device 1 if it is present) in order to indicate the device is active.

In all the above cases: Power on, RESET-, Soft reset, and the EXECUTE DEVICE DIAGNOSTIC command the Device 0 Error register is shown in Figure 49.

Device 1 Present?	PDIAG- Asserted?	Device 0 Passed	Error Register
Yes	Yes	Yes	01h
Yes	Yes	No	0xh
Yes	No	Yes	81h
Yes	No	No	8xh
No	(not read)	Yes	01h
No	(not read)	No	0xh

Where x indicates the appropriate Diagnostic Code for the Power on, RESET-, Soft reset, or Device Diagnostic error.

Figure 49. Reset error register values

9.3 Sector Addressing Mode

All addressing of data sectors recorded on the device's media is by a logical sector address. The logical CHS address for DAQA-3xxxx is different from the actual physical CHS location of the data sector on the disk media.

DAQA-3xxxx support both Logical CHS Addressing Mode and LBA Addressing Mode as sector addressing mode.

The host system may select either the currently selected CHS translation addressing or LBA addressing on a command-by-command basis by using the L bit in the DEVICE/HEAD register. So a host system must set the L bit to 1 if the host uses LBA Addressing mode.

9.3.1 Logical CHS Addressing Mode

The logical CHS addressing is made up of three fields: the cylinder number, the head number and the sector number. Sectors are numbered from 1 to the maximum value allowed by the current CHS translation mode but can not exceed 255(0FFh). Heads are numbered from 0 to the maximum value allowed by the current CHS translation mode but can not exceed 15(0Fh). Cylinders are numbered from 0 to the maximum value allowed by the current CHS translation mode but cannot exceed 65535(0FFFFh).

When the host selects a CHS translation mode using the INITIALIZE DEVICE PARAMETERS command, the host requests the number of sectors per logical track and the number of heads per logical cylinder. The device then computes the number of logical cylinders available in requested mode.

The default CHS translation mode is described in the Identify Device Information. The current CHS translation mode also is described in the Identify Device Information.

9.3.2 LBA Addressing Mode

Logical sectors on the device shall be linearly mapped with the first LBA addressed sector (sector 0) being the same sector as the first logical CHS addressed sector (cylinder 0, head 0, sector 1). Irrespective of the logical CHS translation mode currently in effect, the LBA address of a given logical sector does not change. The following is always true:

$$\text{LBA} = ((\text{cylinder} * \text{heads_per_cylinder} + \text{heads}) * \text{sectors_per_track}) + \text{sector} - 1$$

where heads_per_cylinder and sectors_per_track are the current translation mode values.

On LBA addressing mode, the LBA value is set to the following register.

Device/Head	<---	LBA bits 27-24
Cylinder High	<---	LBA bits 23-16
Cylinder Low	<---	LBA bits 15- 8
Sector Number	<---	LBA bits 7- 0

9.4 Power Management Feature

The power management feature set permits a host to modify the behavior of a manner which reduces the power required to operate. The power management feature set provides a set of commands and a timer that enable a device to implement low power consumption modes.

DAQA-3xxxx implement the following set of functions.

1. A Standby timer
2. Idle command
3. Idle Immediate command
4. Sleep command
5. Standby command
6. Standby Immediate command

9.4.1 Power Mode

In Standby or Sleep Mode the device interface is capable of accepting commands, but as the media may not immediately accessible, there is a delay while waiting for the spindle to reach operating speed.

In Idle Mode the device is capable of responding immediately to media access requests.

In Active Mode the device is under executing a command or accessing the disk media with read look-ahead function or write cache function.

9.4.2 Power Management Commands

The Check Power Mode command allows a host to determine if a device is currently in, going to or leaving standby mode.

The Idle and Idle Immediate commands move a device to idle mode immediately from the active or standby modes. The idle command also sets the standby timer count and starts the standby timer.

The Standby and Standby Immediate commands move a device to standby mode immediately from the active or idle modes. The standby command also sets the standby timer count.

The sleep command moves a device to sleep mode, which is identical with standby mode.

9.4.3 Standby timer

The standby timer provides a method for the device to automatically enter standby mode from either active or idle mode following a host programmed period of inactivity. If the device is in the active or idle mode, the device waits for the specified time period and if no command is received, the device automatically enters the standby mode.

If the value of SECTOR COUNT register on Idle command or Standby command is set to 00h, the standby timer is disabled.

9.4.4 Interface Capability for Power Modes

The each power mode affects the physical interface as defined in the following table:

Mode	BSY	RDY	Interface active	Media
Active	x	x	Yes	Active
Idle	0	1	Yes	Active
Standby	0	1	Yes	Inactive
Sleep	0	1	Yes	Inactive

Figure 50. Power conditions

Ready(RDY) is not a power condition. A device may post ready at the interface even though the media may not be accessible.

9.5 S.M.A.R.T. Function

The intent of Self-monitoring, analysis and reporting technology (S.M.A.R.T) is to protect user data and prevent unscheduled system downtime that may be caused by predictable degradation and/or fault of the device. By monitoring and storing critical performance and calibration parameters, S.M.A.R.T devices employ sophisticated data analysis algorithms to predict the likelihood of near-term degradation or fault condition. By alerting the host system of a negative reliability status condition, the host system can warn the user of the impending risk of a data loss and advise the user of appropriate action.

9.5.1 Attributes

Attributes are the specific performance or calibration parameters that are used in analyzing the status of the device. Attributes are selected by the device manufacturer based on that attribute's ability to contribute to the prediction of degrading or faulty conditions for that particular device. The specific set of attributes being used and the identity of these attributes is vendor specific and proprietary.

9.5.2 Attribute values

Attribute values are used to represent the relative reliability of individual performance or calibration attributes. The valid range of attribute values is from 1 to 253 decimal. Higher attribute values indicate that the analysis algorithms being used by the device are predicting a lower probability of a degrading or faulty condition existing. Accordingly, lower attribute values indicate that the analysis algorithms being used by the device are predicting a higher probability of a degrading or faulty condition existing.

9.5.3 Attribute thresholds

Each attribute value has a corresponding attribute threshold limit which is used for direct comparison to the attribute value to indicate the existence of a degrading or faulty condition. The numerical value of the attribute thresholds are determined by the device manufacturer through design and reliability testing and analysis. Each attribute threshold represents the lowest limit to which its corresponding attribute value can be equal while still retaining a positive reliability status. Attribute thresholds are set at the device manufacturer's factory and cannot be changed in the field. The valid range for attribute thresholds is from 1 through 253 decimal.

9.5.4 Threshold exceeded condition

If one or more attribute values are less than or equal to their corresponding attribute thresholds, then the device reliability status is negative, indicating an impending degrading or faulty condition.

9.5.5 S.M.A.R.T. commands

The S.M.A.R.T. commands provide access to attribute values, attribute thresholds and other logging and reporting information.

9.6 Reassign Function

Reassign Function is used with `FORMAT TRACK` command, read with retry commands and write commands. The sectors of data for reassignment are prepared as the spare data sector. The assured number of the spare sectors is minimum 100 sectors.

This reassignment information is registered internally, and the information is available right after completing the reassign function. Also the information is used on next power on reset or hard reset.

If the number of the spare sector reaches 0 sector, the reassign function will be disabled automatically.

The spare sectors for reassignment are located at the end of device. As a result of reassignment, the physical location of logically sequenced sectors will be dispersed.

9.6.1 Auto Reassign Function

The sectors those show some errors may be reallocated automatically when specific conditions are met. The spare sectors for reallocation are located at the end of drive. The conditions for auto-reallocation are described below.

When a device shipped from IBM, minimum 100 of usable spare sectors are available.

Non recovered write errors

When a write operation can not be completed after the Error Recovery Procedure(ERP) is fully carried out, the sector(s) are reallocated to the spare location. An error is reported to the host system only when the write cache is disabled and the auto reallocation is failed.

If the write cache function is `DISABLED`, and when the number of available spare sectors reaches 16 sectors, the auto reassign function will be disabled automatically.

If the write cache function is `ENABLED`, and when the number of available spare sectors reaches 0 sector, both auto reassign function and write cache function are disabled automatically.

If the command is without retry and the write cache function is disabled, the auto reassign function is not invoked.

Non recovered read errors

When a read operation is failed after defined ERP is fully carried out, a hard error is reported to the host system. This location is registered internally as a candidate for the reallocation. When a registered location is specified as a target of a write operation, a sequence of media verification is performed automatically. When the result of this verification meets the criteria, this sector is reallocated.

Recovered read errors

When a read operation for a sector failed once then recovered at the specific ERP step, this sector of data is reallocated automatically. A media verification sequence may be run prior to the relocation according to the pre-defined conditions.

If the number of available spare sectors reaches 16 sectors, the auto reassign function is disabled automatically.

9.7 Write Cache Function

Write cache is a performance enhancement whereby the device reports as completing the write command (Write Sectors, Write Multiple and Write DMA) to the host as soon as the device has received all of the data into its buffer. And the device assumes responsibility to write the data subsequently onto the disk.

- While writing data after completed acknowledgment of a write command, soft reset or hard reset does not affect its operation. But power off terminates writing operation immediately and unwritten data are to be lost.
- Soft reset and Check Power Mode command during writing the cached data are executed after the completion of writing to media. So the host system can confirm the completion of write cache operation by issuing Soft reset or Check Power Mode command and then confirming its completion. We developer of the device recommend that a host system checks the completion of write cache operation by issuing Soft reset or Check Power Mode command to the device before power off.
- The retry bit of Write Sectors is ignored when write cache is enabled.

9.8 Write Cache Jumper

Write Cache feature can be disabled by installing the jumper. The device firmware checks the state of the jumper during Power On initialization.

The Set Features command to enable Write Cache is terminated with Aborted Command error if the jumper is installed.

10.0 Command Protocol

The commands are grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined below.

For all commands, the host must first check if BSY=1, and should proceed no further unless and until BSY=0. For all commands, the host must also wait for RDY=1 before proceeding.

A device must maintain either BSY=1 or DRQ=1 at all times until the command is completed. The INTRQ signal is used by the device to signal most, but not all, times when the BSY bit is changed from 1 to 0 during command execution.

A command shall only be interrupted with a hardware or software reset. The result of writing to the Command register while BSY=1 or DRQ=1 is unpredictable and may result in data corruption. A command should only be interrupted by a reset at times when the host thinks there may be a problem, such as a device that is no longer responding.

Interrupts are cleared when the host reads the Status Register, issues a reset, or writes to the Command Register.

Figure 91 on page 129 shows the device timeout values.

10.1 Data In Commands

These commands are:

- Identify Device
- Read Buffer
- Read Long
- Read Multiple
- Read Sectors
- SMART Read Attribute Values
- SMART Read Attribute Thresholds

Execution includes the transfer of one or more 512 byte (>512 bytes on Read Long) sectors of data from the device to the host.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head Registers.
2. The host writes the command code to the Command Register.
3. For each sector (or block) of data to be transferred:
 - a. The device sets BSY=1 and prepares for data transfer.
 - b. When a sector (or block) of data is available for transfer to the host, the device sets BSY=0, sets DRQ=1, and interrupts the host.
 - c. In response to the interrupt, the host reads the Status Register.
 - d. The device clears the interrupt in response to the Status Register being read.
 - e. The host reads one sector (or block) of data via the Data Register.

- f. The device sets DRQ=0 after the sector (or block) has been transferred to the host.
4. For the Read Long command:
 - a. The device sets BSY=1 and prepares for data transfer.
 - b. When the sector of data is available for transfer to the host, the device sets BSY=0, sets DRQ=1, and interrupts the host.
 - c. In response to the interrupt, the host reads the Status Register.
 - d. The device clears the interrupt in response to the Status Register being read.
 - e. The host reads the sector of data including ECC bytes via the Data Register.
 - f. The device sets DRQ=0 after the sector has been transferred to the host.

The Read Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.

Note that the status data for a sector of data is available in the Status Register **before** the sector is transferred to the host.

If the device detects an invalid parameter, then it will abort the command by setting BSY=0, ERR=1, ABT=1, and interrupting the host.

If an error occurs, the device will set BSY=0, ERR=1, and DRQ=1. The device will then store the error status in the Error Register, and interrupt the host. The registers will contain the location of the sector in error. The errored location will be reported with CHS mode or LBA mode, the mode is decided by mode select bit (bit 6) of Device/Head register on issuing the command.

If an Uncorrectable Data Error (UNC=1) occurs, the defective data will be transferred from the media to the sector buffer, and will be available to be transferred to the host, at the host's option. In case of Read Multiple command, the host should complete transfer the block which includes error from the sector buffer and terminate whatever kind of type of error occurred.

If an error occurs that is correctable by retries, the data will be corrected and the transfer will continue normally. There will be no indication to the host that any retry occurred.

All data transfers to the host through the Data Register are 16 bits, except for the ECC bytes, which are 8 bits.

10.2 Data Out Commands

These commands are:

- Format Track
- Write Buffer
- Write Long
- Write Multiple
- Write Sectors

Execution includes the transfer of one or more 512 byte (>512 bytes on Write Long) sectors of data from the host to the device.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head Registers.
2. The host writes the command code to the Command Register.
3. The device sets BSY=1.
4. For each sector (or block) of data to be transferred:
 - a. The device sets BSY=0 and DRQ=1 when it is ready to receive a sector (or block).
 - b. The host writes one sector (or block) of data via the Data Register.
 - c. The device sets BSY=1 after it has received the sector (or block).
 - d. When the device has finished processing the sector (or block), it sets BSY=0, and interrupts the host.
 - e. In response to the interrupt, the host reads the Status Register.
 - f. The device clears the interrupt in response to the Status Register being read.
5. For the Write Long command:
 - a. The device sets BSY=0 and DRQ=1 when it is ready to receive a sector.
 - b. The host writes one sector of data including ECC bytes via the Data Register.
 - c. The device sets BSY=1 after it has received the sector.
 - d. After processing the sector of data the device sets BSY=0 and interrupts the host.
 - e. In response to the interrupt, the host reads the Status Register.
 - f. The device clears the interrupt in response to the Status Register being read.

The Write Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.

If the device detects an invalid parameter, then it will abort the command by setting BSY=0, ERR=1, ABT=1, and interrupting the host.

If an uncorrectable error occurs, the device will set BSY=0 and ERR=1, store the error status in the Error Register, and interrupt the host. The registers will contain the location of the sector in error. The errored location will be reported with CHS mode or LBA mode, the mode is decided by mode select bit (bit 6) of Device/Head register on issuing the command.

All data transfers to the device through the Data Register are 16 bits, except for the ECC bytes, which are 8 bits.

10.3 Non-Data Commands

These commands are:

- Check Power Mode
- Execute Device Diagnostic
- Idle
- Idle Immediate
- Initialize Device Parameters
- Read Verify Sectors
- Recalibrate
- Seek
- Set Features
- Set Multiple Mode
- Sleep
- SMART Disable Operations
- SMART Enable/Disable Attribute Autosave
- SMART Enable Operations
- SMART Execute Off-line Data Collection
- SMART Return Status
- SMART Save Attribute Values
- Standby
- Standby Immediate

Execution of these commands involves no data transfer.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head Registers.
2. The host writes the command code to the Command Register.
3. The device sets BSY=1.
4. When the device has finished processing the command, it sets BSY=0, and interrupts the host.
5. In response to the interrupt, the host reads the Status Register.
6. The device clears the interrupt in response to the Status Register being read.

10.4 DMA Data Transfer Commands

These commands are:

- Identify Device DMA
- Read DMA
- Write DMA

Data transfer using DMA commands differ in two ways from PIO transfers:

- data transfers are performed using the slave-DMA channel
- no intermediate sector interrupts are issued on multi-sector commands

Initiation of the DMA transfer commands is identical to the Read Sector or Write Sector commands except that the host initializes the slave-DMA channel prior to issuing the command.

The interrupt handler for DMA transfers is different in that:

- no intermediate sector interrupts are issued on multi-sector commands
- the host resets the DMA channel prior to reading status from the device.

The DMA protocol allows high performance multi-tasking operating systems to eliminate processor overhead associated with PIO transfers.

1. Host initializes the slave-DMA channel
2. Host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder and Device/Head registers.
3. Host writes command code to the Command Register
4. The device sets DMARQ when it is ready to transfer any part of the data.
5. Host transfers the data using the DMA transfer protocol currently in effect.
6. When all of the data has been transferred, the device generates an interrupt to the host.
7. Host resets the slave-DMA channel
8. Host reads the Status Register and, optionally, the Error Register

11.0 Command Descriptions

Proto col	Command	Code (Hex)	Binary Code Bit							
			7	6	5	4	3	2	1	0
3	Check Power Mode	E5	1	1	1	0	0	1	0	1
3	Check Power Mode*	98	1	0	0	1	1	0	0	0
3	Execute Device Diagnostic	90	1	0	0	1	0	0	0	0
2	Format Track	50	0	1	0	1	0	0	0	0
1	Identify Device	EC	1	1	1	0	1	1	0	0
4	Identify Device DMA	EE	1	1	1	0	1	1	1	0
3	Idle	E3	1	1	1	0	0	0	1	1
3	Idle*	97	1	0	0	1	0	1	1	1
3	Idle Immediate	E1	1	1	1	0	0	0	0	1
3	Idle Immediate*	95	1	0	0	1	0	1	0	1
3	Initialize Device Parameters	91	1	0	0	1	0	0	0	1
1	Read Buffer	E4	1	1	1	0	0	1	0	0
4	Read DMA (retry)	C8	1	1	0	0	1	0	0	0
4	Read DMA (no retry)	C9	1	1	0	0	1	0	0	1
1	Read Long (retry)	22	0	0	1	0	0	0	1	0
1	Read Long (no retry)	23	0	0	1	0	0	0	1	1
1	Read Multiple	C4	1	1	0	0	0	1	0	0
1	Read Sectors (retry)	20	0	0	1	0	0	0	0	0
1	Read Sectors (no retry)	21	0	0	1	0	0	0	0	1
3	Read Verify Sectors (retry)	40	0	1	0	0	0	0	0	0
3	Read Verify Sectors (no retry)	41	0	1	0	0	0	0	0	1
3	Recalibrate	1x	0	0	0	1	—	—	—	—
3	Seek	7x	0	1	1	1	—	—	—	—
3	Set Features	EF	1	1	1	0	1	1	1	1
3	Set Multiple Mode	C6	1	1	0	0	0	1	1	0

Figure 51. Command Set

Protocol	Command	Code (Hex)	Binary Code							
			7	6	5	4	3	2	1	0
3	Sleep	E6	1	1	1	0	0	1	1	0
3	Sleep*	99	1	0	0	1	1	0	0	1
3	SMART Disable Operations	B0	1	0	1	1	0	0	0	0
3	SMART Enable/Disable Attribute Autosave	B0	1	0	1	1	0	0	0	0
3	SMART Enable Operations	B0	1	0	1	1	0	0	0	0
3	SMART Execute Off-line Data Collection	B0	1	0	1	1	0	0	0	0
1	SMART Read Attribute Values	B0	1	0	1	1	0	0	0	0
1	SMART Read Attribute Thresholds	B0	1	0	1	1	0	0	0	0
3	SMART Return Status	B0	1	0	1	1	0	0	0	0
3	SMART Save Attribute Values	B0	1	0	1	1	0	0	0	0
3	Standby	E2	1	1	1	0	0	0	1	0
3	Standby*	96	1	0	0	1	0	1	1	0
3	Standby Immediate	E0	1	1	1	0	0	0	0	0
3	Standby Immediate*	94	1	0	0	1	0	1	0	0
2	Write Buffer	E8	1	1	1	0	1	0	0	0
4	Write DMA (retry)	CA	1	1	0	0	1	0	1	0
4	Write DMA (no retry)	CB	1	1	0	0	1	0	1	1
2	Write Long (retry)	32	0	0	1	1	0	0	1	0
2	Write Long (no retry)	33	0	0	1	1	0	0	1	1
2	Write Multiple	C5	1	1	0	0	0	1	0	1
2	Write Sectors (retry)	30	0	0	1	1	0	0	0	0
2	Write Sectors (no retry)	31	0	0	1	1	0	0	0	1

Protocol : 1 : PIO data IN command
2 : PIO data OUT command
3 : Non data command
4 : DMA command

Figure 52. Command Set - continued

Commands marked * are alternate command codes for previous defined commands.

Command (Subcommand)	Command Code (Hex)	Feature Register (Hex)
(S.M.A.R.T function)		
SMART Read Attribute Values	B0	D0
SMART Read Attribute Thresholds	B0	D1
SMART Enable/Disable Attribute Autosave	B0	D2
SMART Save Attribute Values	B0	D3
SMART Execute Off-line Data Collection	B0	D4
SMART Enable Operations	B0	D8
SMART Disable Operations	B0	D9
SMART Return Status	B0	DA
(Set Features)		
Enable Write Cache	EF	02
Set Transfer Mode	EF	03
22 bytes of ECC apply on Read/Write Long	EF	44
Disable read look-ahead feature	EF	55
Disable reverting to power on defaults	EF	66
Disable write cache	EF	82
Enable read look-ahead feature	EF	AA
4 bytes of ECC apply on Read/Wrtie Long	EF	BB
Enable reverting to power on defaults	EF	CC

Figure 53. Command Set (Subcommand)

Figure 51 on page 73 and Figure 52 on page 74 shows the commands that are supported by the device. Figure 53 shows the sub-commands that are supported by each command or feature.

The following symbols are used in the command descriptions:

Output Registers

- 0** Indicates that the bit must be set to 0.
- 1** Indicates that the bit must be set to 1.
- D** The device number bit. Indicates that the device number bit of the Device/Head Register should be specified. Zero selects the master device and one selects the slave device.
- H** Head number. Indicates that the head number part of the Device/Head Register is an output parameter and should be specified.
- L** LBA mode. Indicates the addressing mode. Zero specifies CHS mode and one does LBA addressing mode.
- R** Retry. Indicates that the Retry bit of the Command Register should be specified.
- V** Valid. Indicates that the bit is part of an output parameter and should be specified.
- x** Indicates that the hex character is not used.
- Indicates that the bit is not used.

Input Registers

- 0** Indicates that the bit is always set to 0.
- 1** Indicates that the bit is always set to 1.
- H** Head number. Indicates that the head number part of the Device/Head Register is an input parameter and will be set by the device.
- V** Valid. Indicates that the bit is part of an input parameter and will be set to 0 or 1 by the device.
- Indicates that the bit is not part of an input parameter.

The command descriptions show the contents of the Status and Error Registers after the device has completed processing the command and has interrupted the host.

11.1 Check Power Mode (E5h/98h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	1	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	-	-	0	-	V

Figure 54. Check Power Mode Command (E5h/98h)

The Check Power Mode command will report whether the device is spun up and the media is available for immediate access.

Input Parameters From The Device

Sector Count The power mode code. The command returns FFh in the Sector Count Register if the spindle motor is at speed and the drive is not in Standby or Sleep mode. Otherwise, the Sector Count Register will be set to 0.

11.2 Execute Device Diagnostic (90h)

Command Block Output Registers							
Register	7	6	5	4	3	2	1 0
Data	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-
Device/Head	1	-	1	-	-	-	-
Command	1	0	0	1	0	0	0 0

Command Block Input Registers							
Register	7	6	5	4	3	2	1 0
Data	-	-	-	-	-	-	-
Error	...See Below...						
Sector Count	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-
Status	...See Below...						

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
V	V	V	V	V	V	V	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	-	-	0	-	0

Figure 55. Execute Device Diagnostic Command (90h)

The Execute Device Diagnostic command performs the internal diagnostic tests implemented by the device. The results of the test are stored in the Error Register.

The normal Error Register bit definitions do not apply to this command. Instead, the register contains a diagnostic code. See Figure 48 on page 58 for the definition.

11.3 Format Track (50h: Vendor Specific)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	1	0	1	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 56. Format Track Command (50h)

The Format Track command formats a single logical track on the device. Each good sector of data on the track will be initialized to zero with write operation. At this time, the sector of data is not verified with read operation whether the sector of data is initialized correctly. Any data previously stored on the track will be lost.

The host transfers a sector of data containing a format table to the device. The format table should contain two bytes for each sector on the track to be formatted. The structure of format table is shown in Figure 57 on page 81. The first byte should contain a descriptor value and the second byte should contain the sector number. The descriptor value should be 0 for a good sector, 20h for an unassign sector, 40h for an assign sector, 80h for a bad sector, and any other descriptor value will cause an aborted error. The remaining bytes of the sector following the format table are ignored.

Since device performance is optimal at 1:1 interleave, and the device uses relative block addressing internally, the device will always format a track in the same way no matter what sector numbering is specified in the format table.

Output Parameters To The Device

Sector Number In LBA mode, this register specifies LBA address bits 0 - 7 to be formatted. (L=1)

Cylinder High/Low The cylinder number of the track to be formatted. (L=0)

In LBA mode, this register specifies LBA address bits 8 - 15 (Low), 16 - 23 (High) to be formatted. (L=1)

H The head number of the track to be formatted. (L=0)
In LBA mode, this register specifies LBA address bits 24 - 27 to be formatted. (L=1)

Input Parameters From The Device

Sector Number In LBA mode, this register specifies current LBA address bits 0-7. (L=1)

Cylinder High/Low In LBA mode, this register specifies current LBA address bits 8 - 15 (Low), 16 - 23 (High)

H In LBA mode, this register specifies current LBA address bits 24 - 27. (L=1)

Error The Error Register. An Abort error (ABT=1) will be returned under the following conditions:

- The descriptor value does not match the certain value. (except 00h, 20h, 40h and 80h)
- The number of assign(40h) exceeds the maximum number of reassign table entry.
- No spare data sector to be assigned.

In LBA mode, this command formats a single logical track including the specified LBA.

Explanation for descriptor

Descriptor : 00h The sector of data will be initialized to 00h.

Descriptor : 20h The sector will be unassigned to the original location from the reassigned location.

Descriptor : 40h The sector will be assigned to a spare data sector. When being accessed by next command, the spare sector of data will be used automatically. The assigned sector can be unassigned with a descriptor 20h.

Descriptor : 80h The sector will be registered as a bad sector. Thereafter, the sector reports BAD BLOCK to ERROR Register on Read commands. But the sector will not report BAD BLOCK if the sector is written by Write commands.

Byte	Data	Description
0 1	xxh 00h	descriptor value for sector number 00h sector number
2 3	xxh 01h	descriptor value for sector number 01h sector number
4 5	xxh 02h	descriptor value for sector number 02h sector number
:	:	
:	:	
N*2 N*2+1	xxh N	descriptor value for sector number N sector number (last sector for the track)
N*2+2 N*2+3 : : 510 511	00h 00h : : 00h 00h	remainder of buffer filled with 00h

Descriptor : 00h – Format sector as good sector
20h – Unassign the alternate location for this sector
40h – Assign this sector to an alternate location
80h – Format sector as bad sector

Figure 57. Format track data field format

11.4 Identify Device (ECh)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 58. Identify Device Command (ECh)

The Identify Device command requests the device to transfer configuration information to the host. The device will transfer a sector to the host containing the information in Figure 59 on page 83.

Word	Content	Description
00	045AH	Drive classification, bit assignments: 15(=0): 1=ATAPI device, 0=ATA device * 14(=0): 1=format speed tolerance gap required * 13(=0): 1=track offset option available * 12(=0): 1=data strobe offset option available * 11(=0): 1=rotational speed tolerance > 0.5% * 10(=1): 1=disk transfer rate > 10 Mbps * 9(=0): 1=disk transfer rate > 5 Mbps but <= 10 Mbps * 8(=0): 1=disk transfer rate <= 5 Mbps 7(=0): 1=removable cartridge drive 6(=1): 1=fixed drive * 5(=0): 1=spindle motor control option implemented * 4(=1): 1=head switch time > 15 us * 3(=1): 1=not MFM encoded * 2(=0): 1=soft sectoring * 1(=1): 1=hard sectoring 0(=0): Reserved
01	Note 1	Number of cylinders in default translate mode
02	0	* Number of removable cylinders
03	0010H	Number of heads in default translate mode
04	0	* Reserved
05	0	* Reserved
06	003FH	Number of sectors per track in default translate mode
07	0000H	* Number of bytes of sector gap
08	0000H	* Number of bytes in sync field
09	0000H	* Reserved
10-19	XXXX	Serial number in ASCII (0 = not specified)
20	0003H	* Controller type: 0003: dual ported, multiple sector buffer with look-ahead read
21	00C0H	* Buffer size in 512-byte increments (=96KB)
22	0016H	Number of ECC bytes (Vendor unique length selected via set feature cmd)
23-26	XXXX	Microcode version in ASCII
27-46	Note 1	Model number in ASCII
47	0010H	Maximum number of sectors that can be transferred per interrupt on Read and Write Multiple commands
48	0000H	Capable of double word I/O, '0000'= cannot perform
49	0F00H	Capabilities, bit assignments: 15-14(=0) Reserved 13(=0) Standby timer value are vendor specific 12(=0) Reserved 11(=1) IORDY Supported 10(=1) IORDY can be disabled 9(=1) 1=LBA Supported 8(=1) 1=DMA Supported * 7- 0(=0) Reserved
50	0000H	Reserved

Figure 59. Identify device information

Word	Content	Description
51	0200H	PIO data transfer cycle timing mode
52	0200H	DMA data transfer cycle timing mode Refer Word 62 and 63
53	0003H	Validity flag of the word 15- 2(=0) Reserved 1(=1) 1=Word 64-70 are Valid 0(=1) 1=Word 54-58 are Valid
54	XXXXH	Number of current cylinders
55	XXXXH	Number of current heads
56	XXXXH	Number of current sectors per track
57-58	XXXXH	Current capacity in sectors Word 57 specifies the low word of the capacity
59	0XXXH	Current Multiple setting. bit assignments 15- 9(=0) Reserved 8 1= Multiple Sector Setting is Valid 7- 0 xxh = Current setting for number of sectors
60-61	Note 1	Total Number of User Addressable Sectors Word 60 specifies the low word of the number
62	xx07H	Single Word DMA Transfer Capability 15- 8 Single word DMA transfer mode active 7- 0(=7) Single word DMA transfer modes supported (support mode 0,1 and 2)
63	Note 2	Multiword DMA Transfer Capability 15- 8 Multiword DMA transfer mode active 7- 0(=3) Multiword DMA Mode 0 and 1 supported 7- 0(=7) Multiword DMA Mode 0, 1 and 2 supported
64	0003H	Flow Control PIO Transfer Modes Supported 15- 8(=0) Reserved 7- 0(=3) Advanced PIO Transfer Modes Supported '11' = PIO Mode 3 and 4 Supported
65	Note 3	Minimum Multiword DMA Transfer Cycle Time
66	Note 3	Manufacturer's Recommended Multiword DMA Transfer Cycle Time
67	00F0H	Minimum PIO Transfer Cycle Time Without Flow Control 15- 0(=F0) Cycle time in nanoseconds (240ns, 8.3MB/s)
68	0078H	Minimum PIO Transfer Cycle Time With IORDY Flow Control 15- 0(=78) Cycle time in nanoseconds (120ns, 16.6MB/s)
69-79	0000H	Reserved
80	000EH	Major version number 15- 0(=0E) ATA-1, ATA-2 and ATA-3
81	0006H	Minor version number 15- 0(=06) ATA-3 X3T10 2008D revision 1

Figure 60. Identify device information --- Continued ---

Word	Content	Description
82	0009H	Command set supported 15- 4(=0) Reserved 3(=1) Power management feature set 2(=0) Removable feature set 1(=0) Security feature set 0(=1) SMART feature set
83	4000H	Command set supported
84-127	0000H	Reserved
128	0000H *	Device Lock Function. Bit assignments 0 Capability 1= Support 1 Enable/Disable 1= Enable 2 Lock 1= Locked 3 Freeze 1= Frozen 4 Expire 1= Expired 8 Security Level 1= Maximum, 0= High 9-15 Reserved
129	XXXXH *	Current Set Feature Option. Bit assignments 0 Write Cache 1= Enable 1 Read Look-ahead 1= Enable 2 Reverting 1= Enable 3 Auto reassign 1= Enable 4-15 Reserved
130	XXXXH *	Reserved
131-255	0000H	Reserved

Figure 61. Identify device information --- Continued ---

Note. The '*' mark in 'Content' field indicates the use of the parameter is vendor specific.

Note 1. The number of cylinders, total number of user addressable sectors and the model number in ASCII are as follows.

Model	Cylinders	Total LBAs	Model Number in ASCII
DAQA-32160	1068H	409980H	'IBM-DAQA-32160'
DAQA-32700	1480H	50B800H	'IBM-DAQA-32700'
DAQA-33240	1898H	60D680H	'IBM-DAQA-33240'

Note 2. Earlier versions of the drive only provided support for Mode-1 rather than Mode-2 transfers when operated in DMA Multiword mode.

This information is specified in the Identify Device data, word 63.

If the drive reports this word as xx03H, it returns then only DMA Multiword mode 0 and 1 are supported.

If the drive reports this word as xx07H, it returns then DMA Multiword mode 0, 1 and 2 are supported.

Note 3. DAQA-3xxxx has two versions on Multiword DMA as described in Note 2. The word 65 and 66 are as follows.

- Word 65 = Word 66 = 0078H (120ns) : Multiword DMA Mode 2 support version.
- Word 65 = Word 66 = 00F0H (240ns) : Multiword DMA Mode 1 support version.

11.5 Identify Device DMA (EEh)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	1	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 62. Identify Device Command DMA (EEh)

The Identify Device DMA command requests the device to transfer configuration information to the host. The device will transfer the same 256 words of device identification data by the Identify Device command(ECh) via DMA channel.

11.6 Idle (E3h/97h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	0	1	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 63. Idle Command (E3h/97h)

The Idle command causes the device to enter Idle mode immediately, and set auto power down timeout parameter(standby timer). And then the timer starts counting down.

When the Idle mode is entered, the device is spun up to operating speed. If the device is already spinning, the spin up sequence is not executed.

During Idle mode the device is spinning and ready to respond to host commands immediately.

Output Parameters To The Device

Sector Count Timeout Parameter. If zero, the timeout interval(Standby Timer) is disabled, If other than zero, the timeout interval is set for (Timeout Parameter × 5) seconds.

The device will enter Standby mode automatically if the timeout interval expires with no device access from the host. The timeout interval will be reinitialized if there is a device access before the timeout interval expires.

11.7 Idle Immediate (E1h/95h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 64. Idle Immediate Command (E1h/95h)

The Idle Immediate command causes the device to enter Idle mode.

The device is spun up to operating speed. If the device is already spinning, the spin up sequence is not executed.

During Idle mode the device is spinning and ready to respond to host commands immediately.

The Idle Immediate command will not affect to auto power down timeout parameter.

11.8 Initialize Device Parameters (91h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	H	H	H	H
Command	1	0	0	1	0	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	-	-	0	-	V

Figure 65. Initialize Device Parameters Command (91h)

Initialize Device Parameters command enables the host to set the number of sectors per track and the number of heads minus 1, per cylinder. Words 54-58 in Identify Device information reflects these parameters.

The parameters remain in effect until following events:

- Another Initialize Device Parameters command is received.
- The device is powered off.
- Hard reset is occurred.
- Soft reset is occurred and the Set Feature option of CCh is set instead of 66h.

Output Parameters To The Device

Sector Count Number of sectors per track. 0 does not mean there are 256 sectors per track, but there is no sector per track.

H Number of heads minus 1 per cylinder. The minimum is 0 and the maximum is 15.

Note: The following condition needs to be satisfied to avoid invalid number of cylinder beyond FFFFh, which will cause performance degradation of the drive.

$$(\text{Total customer usable data sectors}) / ((\text{Sector Count}) * (\text{H} + 1)) < \text{FFFFh}$$

The total customer usable data sectors are indicated at 3.1, “Logical Drive Format” on page 7, and related description is at 9.3.1, “Logical CHS Addressing Mode” on page 60.

11.9 Read Buffer (E4h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 66. Read Buffer Command (E4h)

The Read Buffer command transfers a sector of data from the sector buffer of device to the host.

The sector is transferred through the Data Register 16 bits at a time.

The sector transferred will be from the same part of the buffer written to by the last Write Buffer command. The contents of the sector may be different if any reads or writes have occurred since the Write Buffer command was issued.

11.10 Read DMA (C8h/C9h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	1	0	0	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
V	0	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 67. Read DMA Command (C8h/C9h)

The Read DMA command reads one or more sectors of data from disk media, then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. The data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Output Parameters To The Device

- Sector Count** The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
- Sector Number** The sector number of the first sector to be transferred. (L=0)
 In LBA mode, this register specifies LBA address bits 0 - 7 to be transferred. (L=1)
- Cylinder High/Low** The cylinder number of the first sector to be transferred. (L=0)
 In LBA mode, this register specifies LBA address bits 8 - 15 (Low) 16 - 23 (High) to be transferred. (L=1)

- H** The head number of the first sector to be transferred. (L=0)
In LBA mode, this register specifies LBA bits 24-27 to be transferred. (L=1)
- R** The retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

- Sector Count** The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
- Sector Number** The sector number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
- Cylinder High/Low** The cylinder number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
- H** The head number of the sector to be transferred. (L=0)
In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

11.11 Read Long (22h/23h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	0	0	0	0	0	0	0	1
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	0	1	0	0	0	1	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 68. Read Long Command (22h/23h)

The Read Long command read the designated one sector of data and the ECC bytes from disk media, then transfers the data and ECC bytes from the device to the host.

After 512 bytes of data have been transferred, the device will keep setting DRQ=1 to indicate that the device is ready to transfer the ECC bytes to the host. The data is transferred 16 bits at a time, and the ECC bytes are transferred 8 bits at a time. The number of ECC bytes are 4 or 22 according to setting of Set Feature option. The default setting is 4 bytes of ECC data.

The command makes a single attempt to read the data and does not check the data using ECC, whatever is read is returned to the host.

Output Parameters To The Device

Sector Count The number of continuous sectors to be transferred. The Sector Count must be set to one.

Sector Number The sector number of the sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

- H** The head number of the sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 24-27. (L=1)
- R** The retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

- Sector Count** The number of requested sectors not transferred.
- Sector Number** The sector number of the transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
- Cylinder High/Low** The cylinder number of the transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
- H** The head number of the transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 24-27. (L=1)

It should be noted that the device internally uses 22 bytes of ECC data on all data written or read from the disk. The 4 byte mode of operation is provided via an emulation. It is recommended that for testing the effectiveness and integrity of the devices ECC functions that the 22 byte ECC mode should be used.

11.12 Read Multiple (C4h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	0	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 69. Read Multiple Command (C4h)

The Read Multiple command reads one or more sectors of data from disk media, then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time. Command execution is identical to the Read Sectors command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector.

Output Parameters To The Device

- Sector Count** The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
- Sector Number** The sector number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 0 - 7. (L=1)
- Cylinder High/Low** The cylinder number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
- H** The head number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 24 - 27. (L=1)

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

11.13 Read Sectors (20h/21h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	0	1	0	0	0	0	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 70. Read Sectors Command (20h/21h)

The Read Sectors command reads one or more sectors of data from disk media, then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Output Parameters To The Device

Sector Count The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number The sector number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H The head number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 24 - 27. (L=1)

R The retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

11.14 Read Verify Sectors (40h/41h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	0	1	0	0	0	0	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 71. Read Verify Sectors Command (40h/41h)

The Read Verify Sectors verifies one or more sectors on the device. No data is transferred to the host.

The difference of Read Sectors command and Read Verify Sectors command is whether the data is transferred to the host or not.

If an uncorrectable error occurs, the read verify will be terminated at the failing sector.

Output Parameters To The Device

- Sector Count** The number of continuous sectors to be verified. If zero is specified, then 256 sectors will be verified.
- Sector Number** The sector number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 0 - 7. (L=1)
- Cylinder High/Low** The cylinder number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
- H** The head number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 24 - 27. (L=1)
- R** The retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

Sector Count	The number of requested sectors not verified. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

11.15 Recalibrate (1xh)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	0	0	0	1	-	-	-	-

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	V	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 72. Recalibrate Command (1xh)

The Recalibrate command moves the read/write heads from anywhere on the disk to cylinder 0.

If the device cannot reach cylinder 0, T0N (Track 0 Not Found) will be set in the Error Register.

11.16 Seek (7xh)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	1	1	1	-	-	-	-

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 73. Seek Command (7xh)

The Seek command initiates a seek to the designated track and selects the designated head. The device need not be formatted for a seek to execute properly.

Output Parameters To The Device

Sector Number In LBA mode, this register specifies LBA address bits 0 - 7 for seek. (L=1)

Cylinder High/Low The cylinder number of the seek.

In LBA mode, this register specifies LBA address bits 8 - 15 (Low), 16 - 23 (High) for seek. (L=1)

H The head number of the seek.

In LBA mode, this register specifies LBA address bits 24 - 27 for seek. (L=1)

Input Parameters From The Device

Sector Number In LBA mode, this register contains current LBA bits 0 - 7. (L=1)

Cylinder High/Low In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

11.17 Set Features (EFh)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	V	V	V	V	V	V	V	V
Sector Count	Note.1							
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	1	1	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 74. Set Features Command (EFh)

The Set Feature command is to establish the following parameters which affect the execution of certain features as shown in below table.

ABT will be set to 1 in the Error Register if the Feature register contains any undefined values.

Output Parameters To The Device

Feature	Destination code for this command.
02H	Enable write cache
03H	Set transfer mode based on value in sector count register
44H	22 bytes of ECC apply on Read Long/Write Long commands
55H	Disable read look-ahead feature
66H	Disable reverting to power on defaults
82H	Disable write cache
AAH	Enable read look-ahead feature
BBH	4 bytes of ECC apply on Read Long/Write Long commands
CCH	Enable reverting to power on defaults

Note 1.

When Feature register is 03h (=Set Transfer mode), the Sector Count Register specifies the transfer mechanism. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value.

PIO Default Transfer Mode	00000	000
PIO Default Transfer Mode,Disable IORDY	00000	001
PIO Flow Control Transfer Mode x	00001	nnn (nnn=000,001,010,011,100)
Single word DMA mode x	00010	nnn (nnn=000,001,010)
Multiword DMA mode x	00100	nnn (nnn=000,001,010)

Note 2.

If the number of auto reassigned sector reaches the device's reassignment capacity, the write cache function will be automatically disabled. Although the device still accepts the Set Features command with Feature register = 02h without error, but the write cache function will remains disabled. For current write cache function status, please refer to Identify Device Information(129word) by Identify Device command.

Note 3.

After power on reset, the features listed below are set to power on default as shown in the list.
After hard reset while Reverting to power on defaults is enabled, the features listed below are set to power on default as shown in the list.

Write cache	:	Enable
ECC bytes	:	4 bytes
Read look-ahead	:	Enable
Reverting to power on defaults	:	Disable

11.18 Set Multiple (C6h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	0	0	0	1	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 75. Set Multiple Command (C6h)

The Set Multiple command enables the device to perform Read and Write Multiple commands and establishes the block size for these commands. The block size is the number of sectors to be transferred for each interrupt.

The default block size after power up, soft reset, or hard reset is 0, and Read Multiple and Write Multiple commands are disabled.

If an invalid block size is specified, an Abort error will be returned to the host, and Read Multiple and Write Multiple commands will be disabled.

Output Parameters To The Device

Sector Count. The block size to be used for Read Multiple and Write Multiple commands. Valid block sizes can be selected from 0, 2, 4, 8 or 16. If 0 is specified, then Read Multiple and Write Multiple commands are disabled.

11.19 Sleep (E6h/99h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	1	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 76. Sleep Command (E6h/99h)

This command causes the device to enter Sleep Mode.

The device is spun down but the interface remains active. If the device is already spun down, the spin down sequence is not executed.

11.20 S.M.A.R.T. Function Set (B0h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	V	V	V	V	V	V	V	V
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	0	1	0	0	1	1	1	1
Cylinder High	1	1	0	0	0	0	1	0
Device/Head	1	-	1	D	-	-	-	-
Command	1	0	1	1	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 77. S.M.A.R.T. Function Set Command (B0h)

The S.M.A.R.T. Function Set command provides access to Attribute Values, Attribute Thresholds and other low level subcommands that can be used for logging and reporting purposes and to accommodate special user needs. The S.M.A.R.T. Function Set command has several separate subcommands which are selectable via the device's Features Register when the S.M.A.R.T. Function Set command is issued by the host.

In order to select a subcommand the host must write the subcommand code to the device's Features Register before issuing the S.M.A.R.T. Function Set command. The subcommands and their respective codes are listed below.

Code	Subcommand
D0h	SMART Read Attribute Values
D1h	SMART Read Attribute Thresholds
D2h	SMART Enable/disable Attribute Autosave
D3h	SMART Save Attribute Values
D4h	SMART Execute Off-line Data Collection
D8h	SMART Enable Operations
D9h	SMART Disable Operations

11.20.1.1 SMART Read Attribute Values (Subcommand D0h)

This subcommand returns the device's Attribute Values to the host. Upon receipt of the SMART Read Attribute Values subcommand from the host, the device saves any updated Attribute Values to the Attribute Data sectors, and then transfers the 512 bytes of Attribute Value information to the host.

11.20.1.2 SMART Read Attribute Thresholds (Subcommand D1h)

This subcommand returns the device's Attribute Thresholds to the host. Upon receipt of the SMART Read Attribute Thresholds subcommand from the host, the device reads the Attribute Thresholds from the Attribute Threshold sectors, and then transfers the 512 bytes of Attribute Thresholds information to the host.

11.20.1.3 SMART Enable/Disable Attribute Autosave (Subcommand D2h)

DAQA-3xxxx does not support the Attribute Autosave feature. This subcommand is supported for the system which might require that the device responds without error for the subcommand.

The valid value written by host into the Sector Count register is 00h or F1h.

Upon receipt of the subcommand from host, the device saves any updated Attribute Values to the disk.

11.20.1.4 SMART Save Attribute Values (Subcommand D3h)

This subcommand causes the device to immediately save any updated Attribute Values to the device's Attribute Data sector regardless of the state of the Attribute Autosave feature. Upon receipt of the SMART Save Attribute Values subcommand from the host, the device writes any updated Attribute Values to the Attribute Data sector.

11.20.1.5 SMART Execute Off-line Data Collection (Subcommand D4h)

DAQA-3xxxx does not have the off-line data collection capability. This subcommand is supported for the system which might require that the device responds without error for the subcommand.

Upon receipt of the subcommand from host, the device performs no operation.

11.20.1.6 SMART Enable Operations (Subcommand D8h)

This subcommand enables access to all S.M.A.R.T. capabilities within the device. Prior to receipt of a SMART Enable Operations subcommand, Attribute Values are neither monitored nor saved by the device. The state of S.M.A.R.T. (either enabled or disabled) will be preserved by the device across power cycles. Once enabled, the receipt of subsequent SMART Enable Operations subcommands will not affect any of the Attribute Values.

Upon receipt of the SMART Enable Operations subcommand from the host, the device enables S.M.A.R.T. capabilities and functions, and then saves any updated Attribute Values to the Attribute Data sector.

11.20.1.7 SMART Disable Operations (Subcommand D9h)

This subcommand disables all S.M.A.R.T. capabilities within the device including any functions related exclusively to this feature. (e.g., the device's attribute autosave feature) After receipt of the SMART Disable Operations subcommand the device will disable all S.M.A.R.T. Operations. Attribute Values will no longer be monitored or saved by the device. The state of S.M.A.R.T. (either enabled or disabled) will be preserved by the device across power cycles.

Upon receipt of the SMART Disable Operations subcommand from the host, the device disables S.M.A.R.T. capabilities and functions, and then saves any updated Attribute Values to the Attribute Data sector.

After receipt of the device of the SMART Disable Operations subcommand from the host, all other S.M.A.R.T. subcommands -- with the exception of SMART Enable Operations -- are disabled and invalid and will be aborted by the device (including the SMART Disable Operations subcommand), returning the error code as specified in Figure 83 on page 116.

Any Attribute Values accumulated and saved to volatile memory prior to receipt of the SMART Disable Operations command will be preserved in the device's Attribute Data Sectors. If the device is re-enabled, these Attribute Values will be updated, as needed, upon receipt of a SMART Read Attribute Values or SMART Save Attribute Values command.

11.20.1.8 SMART Return Status (Subcommand DAh)

This command is used to communicate the reliability status of the device to the host's request. Upon receipt of the SMART Return Status subcommand the device saves any updated Attribute Values to the reserved sector and compares the updated Attribute Values to the Attribute Thresholds.

If the device does not detect a Threshold Exceeded Condition, the device loads 4Fh into the Cylinder Low register, C2h into the Cylinder High register.

If the device detect a Threshold Exceeded Condition, the device loads F4h into the Cylinder Low register, 2Ch into the Cylinder High register.

11.20.2 Device Attributes Data Structure

The following defines the 512 bytes that make up the Attribute Value information. This data structure is accessed by the host in its entirety using the SMART Read Attribute Values subcommand. All multi-byte fields shown in these data structures follow the ATA-3 specification for byte ordering, namely that the least significant byte occupies the lowest numbered byte address location in the field.

Description	Bytes	Offset	Format	Value
Data Structure Revision Number	2	00h	binary	0005h
1st Device Attribute	12	02h	(*1)	(*2)
...	..			
...	..			
30th Device Attribute	12	15Eh	(*1)	(*2)
Off-line data collection status	1	16Ah	(*1)	(*2)
Total segments required for off-line data collection	1	16Bh	(*1)	07h
Total time in seconds to complete next segment	2	16Ch	(*1)	(*2)
Current segment pointer	1	16Eh	(*1)	(*2)
Off-line data collection capability	1	16Fh	(*1)	05h
S.M.A.R.T. capability	2	170h	(*1)	01h
Reserved	16	172h		(*3)
Vendor specific	125	182h		(*3)
Data structure checksum	1	1FFh		(*2)
	512			

(*1) – See following definitions

(*2) – Value varied by actual operating condition

(*3) – Filled with 00h

Figure 78. Device Attribute Data Structure

11.20.2.1 Data Structure Revision Number

The Data Structure Revision Number identifies which version of this data structure is implemented by the device. This revision number will be set to 0005h. This revision number identifies both the Attribute Value and Attribute Threshold Data structures.

11.20.2.2 Individual Attribute Data Structure

The following defines the 12 bytes that make up the information for each Attribute entry in the Device Attribute Data Structure.

Description	Bytes	Offset	Format
Attribute ID Number (01h to FFh)	1	00h	binary
Status Flags	2	01h	bit flags
Pre-Failure/Advisory bit			
On-line Collection bit			
Vendor Specific (4 bits)			
Reserved (10 bits, all 0)			
Attribute Value (valid values from 01h to FEh)	1	03h	binary
00h invalid for attribute value – not to be used			
01h minimum value			
64h initial value for all attributes prior to any data collection			
FDh maximum value			
FEh value is not valid			
FFh invalid for attribute value – not to be used			
Vendor Specific	8	04h	binary
Total Bytes	12		

Figure 79. Individual Attribute Data Structure

11.20.2.2.1 Attribute ID Numbers: Any non-zero value in the Attribute ID Number indicates an active attribute. The device supports following Attribute ID Numbers.

ID	Attribute Name
0	Indicates that this entry in the data structure is not used
1	Raw Read Error Rate
3	Spin Up Time
4	Start/Stop Count
5	Reallocated Sector Count
7	Seek Error Rate
9	Power-On Hours Count
10	Spin Retry Count
12	Device Power Cycle Count

11.20.2.2.2 Status Flag Definitions

Bit	Flag Name	Definition
0	Pre-Failure/ Advisory bit	If bit = 0, an Attribute Value less than or equal to its corresponding Attribute Threshold indicates an Advisory condition where the usage or age of the device has exceeded its intended design life period. If bit = 1, an Attribute Value less than or equal to its corresponding Attribute Threshold indicates a Pre-Failure condition where imminent loss of data is being predicted.
1	On-Line Collective bit	If bit = 0, the Attribute Value is updated only during Off-Line testing. If bit = 1, the Attribute Value is updated only during On-Line testing
2- 5	Vendor Specific	
6-15	Reserved bits	Always 0

Figure 80. Status Flag Definitions

11.20.2.2.3 Normalized Values: The device will perform conversion of the raw Attribute Values to transform them into normalized values, which the host can then compare with the Threshold values. A Threshold is the excursion limit for a normalized Attribute Value. In normalizing the raw data, the device will perform any necessary statistical validity checks to ensure that an instantaneous raw value is not improperly reflected in the normalized Attribute Value (i.e., one read error in the first 10 reads being interpreted as exceeding the read error rate threshold when the subsequent 1 billion reads all execute without error). The end points for the normalized values for all Attributes will be 1 (01h) at the low end, and 100 (64h) at the high end for the device which is ready for customer shipment. For Performance and Error Rate Attributes, values greater than 100 are also possible, up to a maximum value of 253 (FDh).

11.20.2.3 Off-Line Data Collection Status

The value of this byte defines the current status of the off-line activities of the device. Bit 7 indicates Automatic Off-Line Data Collection Status.

Bit 7 Automatic Off-Line Data Collection Status

0 Automatic Off-Line Data Collection is enabled.

1 Automatic Off-Line Data Collection is disabled.

Bits 0 thru 6 represents a hexadecimal status value reported by the device.

Value Definition

0 Off-line data collection never started

- 1 Segment completed without error
- 2 All segments completed without errors. In this case, current segment pointer equals to total segments required.
- 5 Off-line data collecting aborted by interrupting command
- 6 Off-line data collection aborted with fatal error

11.20.2.4 Total Segments Required for Off-line Data Collection

The device will return 07h as the total segments for off-line data collection.

11.20.2.5 Total Time in Seconds to Complete Next Segment

This field tells the host how many seconds the device requires to complete the segment pointed by the current segment pointer. The host can use this time to set a count down timer that will trigger it to issue the “SMART Read Attribute Values” subcommand to check on the status of off-line data collection. This field indicates the total time in seconds for the first segment if the current segment pointer is 00h or the off-line status indicates all segments completed (02h).

11.20.2.6 Current Segment Pointer

This byte is a counter indicating the next segment to execute as an off-line data collection activity. This varies from 00h to the total number of segments. The current segment pointer will be 00h if the off-line data collection has not been started. If the off-line data collection is aborted by a command or an error (i.e., the status is 05h or 06h), this byte will point to the aborted segment. If the all segments complete, this byte will equal to the total number of segments.

11.20.2.7 Off-Line Data Collection Capability

The device returns 05h as its off-line data collection capability which indicates: the Execute Off-Line Data Collection Immediate is implemented; the device will abort all off-line activity if interrupted by a new command.

11.20.2.8 S.M.A.R.T. Capability

This word of bit flags describes the S.M.A.R.T. capabilities of the device. The device will return 01h indicating that the device has pre-power down mode attribute saving capability.

Bit	Definition
------------	-------------------

0	Pre-power mode attribute saving capability
----------	--

If bit = 1, the device will save its Attribute Values prior to going into a power saving mode (Standby or Sleep mode).

1	Attribute autosave capability
----------	-------------------------------

If bit = 1, the device will save its Attribute Values after some predetermined event.

11.20.2.9 Data Structure Checksum

The Data Structure Checksum is the 2's compliment of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

11.20.3 Device Attribute Thresholds Data Structure

The following defines the 512 bytes that make up the Attribute Threshold information. This data structure is accessed by the host in its entirety using the SMART Read Attribute Thresholds. All multi-byte fields shown in these data structures follow the ATA-2 specification for byte ordering, namely that the least significant byte occupies the lowest numbered byte address location in the field.

The sequence of active Attribute Thresholds will appear in the same order as their corresponding Attribute Values.

Description	Bytes	Offset	Format	Value
Data Structure Revision Number	2	00h	binary	0005h
1st Attribute Threshold	12	02h	(*1)	(*2)
...	..			
...	..			
30th Attribute Threshold	12	15Eh	(*1)	(*2)
Reserved	18	16Ah		(*3)
Vendor specific	131	17Ch		(*3)
Data structure checksum	1	1FFh		(*2)
	512			

(*1) – See following definitions

(*2) – Value varied by actual operating condition

(*3) – Filled with 00h

Figure 81. Device Attribute Thresholds Data Structure

11.20.3.1 Data Structure Revision Number

This value (0005h) is the same as the value used in the Device Attributes Values Data Structure.

11.20.3.2 Individual Thresholds Data Structure

The following defines the 12 bytes that make up the information for each Threshold entry in the Device Attribute Thresholds Data Structure. Attribute entries in the Individual Threshold Data Structure is in the same order and correspond to the entries in the Individual Attribute Data Structure.

Description	Bytes	Offset	Format
Attribute ID Number (01h to FFh)	1	00h	binary
Attribute Threshold (for comparison with Attribute Values from 00h to FFh)	1	01h	binary
00h – "always passing" threshold value to be used for code test purposes			
01h – minimum value for normal operation			
FDh – maximum value for normal operation			
FEh – invalid for threshold value			
FFh – "always failing" threshold value to be used for code test purposes			
Reserved (00h)	10	02h	binary
Total Bytes	12		

Figure 82. Individual Threshold Data Structure

11.20.3.3 Attribute ID Numbers

Attribute ID Numbers supported by the device are the same as Attribute Values Data Structures.

11.20.3.4 Attribute Threshold

These values are preset at the factory and are not meant to be changeable.

11.20.3.5 Data Structure Checksum

The Data Structure Checksum is the 2's compliment of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

11.20.4 Error Reporting

The following table shows the values returned in the Status and Error Registers when specific error conditions are encountered by a device.

Error Condition	Status Register	Error Register
A S.M.A.R.T. FUNCTION SET command was received by the device without the required key being loaded into the Cylinder High and Cylinder Low registers.	51h	04h
A S.M.A.R.T. FUNCTION SET command was received by the device with a subcommand value in the Features Register that is either invalid or not supported by this device.	51h	04h
A S.M.A.R.T. FUNCTION SET command subcommand other than SMART ENABLE OPERATIONS was received by the device while the device was in a "S.M.A.R.T. disabled" state.	51h	04h
The device is unable to read its Attribute Values or Attribute Thresholds data structure.	51h	10h or 40h
The device is unable to write to its Attribute Values data structure.	51h	10h or 01h
The Data Structure Revision Number in the device's Attribute Values data structure does not match the Data Structure Revision Number in the device's Attribute Thresholds data structure.	51h	01h
A mismatch has occurred between the entries in the device's Attribute Values data structure and Attribute Thresholds data structure.	51h	01h
The device has detected a checksum error in its Attribute Threshold data structure.	51h	10h

Figure 83. S.M.A.R.T. Error Codes

11.21 Standby (E2h/96h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	0	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 84. Standby Command (E2h/96h)

The Standby command causes the device to enter the Standby Mode immediately, and set auto power down timeout parameter(standby timer).

When the Standby mode is entered, the device is spun down but the interface remains active. If the device is already spun down, the spin down sequence is not executed.

During the Standby mode the device will respond to commands, but there is a delay while waiting for the spindle to reach operating speed.

The timer starts counting down when the device returns to Idle mode.

Output Parameters To The Device

Sector Count Timeout Parameter. If zero, then the automatic power down sequence is disabled. If non-zero, then the automatic power down sequence is enabled, and the timeout interval is set of the Timeout Parameter times 5, in seconds, for the value range from 12 to 255. If the value is 1 to 11, the Timeout Value is 60 seconds.

When the automatic power down sequence is enabled, the drive will enter Standby mode automatically if the timeout interval expires with no drive access from the host. The timeout interval will be reinitialized if there is a drive access before the timeout interval expires.

11.22 Standby Immediate (E0h/94h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 85. Standby Immediate Command (E0h/94h)

The Standby Immediate command causes the device to enter Standby mode immediately.

The device is spun down but the interface remains active. If the device is already spun down, the spin down sequence is not executed.

During the Standby mode, the device will respond to commands, but there is a delay while waiting for the spindle to reach operating speed.

The Standby Immediate command will not affect to auto power down timeout parameter.

11.23 Write Buffer (E8h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 86. Write Buffer Command (E8h)

The Write Buffer command transfers a sector of data from the host to the sector buffer of the device. The sectors of data are transferred through the Data Register 16 bits at a time.

The Read Buffer and Write Buffer commands are synchronized such that sequential Write Buffer and Read Buffer commands access the same 512 byte within buffer.

11.24 Write DMA (CAh/CBh)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	1	0	1	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 87. Write DMA Command (CAh/CBh)

The Write DMA command transfers one or more sectors of data from the host to the device, then the data is written to the disk media.

The sectors of data are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. Data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Output Parameters To The Device

Sector Count The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number The sector number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

- H** The head number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 24 - 27. (L=1)
- R** The retry bit. If set to one, then retries are disabled. But ignored, when write cache is enabled. (Ignoring the retry bit is in violation of ATA-2.)

Input Parameters From The Device

- Sector Count** The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
- Sector Number** The sector number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
- Cylinder High/Low** The cylinder number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
- H** The head number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

11.25 Write Long (32h/33h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	0	0	0	0	0	0	0	1
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	0	1	1	0	0	1	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 88. Write Long Command (32h/33h)

The Write Long command transfers the data and the ECC bytes of the designated one sector from the host to the device, then the data and the ECC bytes are written to the disk media.

After 512 bytes of data have been transferred, the device will keep setting DRQ=1 to indicate that the device is ready to receive the ECC bytes from the host. The data is transferred 16 bits at a time, and the ECC bytes are transferred 8 bits at a time. The number of ECC bytes are 4 or 22 according to setting of Set Feature option. The default number after power on is 4 bytes.

Output Parameters To The Device

- Sector Count** The number of continuous sectors to be transferred. The Sector Count must be set to one.
- Sector Number** The sector number of the sector to be transferred. (L=0)
 In LBA mode, this register contains LBA bits 0 - 7. (L=1)
- Cylinder High/Low** The cylinder number of the sector to be transferred. (L=0)
 In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
- H** The head number of the sector to be transferred. (L=0)
 In LBA mode, this register contains LBA bits 24 - 27. (L=1)
- R** The retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred.
Sector Number	The sector number of the sector to be transferred. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the sector to be transferred. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the sector to be transferred. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

The file internally uses 22 bytes of ECC on all data read or writes. The 4 byte mode of operation is provided via an emulation technique. As a consequence of this emulation it is recommended that 22 byte ECC mode is used for all tests to confirm the operation of the files ECC hardware. Unexpected results may occur if such testing is performed using 4 byte mode.

11.26 Write Multiple (C5h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	0	1	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 89. Write Multiple Command (C5h)

The Write Multiple command transfers one or more sectors from the host to the device, the the data is written to the disk media.

Command execution is identical to the Write Sectors command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector. The sectors are transferred through the Data Register 16 bits at a time.

Output Parameters To The Device

Sector Count The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number The sector number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H The head number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 24 - 27. (L=1)

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

11.27 Write Sectors (30h/31h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	1	L	1	D	H	H	H	H
Command	0	0	1	1	0	0	0	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 90. Write Sectors Command (30h/31h)

The Write Sectors command transfers one or more sectors from the host to the device, then the data is written to the disk media.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Output Parameters To The Device

- Sector Count** The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
- Sector Number** The sector number of the first sector to be transferred. (L=0)
 In LBA mode, this register contains LBA bits 0 - 7. (L=1)
- Cylinder High/Low** The cylinder number of the first sector to be transferred. (L=0)
 In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
- H** The head number of the first sector to be transferred. (L=0)
 In LBA mode, this register contains LBA bits 24 - 27. (L=1)
- R** The retry bit. If set to one, then retries are disabled. But ignored, when write cache is enabled. (Ignoring the retry bit is in violation of ATA-2.)

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

12.0 Timings

The timing of BSY and DRQ in Status Register are shown in Figure 91

The other timings are described in 6.1.4, “ Reset Timings” on page 23 through 6.1.7, “ DMA Timings (Multiword)” on page 27.

FUNCTION	INTERVAL	START	STOP	TIMEOUT
Power On	Device Busy After Power On	Power On	Status Register BSY=1	400 ns
	Device Ready After Power On	Power On	Status Register BSY=0 and RDY=1	31 sec
Software Reset	Device Busy After Software Reset	Device Control Register RST=1	Status Register BSY=1	400 ns
	Device Ready After Software Reset	Device Control Register RST=1	Status Register BSY=0 and RDY=1	6 sec
Hard Reset	Device Busy After Hard Reset	Bus RESET Signal Asserted	Status Register BSY=1	400 ns
	Device Ready After Hard Reset	Bus RESET Signal Asserted	Status Register BSY=0 and RDY=1	31 sec
Data In Command	Device Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns
	Interrupt, DRQ For Data Transfer In	Status Register BSY=1	Status Register BSY=0 and DRQ=1, Interrupt	30 sec
	Device Busy After Data Transfer In	256th Read From Data Register	Status Register BSY=1	10 us
Data Out Command	Device Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns
	Data Request For Data Transfer Out	Status Register BSY=1	Status Register BSY=0 and DRQ=1	700 us
	Device Busy After Data Transfer Out	256th Write From Data Register	Status Register BSY=1	5 us
	Interrupt For Data Transfer Out	Status Register BSY=1	Status Register BSY=0 and RDY=1 Interrupt	30 sec

Figure 91. Timeout Values

FUNCTION	INTERVAL	START	STOP	TIMEOUT
Non-Data Command	Device Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns
	Interrupt For Command Complete	Status Register BSY=1	Interrupt	30 sec
DMA Data Transfer Command	Device Busy after Command Code Out	Out to Command Register	Status Register BSY=1	400 ns

Figure 92. Timeout Values --- Continued ---

Command category is referred to 10.0, “ Command Protocol” on page 67.

The abbreviations "ns", "us", "ms" and "sec" mean nanoseconds, microseconds, milliseconds and seconds, respectively.

We recommend that the host system executes Soft reset and then retry to issue the command if the host system would occur timeout for the device.

13.0 Appendix

13.1 Commands Support Coverage

Following table is provided to facilitate the understanding of DAQA-3xxxx command support coverage comparing to the ATA-3 defined command set. The column of 'Implementation' shows the capability of DAQA-3xxxx for those commands.

Command Code	Command Name		Implementation for DAQA-2XXXX	ATA-3 Category
00h	NOP		No	Optional
01h-0Fh	Reserved		Reserved	Reserved
1xh	RECALIBRATE		Yes	Optional
20h	READ SECTOR(S)	(w/ retry)	Yes	Mandatory
21h	READ SECTOR(S)	(w/o retry)	Yes	Mandatory
22h	READ LONG	(w/ retry)	Yes	Optional
23h	READ LONG	(w/o retry)	Yes	Optional
24h-2Fh	Reserved		Reserved	Reserved
30h	WRITE SECTOR(S)	(w/ retry)	Yes	Mandatory
31h	WRITE SECTOR(S)	(w/o retry)	Yes	Mandatory
32h	WRITE LONG	(w/ retry)	Yes	Optional
33h	WRITE LONG	(w/o retry)	Yes	Optional
34h-3Bh	Reserved		Reserved	Reserved
3Ch	WRITE VERIFY (2)		No	Optional
3Dh-3Fh	Reserved		Reserved	Reserved
40h	READ VERIFY SECTOR(S)	(w/ retry)	Yes	Mandatory
41h	READ VERIFY SECTOR(S)	(w/o retry)	Yes	Mandatory
42h-4Fh	Reserved		Reserved	Reserved
50h	FORMAT TRACK		Yes	Vendor specific
51h-5Fh	Reserved		Reserved	Reserved
60h-6Fh	Reserved		Reserved	Reserved
7xh	SEEK		Yes	Mandatory
8xh	Vendor specific		Reserved	Vendor specific
90h	EXECUTE DEVICE DIAGNOSTIC		Yes	Mandatory
91h	INITIALIZE DEVICE PARAMETERS		Yes	Mandatory
92h	DOWNLOAD MICROCODE		No	Optional
93h	Reserved		Reserved	Reserved
94h,E0h	STANDBY IMMEDIATE (1)		Yes	Optional (2)
95h,E1h	IDLE IMMEDIATE (1)		Yes	Optional (2)
96h,E2h	STANDBY (1)		Yes	Optional (2)
97h,E3h	IDLE (1)		Yes	Optional (2)
98h,E5h	CHECK POWER MODE (1)		Yes	Optional (2)
99h,E6h	SLEEP (1)		Vendor specific	Optional (2)
9Ah	Vendor specific		Reserved	Vendor specific
9Bh-9Fh	Reserved		Reserved	Reserved
A0h-AFh	Reserved		Reserved	Reserved

Figure 93. Command coverage

Command Code	Command Name	Implementation for DAQA-3XXXX	ATA-3 Category
B0h	SMART FUNCTION SET	Yes	Optional - (4)
B1h-BFh	Reserved	Reserved	Reserved
C0h-C3h	Vendor specific	Reserved	Vendor specific
C4h	READ MULTIPLE	Yes	Optional
C5h	WRITE MULTIPLE	Yes	Optional
C6h	SET MULTIPLE MODE	Yes	Optional
C7h	Reserved	Reserved	Reserved
C8h	READ DMA (w/ retry)	Yes	Optional
C9h	READ DMA (w/o retry)	Yes	Optional
CAh	WRITE DMA (w/ retry)	Yes	Optional
CBh	WRITE DMA (w/o retry)	Yes	Optional
CCh-CFh	Reserved	Reserved	Reserved
D0h-DAh	Reserved	Reserved	Reserved
DBh	ACKNOWLEDGE MEDIA CHANGE	No	Optional - (5)
DCh	BOOT - POST-BOOT	No	Optional - (5)
DDh	BOOT - PRE-BOOT	No	Optional - (5)
DEh	DOOR LOCK	No	Optional - (5)
DFh	DOOR UNLOCK	No	Optional - (5)
E0h,94h	STANDBY IMMEDIATE (1)	Yes	Optional - (2)
E1h,95h	IDLE IMMEDIATE (1)	Yes	Optional - (2)
E2h,96h	STANDBY (1)	Yes	Optional - (2)
E3h,97h	IDLE (1)	Yes	Optional - (2)
E4h	READ BUFFER	Yes	Optional
E5h,98h	CHECK POWER MODE (1)	Yes	Optional - (2)
E6h,99h	SLEEP (1)	Vendor specific	Optional - (2)
E7h	Reserved	Reserved	Reserved
E8h	WRITE BUFFER	Yes	Optional
E9h	WRITE SAME	No	Optional
EAh-EBh	SECURE MODE SET	No	Optional - (3)
ECh	IDENTIFY DEVICE	Yes	Mandatory
EDh	MEDIA EJECT	No	Optional - (5)
EEh	IDENTIFY DEVICE DMA	Yes	Optional
EFh	SET FEATURES	Yes	Optional
F0h	Vendor specific	Reserved	Vendor specific
F1h	SET PASSWORD (3)	No	Optional
F2h	UNLOCK (3)	No	Optional
F3h	ERASE PREPARE (3)	No	Optional
F4h	ERASE UNIT (3)	No	Optional
F5h	FREEZE LOCK (3)	No	Optional
F6h	DISABLE PASSWORD (3)	No	Optional
F7h-FFh	Vendor specific	Reserved	Vendor specific

- Note:(1) These commands have two command codes and appear in this table twice, once for each command code.
(2) Power Management Feature Set
(3) Secure Mode Feature Set (Not supported)
(4) S.M.A.R.T. Function Set
(5) Removable

Figure 94. Command coverage --- Continued ---

13.2 SET FEATURES Command Support Coverage

Following table is provided to facilitate the understanding of DAQA-3xxxx "Set Features" command support coverage comparing to the ATA-3 defined command set. The column of 'Implementation' shows the capability of DAQA-3xxxx for those commands. For detail operation, refer to 11.17, "Set Features (EFh)" on page 103.

Features Register	Features Name	Implementation for DAQA-3XXXX	ATA-3 Category
01h	Enable 8 bit data transfers	No	Optional
02h	Enable write cache	Yes	Vendor specific
03h	Set transfer mode	Yes	Optional
04h	Enable all auto reassignment	No	Vendor specific
33h	Disable retry	No	Vendor specific
44h	Set vendor specific bytes ECC	Yes	Optional
54h	Set cache segments	No	Vendor specific
55h	Disable read look-ahead feature	Yes	Optional
66h	Disable reverting to power on defaults	Yes	Optional
77h	Disable ECC	No	Vendor specific
81h	Disable 8 bit data transfers	No	Optional
82h	Disable write cache	Yes	Vendor specific
84h	Disable all auto reassignment	No	Vendor specific
88h	Enable ECC	No	Vendor specific
99h	Enable retries	No	Vendor specific
9Ah	Set device maximum average current	No	Optional
AAh	Enable read look-ahead feature	Yes	Optional
ABh	Set maximum prefetch	No	Vendor specific
BBh	Set 4 bytes ECC	Yes	Optional
CCh	Enable reverting to power on defaults	Yes	Optional
others	Reserved	Reserved	Reserved

Figure 95. SET FEATURES Command coverage

Index

A

ABRT 54
ABT 54
AMN 55
AMNF 55
Auto Reassign Function 64
 Non recovered read errors 64
 Non recovered write errors 64
 Recovered read errors 64
Automatic Power Down Sequence 117

B

BBK 54
BSY 56

C

Check Power Mode 71, 77
Command
 Check Power Mode (E5h/98h) 77
 Execute Device Diagnostic (90h) 78
 Format Track (50h) 79
 Identify Device (ECh) 82
 Identify Device DMA (EEh) 86
 Idle (E3h/97h) 87
 Idle Immediate (E1h/95h) 88
 Initialize Device Parameters (91h) 89
 Read Buffer (E4h) 90
 Read DMA (C8h/C9h) 91
 Read Long (22h/23h) 93
 Read Multiple (C4h) 95
 Read Sectors (20h/21h) 97
 Read Verify Sectors (40h/41h) 99
 Recalibrate (1xh) 101
 S.M.A.R.T. Function Set (B0h) 107
 Seek (7xh) 102
 Set Features (EFh) 103
 Set Multiple (C6h) 105
 Sleep (E6h/99h) 106
 Sleep Mode 49
 Standby (E2h/96h) 117
 Standby Immediate (E0h/94h) 118
 Write Buffer (E8h) 119
 Write DMA (CAh/CBh) 120
 Write Long (32h/33h) 122
 Write Multiple (C5h) 124
 Write Sectors (30h/31h) 126
Commands support Coverage 131
COR 56
CORR 56

D

D 76
DF 56
Diagnostic
 Diagnostic and Reset considerations 59
Diagnostic and Reset considerations 59
Diagnostic Codes 54, 58, 78
DRDY 56
DRQ 56
DRV 54
DS0 53
DS1 53
DSC 56

E

ERR 56
Error Register
 Diagnostic Codes 58
Execute Device Diagnostic 71, 78

F

Format Track 69, 79

H

H 76
H0 53
H1 53
H2 53
H3 53
Hard Reset 49
HS0 54
HS1 54
HS2 54
HS3 54

I

Identify Device 67, 82
Identify Device DMA 72, 86
Idle 71, 87
Idle Immediate 71, 88
IDN 54
IDNF 54
IDX 56
IEN 53
Initialize Device Parameters 71, 89

L

L 54, 76

LBA Addressing Mode 60
Logical CHS Addressing Mode 60

M

Master 54

P

Power Management Feature 61
 Interface Capability for Power Modes 61
 Power Management Commands 61
 Power Mode 61
 Standby timer 61

R

R 76
RDY 56
Read Buffer 67, 90
Read DMA 72, 91
Read Long 67, 93
Read Multiple 67, 95
Read Sectors 67, 97
Read Verify Sectors 71, 99
Reassign Function 64
Recalibrate 71, 101
Register
 Alternate Status Register 51
 Command Register 52
 Cylinder High Register 52
 Cylinder Low Register 52
 Data Register 52
 Device Control Register 52
 Device/Head Register 53
 Drive Address Register 53
 Error Register 54
 Features Register 55
 Register Initialization 58
 Sector Count Register 55
 Sector Number Register 55
 Status Register 55
Register Initialization 58
Reset
 Diagnostic and Reset considerations 59
 Register Initialization 58
RST 53

S

S.M.A.R.T. Function 63
 Attribute thresholds 63
 Attribute values 63
 Attributes 63
 S.M.A.R.T. commands 63
 Threshold exceeded condition 63
S.M.A.R.T. Function Set 107
Sector Addressing Mode 60
 LBA Addressing Mode 60

Sector Addressing Mode (*continued*)
 Logical CHS Addressing Mode 60
Seek 71, 102
Set Features 71, 103
SET FEATURES Command support Coverage 133
Set Multiple 105
Set Multiple Mode 71
Slave 54
Sleep 71, 106
Sleep Mode 49
SMART Disable Operations 71
SMART Enable Operations 71
SMART Enable/Disable Attribute Autosave 71
SMART Execute Off-line Data Collection 71
SMART Read Attribute Thresholds 67
SMART Read Attribute Values 67
SMART Return Status 71
SMART Save Attribute Values 71
SRST 53
Standby 71, 117
Standby Immediate 71, 118

T

T0N 54
Timeout Interval 53, 129
Timeout Parameter 87, 117
TK0NF 54

U

UNC 54

V

V 76

W

Write Buffer 69, 119
Write Cache 65
Write Cache Jumper 65
Write DMA 72, 120
Write Long 69, 122
Write Multiple 69, 124
Write Sectors 69, 126
WTG 53

X

x 76



S46H-3342-05