



OEM HARD DISK DRIVE SPECIFICATIONS

for

DALA-3540 (541/528 MB)

3.5-Inch Hard Disk Drive with ATA Interface



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1.0 General

This document describes the characteristics of the following IBM 3.5-inch, ATA interface hard disk drives (hereinafter called "drive"). These drives are convertible by using one jumper (jumper position 7) i.e. they are same except for the jumper attachment. The capacity can be 541 MB with the jumper and 528 MB without the jumper.

- DALA-3540 (541 MB two heads)
- DALA-3540 (528 MB two heads)

1.1 Glossary

<i>Word</i>	<i>Meaning</i>
Kbpi	1000 Bits Per Inch
Mbps	1000 000 Bits per second
MB	1000 000 bytes
KB	1000 bytes
32 KB	32 x 1024 bytes
64 KB	64 x 1024 bytes
Mb/sq.in	1000 000 bits per square inch
MLC	Machine Level Control

1.2 General Caution

The drive can be damaged by shocks or ESD (Electric Static Discharge), so any damages applied to the drive after taking out from shipping package and opening ESD protective bag are user's responsibilities.

2.0 General Features

- 512 bytes/sector sector format.
- Write cache for sequential write operation
- 3 x 32 KB segmented sector buffer.
- PIO data transfer - mode 3 (11.1 MB/sec, Burst)
- DMA data transfer
 - Single word mode : mode 2 (8.3 MB/sec)
 - Multiword mode : mode 1 (11.1 MB/sec, Burst)
- CHS and LBA mode
- Selectable capacity of 541/528MB by a jumper attachment/detachment
- Advanced ECC on the fly (EOF)
- Automatic error recovery procedures for read and write commands
- Self diagnostics on power on and resident diagnostics
- Transparent defect management with ADR(Automatic Defect Reallocation) during write cache.
- 12 msec seek time in read operation.
- 4500 rpm disk rotation.
- Closed loop actuator servo
- Dedicated head landing zone
- Automatic actuator lock
- Power saving modes

3.0 Fixed Disk Characteristics

3.1 Formatted Capacity

Capacity (Model).	541 MB (DALA-3540)	528 MB (DALA-3540)
Jumper #7 (Note.1)	Attached	Not Attached
Logical Layout (Note.2)		
Number of Heads	16	16
Number of Sectors/Track	63	63
Number of Cylinders (Note.3)	1049	1024
Number of Sectors	1057 392	1032 192
Total logical Data Bytes	541 384 704	528 482 304

Figure 1. Formatted Capacity

Notes:

1. Capacity switch
Attach a jumper-#7 for 541 MB and remove it for 528 MB.
2. Logical Layout
Logical layout is imaginable drive parameters (i.e. numbers of Cylinder/Head/Sector) which are used to access the drive from system interface. Default setting can be obtained by issuing IDENTIFY DRIVE command.
3. Logical Cylinders
This number includes one cylinder which is to be used for diagnostic program use.

3.2 Data Sheet

Data transfer rates

- Buffer to/from media (Mbps)	32.25 - 48.75 Mbps
- Host to/from buffer (Interface transfer rate)	11.1 MB/sec(PIO)
	11.1 MB/sec(DMA)

Data buffer size 96 KB

- Number of buffer segments 3 x 32 KB

Rotational speed (RPM) 4500

Recording density (kbits/in) 68.4(Ave)/82.6(Max)

Track density (tracks/in) 5340

Areal Density (Mbits/in²) 365(Ave)/441(Max)

Data bands 8

3.3 Performance Characteristics

The performance is characterized by the following parameters:

- Command Overhead
- Mechanical Positioning
 - Seek Time
 - Latency
- Data Transfer Speed
- Buffering Operation (Lookahead/Write cache)

Note: All the above parameters contribute to the performance. There are other parameters that contribute to the performance of the actual system. This specification tries to define the bare drive characteristics, not the system throughput which will depend on the system and the application.

3.3.1 Command overhead

Command overhead is defined as the time required:

- for the command to be written into the command register by a host
- to the assertion of DRQ for the first data byte of a READ command when the requested data is not in the buffer
- exclude
 - Physical seek time
 - Latency time

Read Command Case (The drive is in quiescence state)	Time
Read(Cache not hit)	< 0.7 msec
Read(Cache hit)	< 0.6 msec
Write	< 0.5 msec
Seek	< 0.5 msec

Figure 2. Command Overhead

Note: The above table gives an average time.

3.3.2 Mechanical Positioning

3.3.2.1 Average Seek Time (Including Settling)

Command Type	Typical	Max
Read	12 msec	13 msec
Write	12.7 msec	14 msec

Figure 3. Mechanical Positioning Performance

"Typical" and "Max" are given throughout the performance specification by;

Typical Average of the drive population tested at nominal environmental and voltage conditions.
Max Maximum value measured on any one drive over the full range of the environmental and voltage conditions. (See section on Environment and D.C. Power Requirement.)

The seek time is measured from the start of motion of the actuator until **a reliable read or write operation may be started**. Reliable read or write implies that error correction/recovery is not employed to correct for arrival problems. The Average Seek Time is measured as the weighted average of all possible seek combinations.

$$\text{Weighted Average} = \frac{\sum_{n=1}^{\text{max}} (\text{max} + 1 - n) (\text{Tn.in} + \text{Tn.out})}{(\text{max} + 1) (\text{max})}$$

Where:

- max = Maximum Seek Length
- n = Seek Length (1 to max)
- Tn.in = Inward measured seek time for a n track seek
- Tn.out = Outward measured seek time for a n track seek

3.3.2.2 Full Stroke Seek

Function	Typical	Max
Read	20 msec	25 msec
Write	21 msec	27 msec

Figure 4. Full Stroke Seek Time

Full stroke seek for DALA-3540 is measured as the average of 1000 full stroke seeks with a **random head switch** from both directions (inward and outward).

3.3.2.3 Cylinder Switch Time (Cylinder Skew)

	Typical
Cylinder Switch Time	4.4 msec

Figure 5. Cylinder Switch Time

A cylinder switch time is defined as the amount of time required by the fixed disk to access the next sequential block after reading the last sector in the current cylinder.

3.3.2.4 Head Switch Time (Track Skew)

	Typical
Head Switch Time	3.5 msec

Figure 6. Head Switch Time

3.3.2.5 Average Latency

Rotational speed	Time for a revolution	Average Latency
4500 rpm	13.3 msec	6.67 msec

Figure 7. Latency Time

3.3.3 Drive Ready Time

Condition	Typical	Max
Power On to Ready	8 sec	31 sec

Figure 8. Drive Ready Time

- Ready** The condition in which the drive is able to perform a media access command (e.g. read, write) immediately.
- Power On** This includes the time required for the internal self diagnostics.

3.3.4 Data Transfer Speed

Description	TYPICAL
Disk-Buffer Transfer (Zone 0)	
(Instantaneous)	4.92 MB/sec
(Sustained)	3.85 MB/sec
Disk-Buffer Transfer (Zone 7)	
(Instantaneous)	3.23 MB/sec
(Sustained)	2.52 MB/sec
Buffer-Host	
(PIO)	11.1 MB/sec
(DMA - single word)	8.3 MB/sec
(DAM - multiword)	11.1 MB/sec

Figure 9. Data Transfer Speed

- Instantaneous disk-buffer transfer rate (MB/sec) is derived by:
 $(\text{Number of sectors on a track}) * 512 * (\text{revolution/sec})$
Note: Number of sectors per track will vary because of the linear density recording.
- Sustained disk-buffer transfer rate (Mbyte/sec) is defined by considering head/cylinder change time. This gives a local average data transfer rate. It is derived by:
 $(\text{Sustained Transfer Rate}) = A / (B + C + D)$
 $A = (\text{Number of data sectors per cylinder}) * 512$
 $B = (\# \text{ of Surface per cylinder} - 1) * (\text{Head switch time})$
 $C = (\text{Cylinder change time})$
 $D = (\# \text{ of surface}) * (\text{One revolution time})$
- Instantaneous Buffer-Host Transfer Rate (Mbyte/sec) defines the maximum data transfer rate on AT Bus. It also depends on the speed of the host.

3.3.5 Buffering Operation (Lookahead/Write cache)

In order to improve the total performance, the drive utilizes its own buffer for lookahead. The total of 96 KB of the buffer is divided into three segmented blocks. Those three segments are managed intelligently to obtain the best performance.

3.3.6 Operating Mode Definition

<i>Operating Mode</i>	<i>Description</i>
Spin-Up	Start up time from a disk-stop or power-down to get ready
Seek	Seek operation mode.
Write	Write operation mode.
Read	Read operation mode.
Idle	Disk-rotation and Servo-system are working normally. Commands can be received and processed immediately.
Standby / Sleep	Disk-rotation is stopped and commands can be received immediately. but write or read operations cannot begin until disk-rotation is spun-up and the Servo system is ready.

Note: Upon a power down or a disk-rotation-stop, a head locking mechanism will secure heads in a parking position.

Recovering from Standby mode does not need soft reset nor hard reset.

3.3.6.1 Mode Transition Time

Transition	Typical	Max
Standby → Idle	8 sec	31 sec
Idle → Standby	Immediate	Not Available

Figure 10. Mode Transition Time

Note: The actual spin down time will exist, however the command will be processed immediately.

4.0 Specifications

4.1 Power Connectors

One of two kinds of DC power connector is used for the drive to work.

One connector has four pins and the other has three pins.

4.1.1 Power Connector

The DC power connector is designed to mate with AMP (part 1-480424-0) using AMP pins (part 350078-4) strip or (part 61173-4) loose piece, or their equivalents. Pin assignments are shown below.

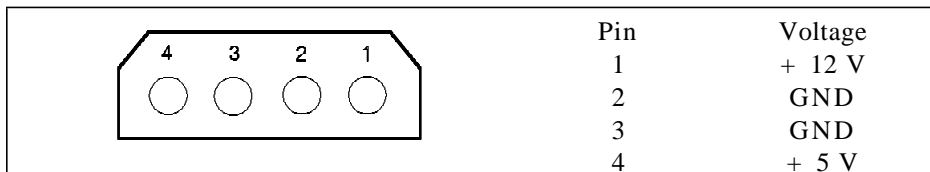


Figure 11. Power Connector Pin Assignments

4.1.2 Alternate Power Connector

The 3-pin DC power connector is designed to mate with the MOLEX (5480-03) using MOLEX pins (5479) or their equivalents. The pin assignments are shown in Figure 12.

Each line is connected to the corresponding voltage lines of the power connector as shown in Figure 11.

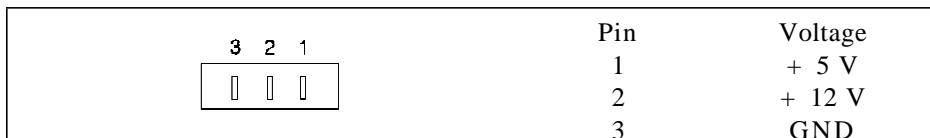


Figure 12. Alternate Power Connector Pin Assignments

4.2 Electrical interface specification

4.2.1.1 AT Signal Connector

The AT signal connector is a 40-pin connector. The pin assignments of interface signals are listed as follows:

PIN	SIGNAL	I/O	Type	PIN	SIGNAL	I/O	Type
01	-HRESET	I	TTL	02	GND		
03	HD07	I/O	3-state	04	HD08	I/O	3-state
05	HD06	I/O	3-state	06	HD09	I/O	3-state
07	HD05	I/O	3-state	08	HD10	I/O	3-state
09	HD04	I/O	3-state	10	HD11	I/O	3-state
11	HD03	I/O	3-state	12	HD12	I/O	3-state
13	HD02	I/O	3-state	14	HD13	I/O	3-state
15	HD01	I/O	3-state	16	HD14	I/O	3-state
17	HD00	I/O	3-state	18	HD15	I/O	3-state
19	GND			(20)	Key		
21	DMARQ	0	3-state	22	GND		
23	-HIOW	I	TTL	24	GND		
25	-HIOR	I	TTL	26	GND		
27	HIORDY	0	OC	28	CSEL	I	TTL
29	-DMACK	I	TTL	30	GND		
31	HIRQ	0	3-state	32	-HIOCS16	0	OC
33	HA01	I	TTL	34	-PDIAG	I/O	OC
35	HA00	I	TTL	36	HA02	I	TTL
37	-HCS0	I	TTL	38	-HCS1	I	TTL
39	-DASP	I/O	OC	40	GND		

Figure 13. Table of signals

Notes:

1. "O" designates an output from the Drive.
2. "I" designates an input to the Drive.
3. "I/O" designates an input/output common.
4. "OC" designates Open-Collector or Open-Drain output.

Signal	Description
HD00-HD15	16-bit bi-directional data bus between the host and the HDD. The lower 8 lines, HD00-07, are used for Register and ECC access. All 16 lines, HD00-15, are used for data transfer. These are 3-State lines with 24 mA current sink capability.
HA00-HA02	Address used to select the individual register in the HDD.
-HCS0	Chip select signal generated from the Host address bus. When active, one of the Command Block Registers (Data, Error{Features when written}, Sector Count, Sector Number, Cylinder Low, Cylinder High, Drive/Head and Status{Command when written} register) can be selected. (See Figure 18 on page 20.)
-HCS1	Chip select signal generated from the Host address bus. When active, one of the Control Block Registers (Alternate Status{Device Control when written} and Drive Address register) can be selected. (See Figure 18 on page 20.)
-HRESET	This line is used to reset the HDD. It shall be kept Low logic state during power up and kept High thereafter.
-HIOW	Its rising edge holds data from the host data bus to a register or data register of the HDD.
-HIOR	When low, this signal enables data from a register or data register of the drive onto data bus. The data on the bus shall be latched on the rising edge of -HIOR.

HIRQ	Interrupt is enabled only when the drive is selected, and the host activates the -IEN bit in the Device Control Reg. Otherwise, this signal is in high impedance state regardless of the state of the IRQ bit. The interrupt is set when the IRQ bit is set by the drive CPU. IRQ is reset to zero by a host read of the status register or a write to the Command Reg. This signal is a 3-State line with 24 mA sink capability.
-HIOCS16	Indication to the host that a 16-bit wide data register has been addressed and that the drive is prepared to send or receive a 16-bit wide data word. This signal is an Open-Drain output with 24 mA sink capability and an external resistor is needed to pull this line to 5 Volt.
-DASP	<p>This is a time-multiplexed signal which indicates that a drive is active, or that drive 1 is present. This signal is driven by Open-Drain driver and internally pulled-up to 5 Volt through a 10Kohm resistor.</p> <p>During Power-On initialization or after -HRESET is negated, -DASP shall be asserted by Drive 1 within 400 msec to indicate that drive 1 is present. Drive 0 shall allow up to 450msec for drive 1 to assert -DASP. If drive 1 is not present, drive 0 may assert -DASP to drive a LED indicator.</p> <p>-DASP shall be negated following acceptance of the first valid command by drive 1. Anytime after negation of -DASP, either drive may assert -DASP to indicate that a drive is active.</p>
-PDIAG	<p>This signal shall be asserted by drive 1 to indicate to drive 0 that it has completed diagnostics. This line is pulled-up to 5 Volt in the HDD through a 10Kohm resistor.</p> <p>Following a Power On Reset, software reset or -HRESET, drive 1 shall negate -PDIAG within 1 msec (to indicate to drive 0 that it is busy). Drive 1 shall then assert -PDIAG within 30 seconds to indicate that it is no longer busy, and is able to provide status.</p> <p>Following the receipt of a valid Execute Drive Diagnostics command, drive 1 shall negate -PDIAG within 1 msec to indicate to drive 0 that it is busy and has not yet passed its drive diagnostics. If drive 1 is present then drive 0 shall wait for up to 5 seconds from the receipt of a valid Execute Drive Diagnostics command for drive 1 to assert -PDIAG. Drive 1 should clear BSY before asserting -PDIAG, as -PDIAG is used to indicate that drive 1 has passed its diagnostics and is ready to post status.</p> <p>If -DASP was not asserted by drive 1 during reset initialization, drive 0 shall post its own status immediately after it completes diagnostics, and clear the drive 1 Status register to 00h. Drive 0 may be unable to accept commands until it has finished its reset procedure and is ready (DRDY=1).</p>
CSEL (Cable Select) (Optional)	<p>The drive is configured as either Drive 0 or 1 depending upon the value of CSEL.</p> <ul style="list-style-type: none"> • If CSEL is grounded then the drive address is 0. • If CSEL is open then the drive address is 1.
KEY	Pin position 20 has no connection pin. It is recommended to close the respective position of the cable connector in order to avoid incorrect insertion by mistake.
HIORDY	This signal is negated to extend the host transfer cycle when a drive is not ready to respond to a data transfer request, and may be negated when the host transfer cycle is less than TBD nsec for PIO data transfer. This signal is an open-drain output with 24 mA sink capability and an external resistor is needed to pull this line to 5 volts.
-DMACK	This signal shall be used by the host in response to DMARQ to either acknowledge that data has been accepted, or that data is available.
DMARQ	This signal, used for DMA data transfers between host and drive, shall be asserted by the drive when it is ready to transfer data to or from the host. The direction of data transfer is controlled by -HIOR and -HIOW. This signal is used on a handshake manner with -DMACK. This signal is a 3-state line with 24mA sink capability and internally pulled-down to GND through 10 KOhm resistor.

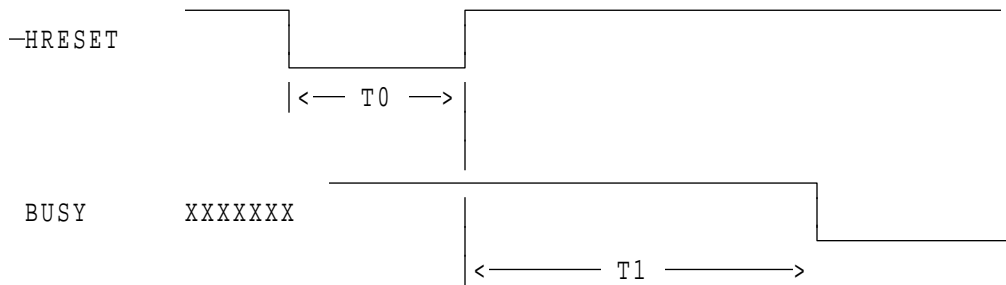
4.2.2 Interface Logic Signal Levels

The interface logic signal has the following electrical specifications:

Inputs :	Input High Voltage	—	2.0 V min.
	Input Low Voltage	—	0.8 V max.
Outputs :	Output High Voltage	—	2.4 V min.
	Output Low Voltage	—	0.5 V max.

4.2.3 Reset timing

HDD reset timing

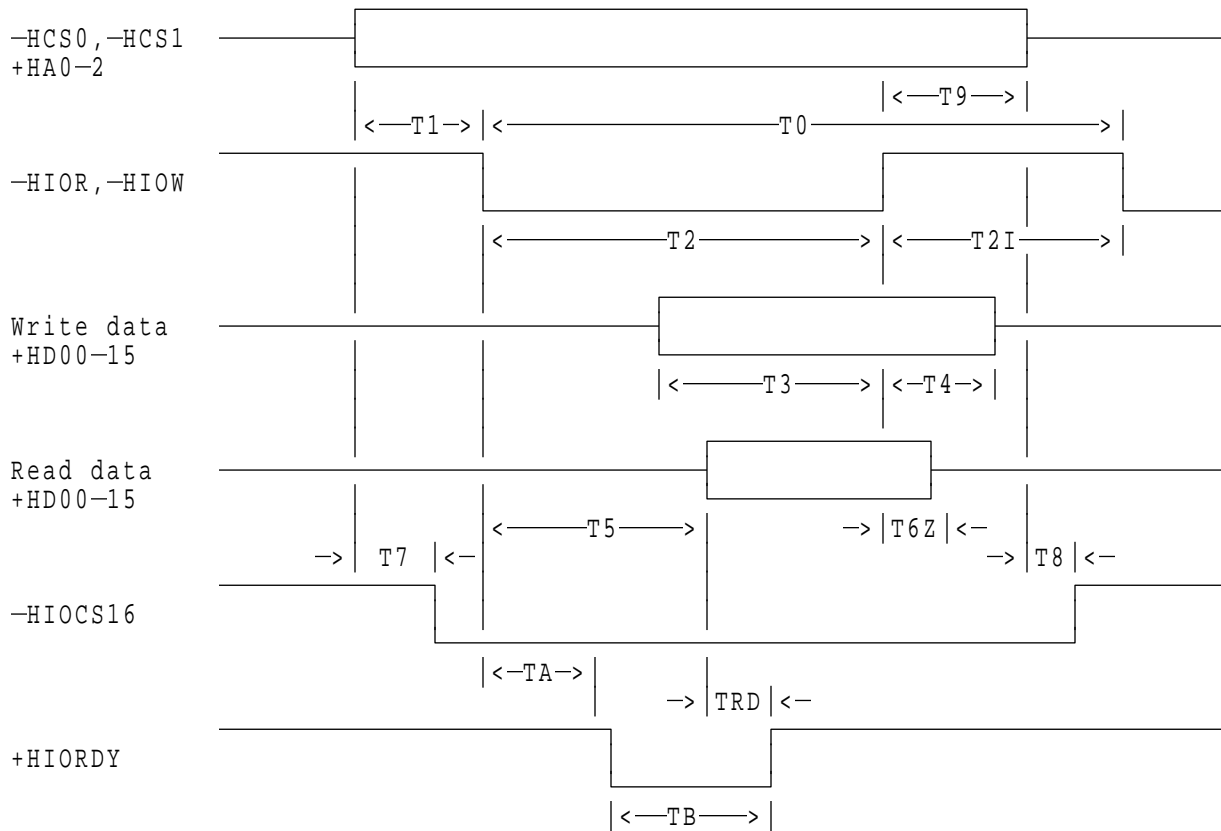


	PARAMETER DESCRIPTION	Min (μ sec)	Typ (sec)	Max (sec)
T0	-HRESET low width	25		
T1	-HRESET high to Not BUSY	—	6	18

Figure 14. System Reset timing

4.2.4 PIO timing

The PIO cycle timing meets Mode 3 of the ATA-2 description.



	PARAMETER DESCRIPTION	MIN (nsec)	MAX (nsec)	
T0	Cycle time	180	—	
T1	$\overline{\text{HCS0-1}}, \text{+HA00-02}$ valid to $\overline{\text{HIOR}}, \overline{\text{HIOW}}$ active	30	—	
T2	$\overline{\text{HIOR}}, \overline{\text{HIOW}}$ pulse width	80	—	
T2I	$\overline{\text{HIOR}}, \overline{\text{HIOW}}$ recovery	70	—	
T3	+HD00-15 setup to $\overline{\text{HIOW}}$ high	30	—	
T4	$\overline{\text{HIOW}}$ high to +HD00-15 hold	10	—	
T5	$\overline{\text{HIOR}}$ low to +HD00-15 valid	—	60	*1
T6	$\overline{\text{HIOR}}$ high to +HD00-15 hold	5	—	
T6Z	$\overline{\text{HIOR}}$ high to +HD00-15 tristate	—	30	
T7	$\overline{\text{HCS0-1}}, \text{+HA00-02}$ valid to $\overline{\text{HIOCS16}}$ assertion	—	30	
T8	$\overline{\text{HCS0-1}}, \text{+HA00-02}$ invalid to $\overline{\text{HIOCS16}}$ negation	—	30	
T9	$\overline{\text{HIOR}}, \overline{\text{HIOW}}$ high to $\overline{\text{HCS0-1}}, \text{+HA00-02}$ hold	10	—	
TRD	Read data valid to +HIORDY active	0	—	
TA	$\overline{\text{HIOR}}, \overline{\text{HIOW}}$ low to +HIORDY low	—	35	
TB	+HIORDY pulse width	—	1250	

Note *1 : This value is applied only when +HIORDY is not negated. When +HIORDY is negated, TRD is applied.

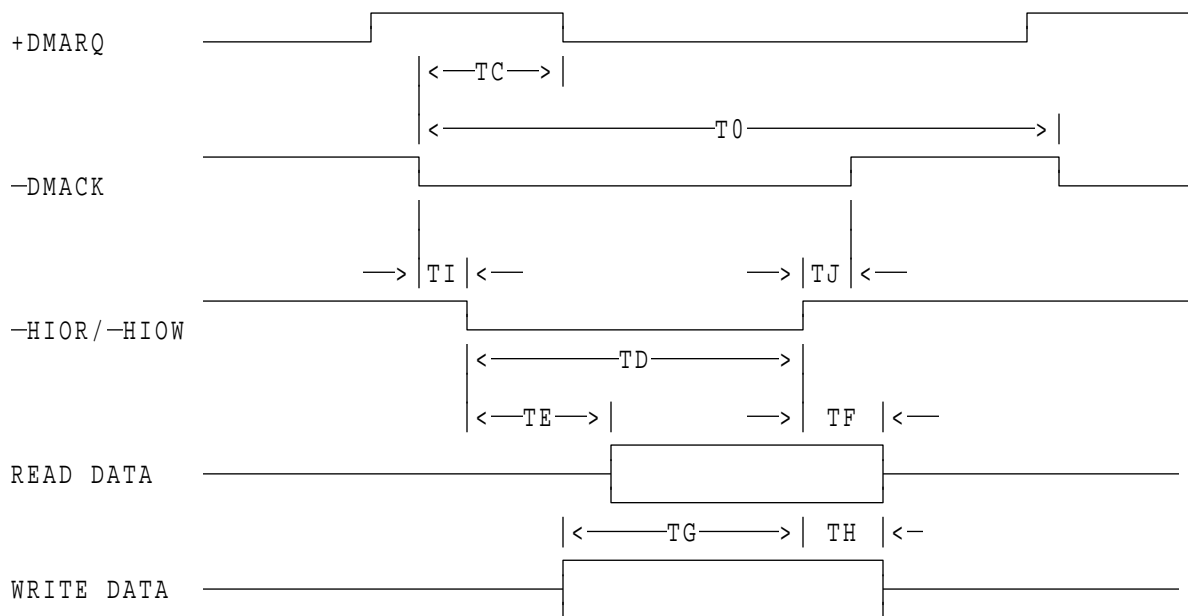
Figure 15. PIO cycle timing

4.2.4.1 Read DRQ Interval Time

For Read sectors and read multiple operations, the interval from the end of negation of DRQ bit until setting of next DRQ bit is not inserted except between the first and the second blocks in case that the status register is not read after the block data transfer. And in case that the status register is read after the block data transfer, the interval is inserted between all blocks. The interval is 15 μ sec.

4.2.5 DMA timing (Single Word)

The Single Word DMA timing meets Mode 2 of the ATA-2 description.

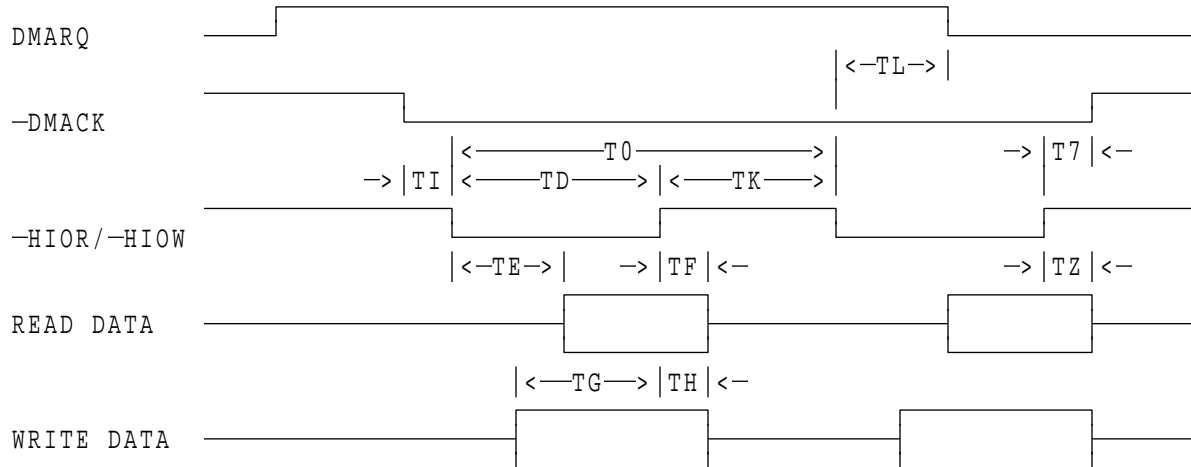


	PARAMETER DESCRIPTION	MIN (nsec)	MAX (nsec)	Note
T0	Cycle time	240	—	
TC	-DMA active to +DMARQ inactive	—	80	
TD	-HIOR, -HIOW pulse width	120	—	
TE	-HIOR data access	—	60	
TF	-HIOR data hold	5	—	
TG	-HIOW data setup	35	—	
TH	-HIOW data hold	20	—	
TI	-DMACK to -HIOR/-HIOW setup	0	—	
TJ	-HIOR/-HIOW to -DMACK hold	0	—	

Figure 16. DMA (Single Word) cycle timing

4.2.6 DMA timing (Multiword)

The Multiword DMA timing meets Mode 1 of the ATA-2 description.



	PARAMETER DESCRIPTION	MIN (nsec)	MAX (nsec)	Note
T0	Cycle time	180	—	
TD	-HIOR,-HIOW pulse width	80	—	
TE	-HIOR data access	—	60	
TF	-HIOR data hold	5	—	
TZ	-HIOR to tristate	—	25	
TG	-HIOW data setup	30	—	
TH	-HIOW data hold	15	—	
TI	-DMACK to -HIOR/-HIOW setup	0	—	
TJ	-HIOR/-HIOW to -DMACK hold	5	—	
TK	-HIOR/-HIOW negated pulse width	50	—	
TL	-HIOR/-HIOW to -DMARQ delay	—	40	

Figure 17. DMA (Multiword) cycle timing

4.2.7 Addressing of HDD Registers

The host addresses the drive through a set of registers called the Task File. These registers are mapped into the host's I/O space. Two chip select lines (-HCS0 and -HCS1) and three address lines (HA00-02) are used to select one of these registers, while a -HIOR or -HIOW is provided at the specified time.

The -HCS0 is used to address Command Block registers, while the -HCS1 is used to address Control Block registers.

The following table shows the I/O address map.

Addr.	-HCS0	-HCS1	HA02	HA01	HA00	-HIOR = 0 (Read)	-HIOW = 0 (Write)
Command Block Registers							
1F0	0	1	0	0	0	Data Reg.	Data Reg.
1F1	0	1	0	0	1	Error Reg.	Features Reg.
1F2	0	1	0	1	0	Sector count Reg.	Sector count Reg.
1F3	0	1	0	1	1	Sector number Reg.	Sector number Reg.
1F4	0	1	1	0	0	Cylinder low Reg.	Cylinder low Reg.
1F5	0	1	1	0	1	Cylinder high Reg.	Cylinder high Reg.
1F6	0	1	1	1	0	Drive/Head Reg.	Drive/Head Reg.
1F7	0	1	1	1	1	Status Reg.	Command Reg.
Control Block Registers							
3F6	1	0	1	1	0	Alt. Status Reg.	Device control Reg.
3F7	1	0	1	1	1	Drive address Reg.	—

Figure 18. Task File

Note: "Addr." field is shown just as an example.

During DMA operation (from writing to the command register until an interrupt), all registers are not accessible.

For example, the host is not supposed to read status register contents before interrupt (the value is invalid).

4.2.8 Cabling

The maximum cable length from the host system to the HDD plus circuit pattern length in the host system shall not exceed 18 inches (45.7 cm).

4.2.9 Jumper Settings

Seven positions for jumpers shown below are used to select Master/Slave, Cable Selection, Write Cache, Auto Reallocation and a capacity of 541/528 MB.

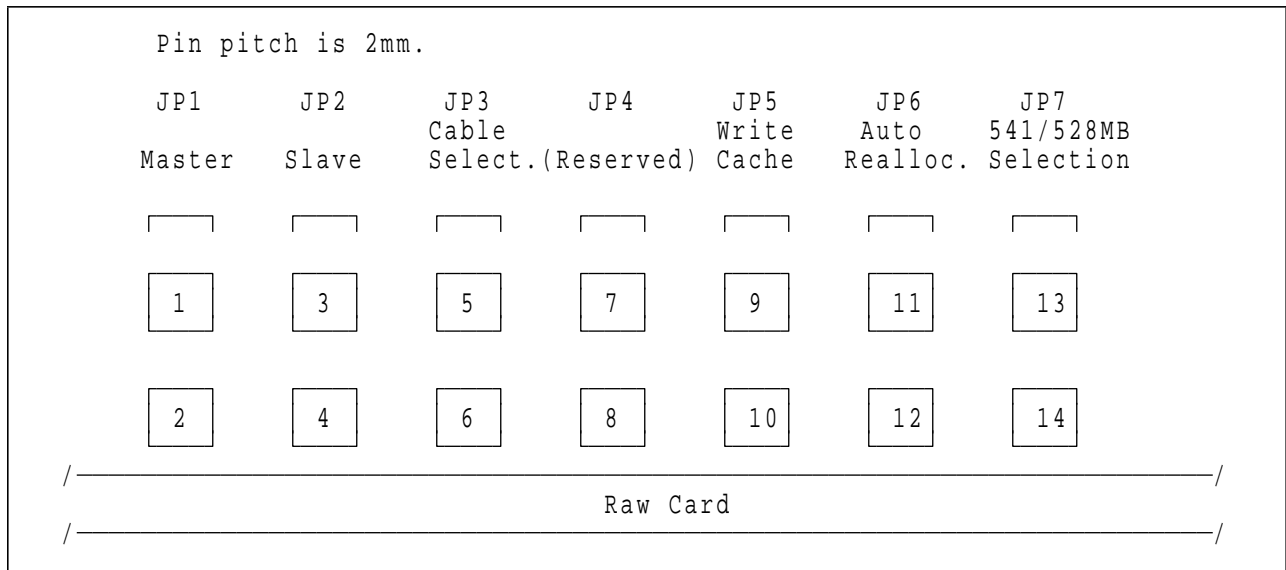


Figure 19. Jumper Pins

Notes:

1. The jumper position of JP1, 2, and 3 should not be selected concurrently.
2. JP1 is the position for Master, JP2 is for Slave, and JP3 is for Cable Selection mode.
3. To enable the CSEL mode (cable selection mode), the JP3 jumper must be installed. In the CSEL mode, the drive address is determined as follows:
 - When CSEL is grounded or at a low level, the drive address is 0 (Master)
 - When CSEL is open or at a high level, the drive address is 1 (Slave).
4. When JP5 jumper is installed, write cache function is disabled.
5. When JP6 jumper is installed, auto reallocation and write cache functions are disabled.
6. When JP7 jumper is installed, the capacity is set to 541MB. Otherwise, the capacity is set to 528MB.

4.2.9.1 The pin assignment

JP#	Pin Number	Description
1	1	GND
	2	-Device Address Select Line
2	3	NC (Slave position)
	4	NC
3	5	Cable Selection (28 PIN)
	6	-Device Address Select Line
4	7	GND
	8	(Reserved)
5	9	GND
	10	+Write Cache ON (If open)
6	11	GND
	12	+Auto Reallocation ON (If open)
7	13	GND
	14	-540 MB (If short)

Figure 20. Jumper Pins Assignment

4.2.9.2 Shipping default condition

The default shipping condition is device ID is Master, write cache on, auto reallocation on.

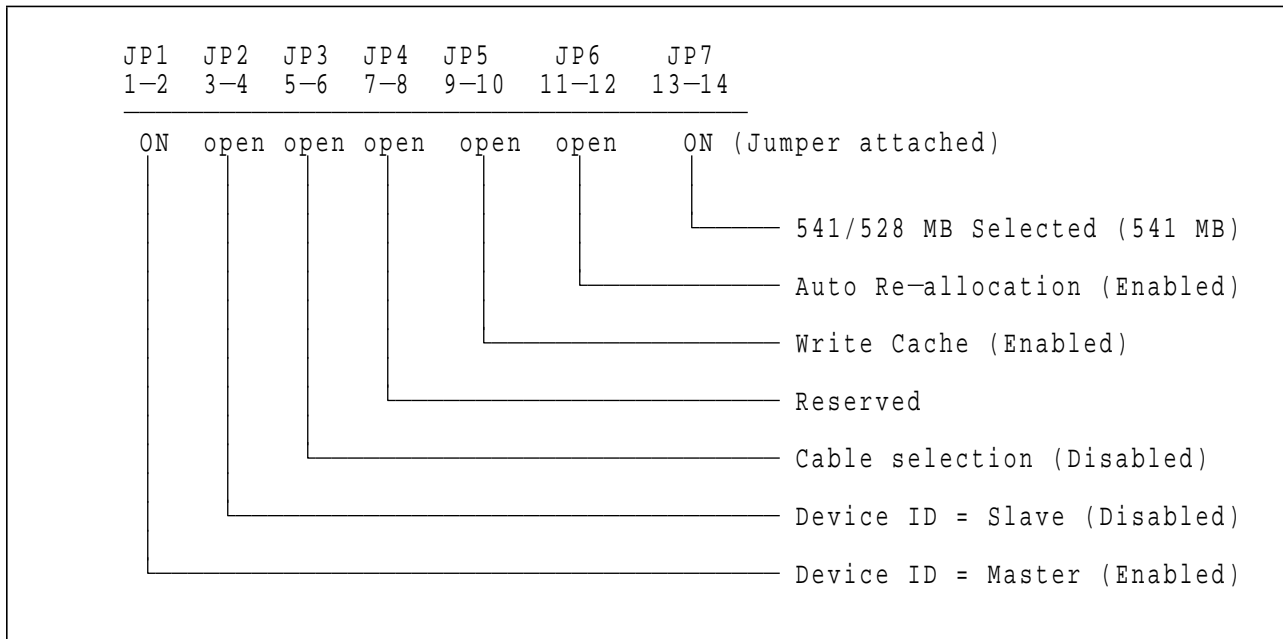


Figure 21. AT Jumper Default Condition

4.2.9.3 Mechanical Outline

The card with disk enclosure mechanical outline is as follows.

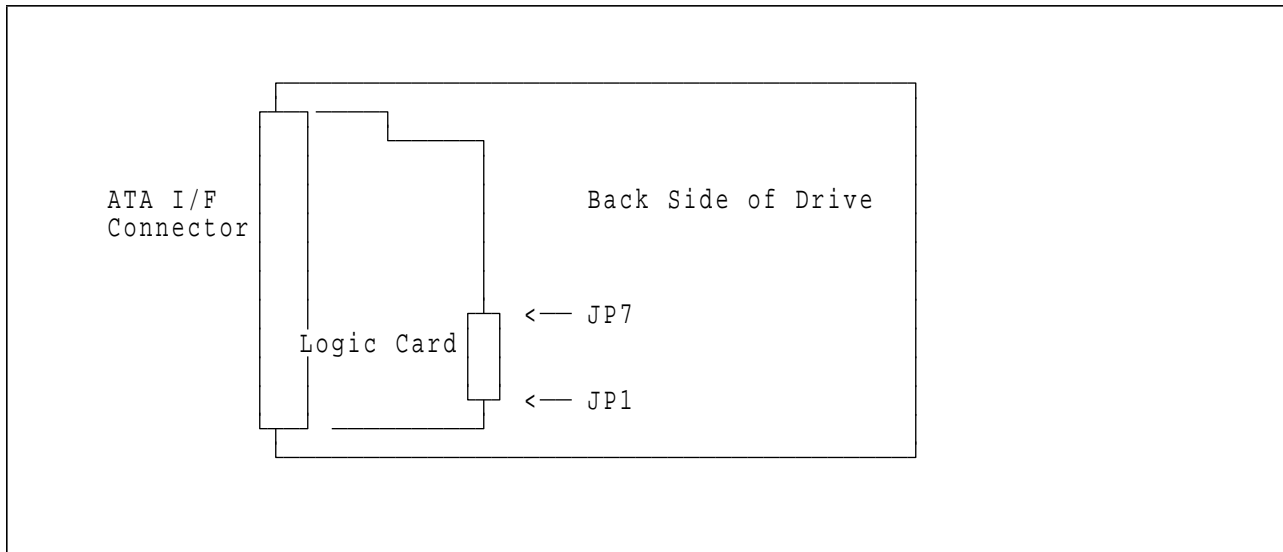


Figure 22. Mechanical Outline

4.3 Environment

4.3.1 Temperature and Humidity

Operating Conditions	
Temperature Relative Humidity Maximum Wet Bulb Temperature Maximum Temperature Gradient Altitude	5 to 55°C (*1) 8 to 90 % non-condensing 29.4°C non-condensing 15°C / Hour -300 to 3 000 m
Shipping Conditions	
Temperature Relative Humidity Maximum Wet Bulb Temperature Altitude	-40 to 65°C 5 to 95 % non-condensing 35°C non-condensing -300 to 12 000 m
Storage Conditions	
Temperature Relative Humidity Maximum Wet Bulb Temperature Altitude	0 to 65°C 5 to 95 % non-condensing 35°C non-condensing -300 to 12 000 m
Note *1: Systems are responsible to provide sufficient air movement to maintain surface temperature below 60°C at the center of top cover of the drive.	

4.4 DC Power Requirements

The following voltage specification apply at the power connector of the drive. Damage to the electronics of the drive may result if the power supply cable is connected or disconnected while power is being applied to the drive (No hot plug/unplug is allowed). There is no special power on/off sequencing required.

Input Voltage

	During run and spin up	Absolute max voltage
+5 Volts Supply	5V ±5%	7V
+12 Volts Supply	12V +10%, -8%	15V

Power Supply Current

(All values in Amps.)	+5 Volts		+12 Volts		Total (W)
	Pop Mean	Std.Dev	Pop Mean	Std.Dev	
Idle average	0.18	0.02	0.14	0.02	2.6
Idle ripple (peak-to-peak)	0.21	0.02	0.11	0.02	
Seek peak (*1)	0.50	0.03	0.52	0.03	
Seek average (*1)	0.41	0.02	0.27	0.02	5.2
Start up(max)	0.51	0.02	1.16	0.03	
RND R/W peak (*2)	0.59	0.03	0.50	0.03	
RND R/W average (*2)	0.49	0.03	0.17	0.02	4.5
Standby/Sleep average	0.11	0.01	0.02	0.01	0.8

(*1 : Random Seeks at 100% duty cycle.)
 (*2 : Seek Duty = 30%, W/R Duty = 45%, Idle Duty = 25%.)

	Maximum	Notes
+5 V DC	100 mV pp	0-10 MHz
+12 V DC	150 mV pp	0-10 MHz

During start up and seeking, 12 volt ripple is generated by the drive (referred to as dynamic loading). If more than two drives have their power daisy chained together then the power supply ripple plus other dynamic loading of the drive must remain within the regulation tolerance of +10/-8%. A common supply with separate power leads to each drive is a more desirable method of power distribution.

To prevent external electrical noise from interfering with the performance, the drive must be attached by using four screws in a user system frame which has no electrical level difference at the four screws position, and has less than +/-300 millivolts peak to peak level difference to the power connector ground of the drive.

4.5 Reliability

4.5.1 Data Integrity

No more than one sector is lost at Hard Reset or Power loss condition during write operation when the write cache option is disabled. If write cache option is active, the data in write cache will be lost. To prevent customer data lost, the last write access before power off is recommended to be issued after setting write cache off.

4.5.2 Cable Noise Interference

To avoid any degradation of performance throughput or error rate when the interface cable is routed on top or comes in contact with the HDA assembly, the drive must be grounded electrically to the system frame by the typical four screws. The common mode noise or voltage level difference between the system frame and power cable ground or ATA interface cable ground should be in the allowable level specified in the power requirement section.

4.5.3 MTBF

350,000 power-on hours (POH) under the following conditions:

- 4,000 POH per year (333 POH per month)
- Seeking/writing/reading operation to be 20% of POH at 40°C or lower environmental temperature.

4.5.4 Contact Start Stop (CSS)

The drive withstands a minimum of 40 000 contact start/stop cycles at 40°C.

4.5.5 Useful Life

The useful life of the drives is 5 years minimum.

4.5.6 Preventive Maintenance

None.

4.5.7 Data Reliability

- Probability of not recovering data 1 in 10E13 bits read
- ECC implementation

A Read Solomon Error Correcting Code of degree 8 with non-interleaved is used to cover the data fields. The ECC polynomial is derived from:

$$g(X) = (X + 1)(X + A)(X + A^{**2}) \text{ --- } (X + A^{**7})$$

ECC On The Fly implemented in the drive covers four or less symbols of error in one sector. (1 Symbol = 10 Bits)

4.6 Mechanical Specifications

4.6.1 Physical Dimensions

The following chart describes the dimensions and the weight of the drive. (see figures in Appendix)

Dimension	Value (mm)
Height	25.4 ± 0.4
Width	101.6 ± 0.4
Length	146.0 ± 0.6
Weight	450 gram Max.

4.6.2 Mounting Holes

The mounting hole location and size for the drive is shown below. For the details, see figures in Appendix.

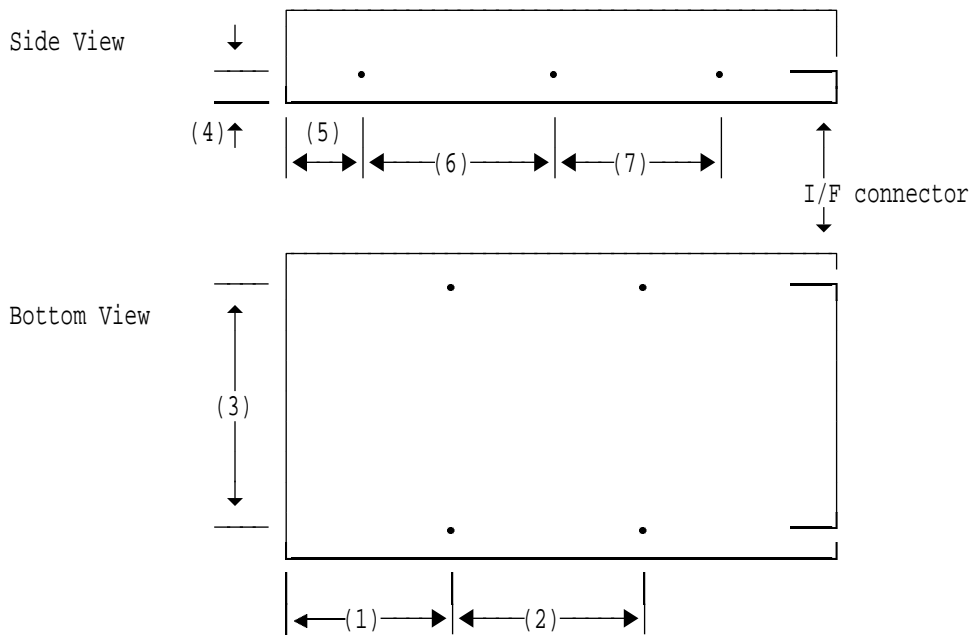


Figure 23. Hole Locations							
Thread	(1)	(2)	(3)	(4)	(5)	(6)	(7)
6-32 UNC	60.3±0.2	44.45±0.1	95.25±0.1	6.35±0.2	16.0±0.2	60.0±0.1	41.6±0.1

Recommended screw torque to be applied to mounting screws is 0.6 - 1.0 Nm (6 - 10 kg*cm). Refer Appendix for screw length.

4.6.3 Connector and Jumper Description

Refer to the figures in Appendix for location of the interface connector and the jumpers.

4.6.4 Drive Mounting

The drive will operate in all axes (6 directions). Performance and error rate will stay within specification limits if the drive is operated in the other orientations from which it was formatted.

For reliable operation, it is recommended to mount the drive in a system securely enough to prevent from excessive motion or vibration of the drive at seek operation or disk rotation by using appropriate screws or equivalent mounting instruments.

Drive level vibration test and shock test are to be conducted with the drive attached to the table by using four screws on the bottom.

4.6.5 Shipping Zone and Lock

A dedicated "shipping" (or "landing") zone on the disk, not on the data area of the disk, is provided to protect the disk data during shipping, movement, or storage. Upon power down, the heads are automatically parked and a head locking mechanism will secure the heads in this zone.

4.7 Vibration and Shock

All vibration and shock measurements in this section shall be for the drive without the mounting attachments for the systems. The input level shall be applied to the normal drive mounting points.

4.7.1 Operating Vibration

4.7.1.1 Random Vibration

The test is 30 minutes of random vibration using the power spectral density (PSD) levels shown below in each of three mutually perpendicular axes. The drive will operate without non-recoverable errors when subjected to the above random vibration levels.

Figure 24. Random vibration PSD profile breakpoints (Operating)									
5	17	45	48	62	65	150	200	500	Hz
0.02	1.1	1.1	8.0	8.0	1.0	1.0	0.5	0.5	$\times 10^{-3} \text{ G}^2/\text{Hz}$
Note: Overall RMS (root mean square) level of vibration is 0.67 G rms.									

4.7.1.2 Swept Sine Vibration

The drive will meet the criteria shown below while operating in respective conditions.

No errors 0.5 G 0-peak, 5-300-5 Hz sine wave, 0.5 oct/min sweep rate
with 3 minutes dwells at 2 major resonances

No data loss 1 G 0-peak, 5-300-5 Hz sine wave, 0.5 oct/min sweep rate
with 3 minutes dwells at 2 major resonances

4.7.2 Non-Operating Vibration

The drive does not sustain permanent hardware damage or loss of previously recorded data after being subjected to the environment described below.

4.7.2.1 Random Vibration

The test consists of a random vibration applied to each of three mutually perpendicular axes with the time duration of 10 minutes. The PSD levels for the test simulating the shipping and relocation environment is shown below.

Figure 25. Random vibration PSD profile breakpoints (Non-operating)							
2	4	8	40	55	70	200	Hz
0.001	0.03	0.03	0.003	0.01	0.01	0.001	G^2/Hz
Note: Overall RMS (root mean square) level of vibration is 1.04 G rms.							

4.7.2.2 Swept Sine Vibration

- 2 G 0-peak, 5-500-5 Hz sine wave
- 0.5 oct/min sweep rate
- 3 minutes dwells at 2 major resonances

4.7.3 Operating shock

The drive meets the following criteria while operating in respective conditions described below. The shock test consists of ten shocks inputs in each axis and direction for total of 60. There must be a delay between shock pulses, long enough to allow the drive to complete all necessary error recovery procedure.

No errors 5 G, 11 ms half-sine shock pulse

No data loss, seek errors or permanent damage
10 G, 11 ms half-sine shock pulse

No data loss or permanent damage
15 G, 5 ms half-sine shock pulse
30 G, 4 ms half-sine shock pulse

4.7.4 Non-operating shock

The drive will operate with no degradation of performance or permanent damage after subjected to shock pulses with the following characteristics.

4.7.4.1 Trapezoidal shock wave

- Approximate square (trapezoidal) pulse shape.
- Approximate rise and fall time of pulse = 1 ms.
- Averaged acceleration level = 50 G.
(Averaged response curve value during the time following the 1 ms rise time and before the 1 ms fall with a time "duration of 11 msec")
- Minimum velocity change = 4.23 meters/sec

4.7.4.2 Sinusoidal shock wave

- Approximate half-sine pulse shape.
- Maximum acceleration level = 75 G
- Shock duration = 11 msec

All shock input shall be applied in each direction of the drive's three mutually perpendicular axes. The heads are not displaced from the landing zone as a result of this test.

4.8 Acoustics

4.8.1 Sound Power

4.8.1.1 Unit Sound Power Level Testing

Sound power emission levels are measured according to ISO 7779. The upper limit criteria of the octave sound power levels are given in Bels relative to 1 pico Watt and are shown in the following table.

Figure 26. Octave band sound power levels								
	Octave Band Center Frequency (Hz)							
Mode	125	250	500	1k	2k	4k	8k	LwAu
Idle	4.8	4.1	3.6	3.6	3.9	3.9	3.6	4.5
Operating	5.0	4.3	4.2	4.2	4.2	4.2	3.8	4.8

Mode definition

Idle mode Power on, disks spinning, track following, unit ready to receive and respond to interface command.

Operating mode

Continuous random cylinder selection and seek operation of the actuator with a delay for a time period achieving the required seek rate N_s according to the following formula:

$$N_s = 0.4 / (T_t + T_l)$$

where:

N_s = average seek rate in seeks/sec.

T_t = published random seek time.

T_l = time for the drive to rotate by half a revolution.

4.8.1.2 Sound Power Acceptance Criteria

Statistical upper limit $(L_{W_{oct}})_{stat}$ is calculated with the following formula.

$$(L_{W_{oct}})_{stat} = (L_{W_{oct}})_m + k \times (s_t)_{W_{oct}}$$

where:

$(L_{W_{oct}})_m$ is the mean value of the sound power level for samples of N drives.

$(s_t)_{W_{oct}}$ is the total standard deviation for sound power level at each octave band.

$$(s_t)_{W_{oct}} = \text{SQRT}((s_R)_W^2 + (s_P)_{W_{oct}}^2)$$

$(s_R)_W$ is the standard deviation of reproducibility for sound power level.

Assume $(s_R)_W = 0.075$ B.

$(s_P)_{W_{oct}}$ is the standard deviation of the samples for sound power level at each octave band.

k is a coefficient determined by number of samples (N) as shown below.

N	5	6	7	8	9	10	11	12	13	14	15
k	2.74	2.49	2.33	2.22	2.13	2.07	2.01	1.97	1.93	1.90	1.87

4.9 Identification

4.9.1 Labels

The following labels are affixed to the drive shipped from the drive manufacturing location in accordance with appropriate assembly drawings of the drive.

- A label containing IBM logo, IBM part number and the statement "Made by IBM Japan Ltd.", or equivalent.
- A label containing drive model number, date code, formatted capacity, place of manufacture, and UL/CSA/TUV logos.
- A bar code label containing the drive serial number.
- An user designed label per agreement.

The labels may be integrated with the other labels.

4.10 Safety

4.10.1 Underwriters Lab (UL) Approval

The product is recognized for use in Information Processing and Business Equipment according to UL 1950. The UL Recognition will be maintained for the life of the product. Vendor/manufacturer marking for UL approval appears on the drive.

4.10.2 Canadian Standards Authority (CSA) Approval

The product is certified for use in Information Processing and Business Equipment according to the following CSA standards.

- C22.2 No.0-M1989
- C22.2 No.0.4-M1982
- C22.2 No.950-M1989

The CSA Certification will be maintained for the life of the product. Vendor/manufacturer marking for the CSA certification appears on the drive.

4.10.3 IEC Compliance

The product is certified for compliance to IEC 380, IEC 435, and IEC 950. The product will comply with these IEC requirements for the life of the product.

4.10.4 German Safety mark

All DALA-3540 is approved by TUV on Test requirement: EN 60 950:1988/A1:1990/A2:1991.

4.10.5 Flammability

Printed Circuit boards used in this product is made of material with a UL recognized flammability rating of V-1 or better. The flammability rating is marked or etched on the board. All other parts not considered electrical components are made of material with a UL recognized flammability rating of V-1 or better.

4.10.6 Environment

The product does not contain any known or suspected carcinogens.

Environmental controls meet or exceed all applicable government regulations in the country of origin. Safe chemical usage and manufacturing control are used to protect the environment. An environmental impact assessment has been done on the manufacturing process used to build the drive, the drive itself and the disposal of the drive at the end of its life.

Production also meets the requirements of the international treaty on chlorofluorocarbon (CFC) control known as the United Nations Environment Program Montreal Protocol, and as ratified by the member nations. Material to be controlled include CFC-11, CFC-12, CFC-113, CFC-114, CFC-115, Halon 1211, Halon 1301 and Halon 2402. Although not specified by the Protocol, CFC-112 is also controlled. In addition to the Protocol IBM requires the following:

- All packaging used for the shipment of the product do not use controlled CFCs in the manufacturing process.
- All manufacturing processes for parts or assemblies include printed circuit boards, does not use controlled CFC materials.

4.11 Electromagnetic Compatibility

When installed in the host system and exercised with a random accessing routine at maximum data rate, the drive meets the following worldwide EMC requirements:

- United States Federal Communications Commission (FCC) Rules and Regulations (Class B), Part 15.
- European Economic Community (EEC) directive number 76/889 related to the control of radio frequency interference and the Verband Deutscher Elektrotechniker (VDE) requirements of Germany (GOP).
- Electrostatic Discharge Susceptibility limits for a Class 2 ESD environment.

5.0 Mechanical Drawings

5.1 Isometric View

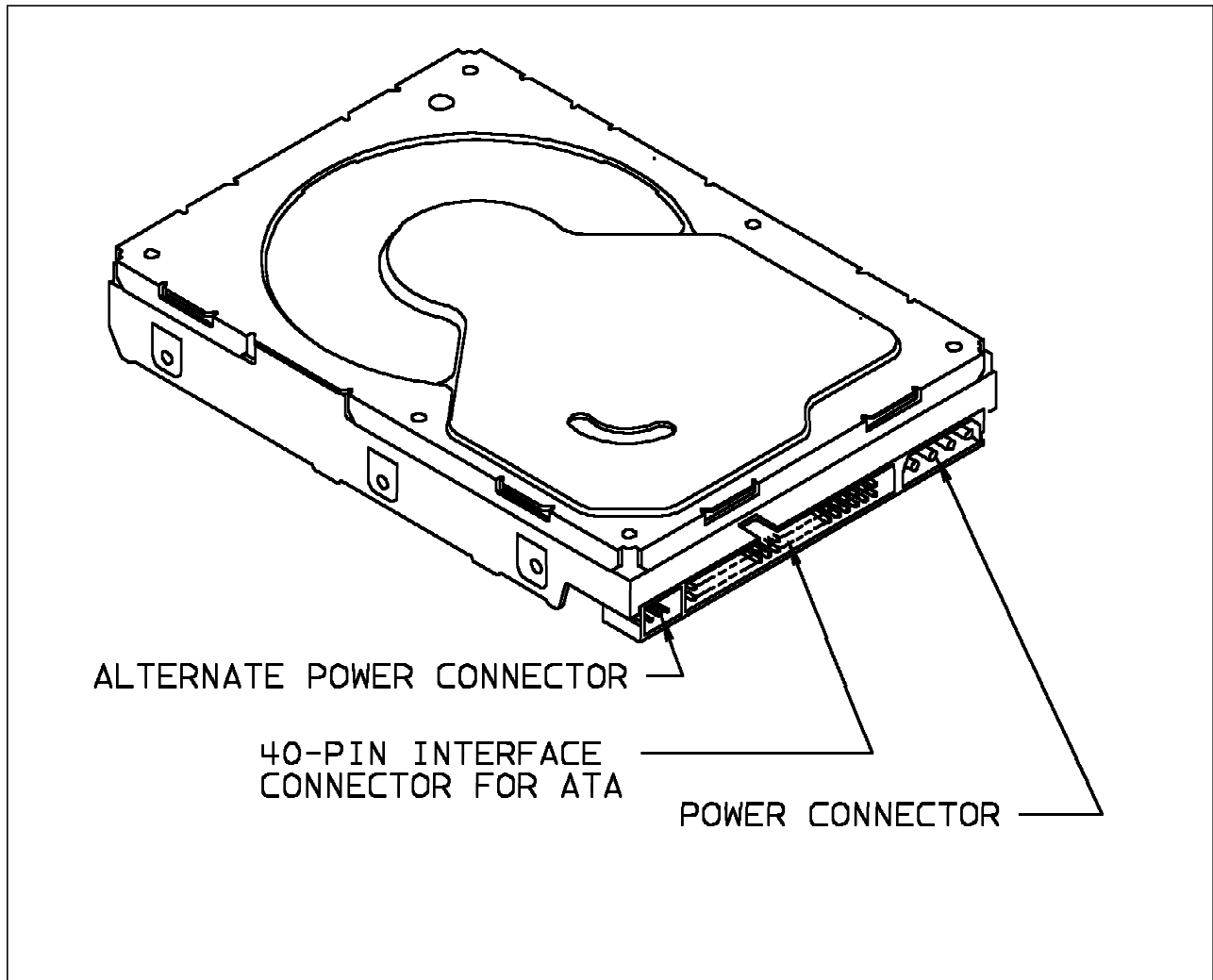


Figure 27. Isometric View of DALA-3540

5.2 Outline Dimensions

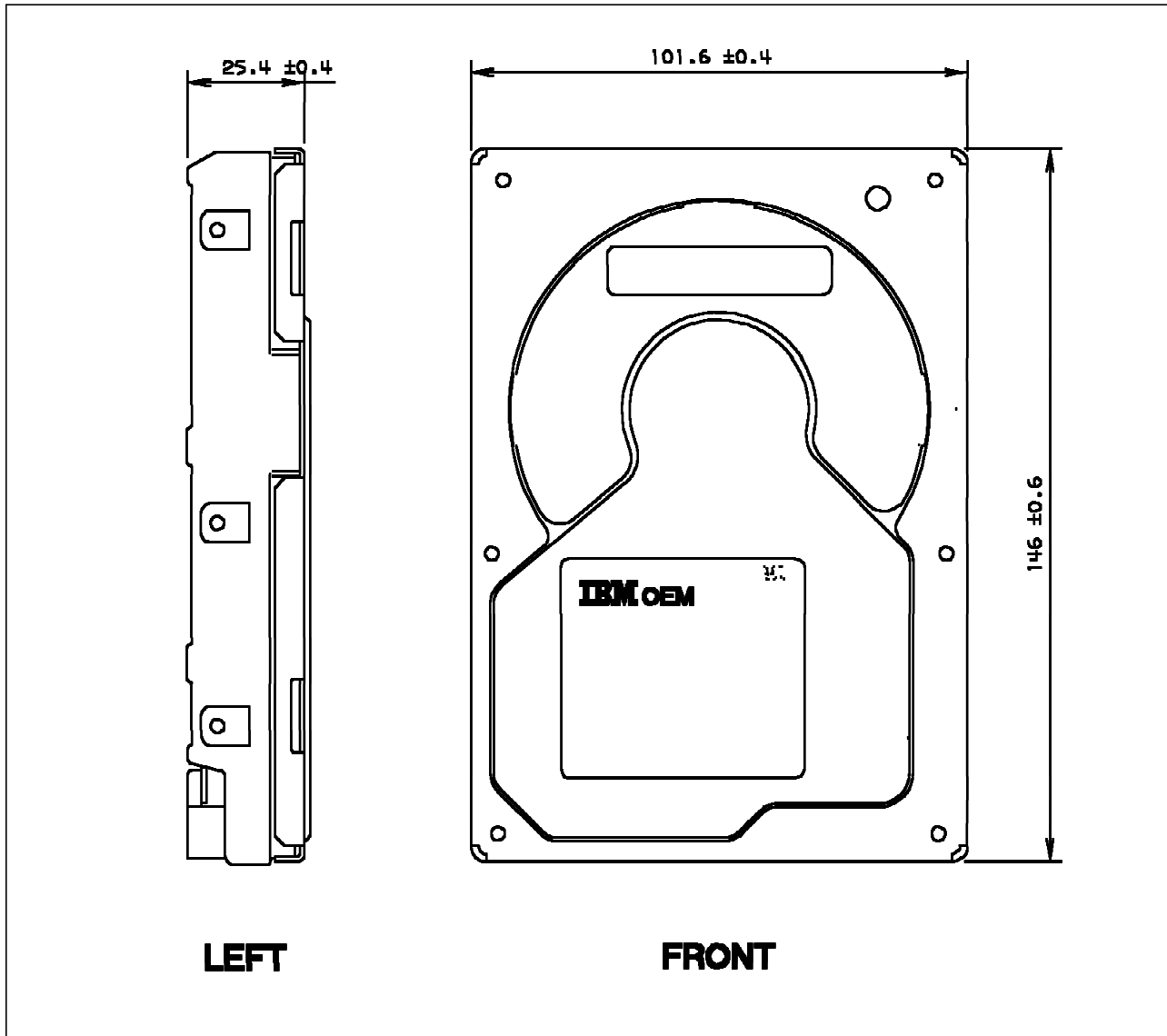


Figure 28. Outline Dimensions of DALA-3540

5.3 Mounting Holes

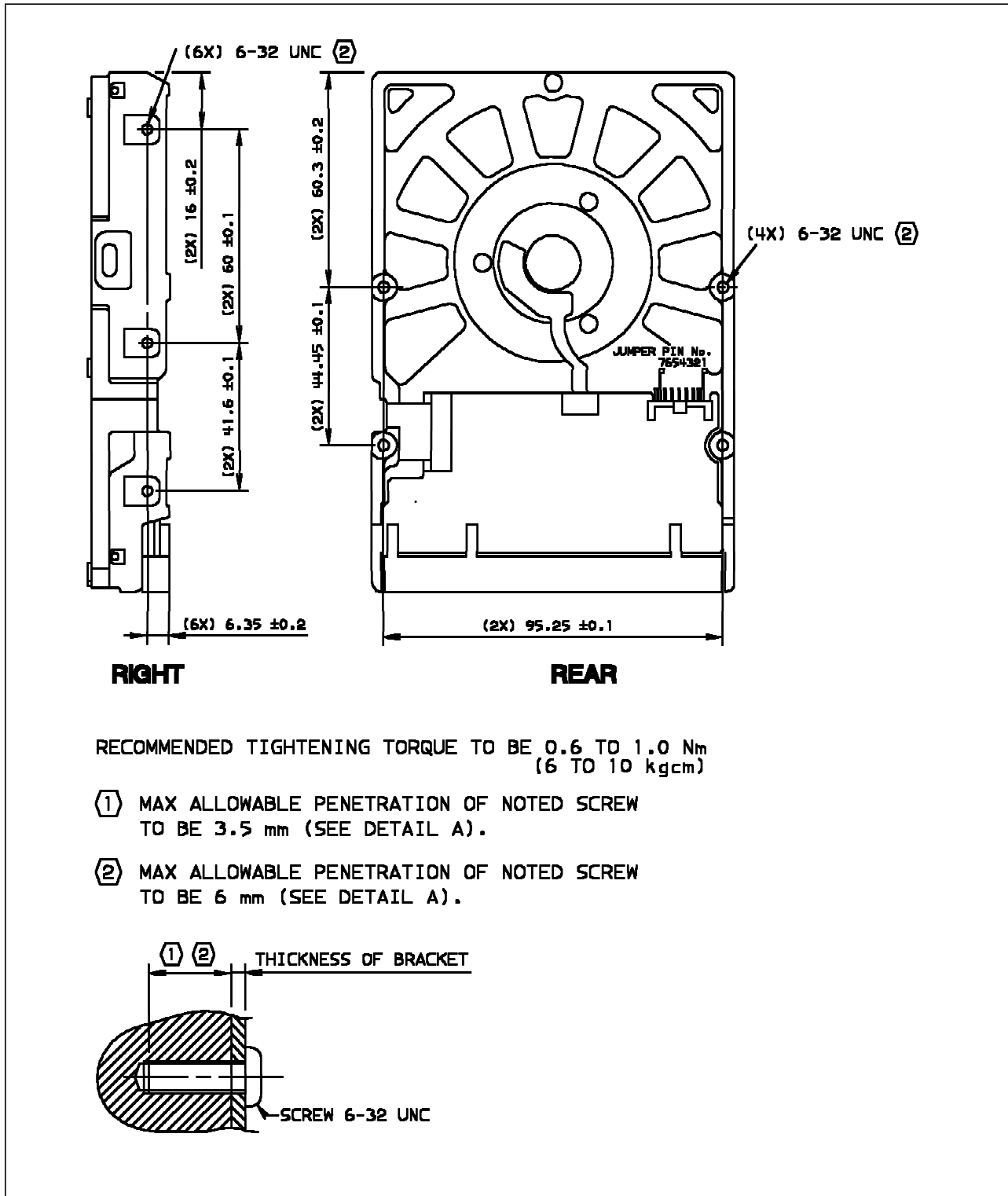


Figure 29. Mounting Holes of DALA-3540

5.4 Interface Connector

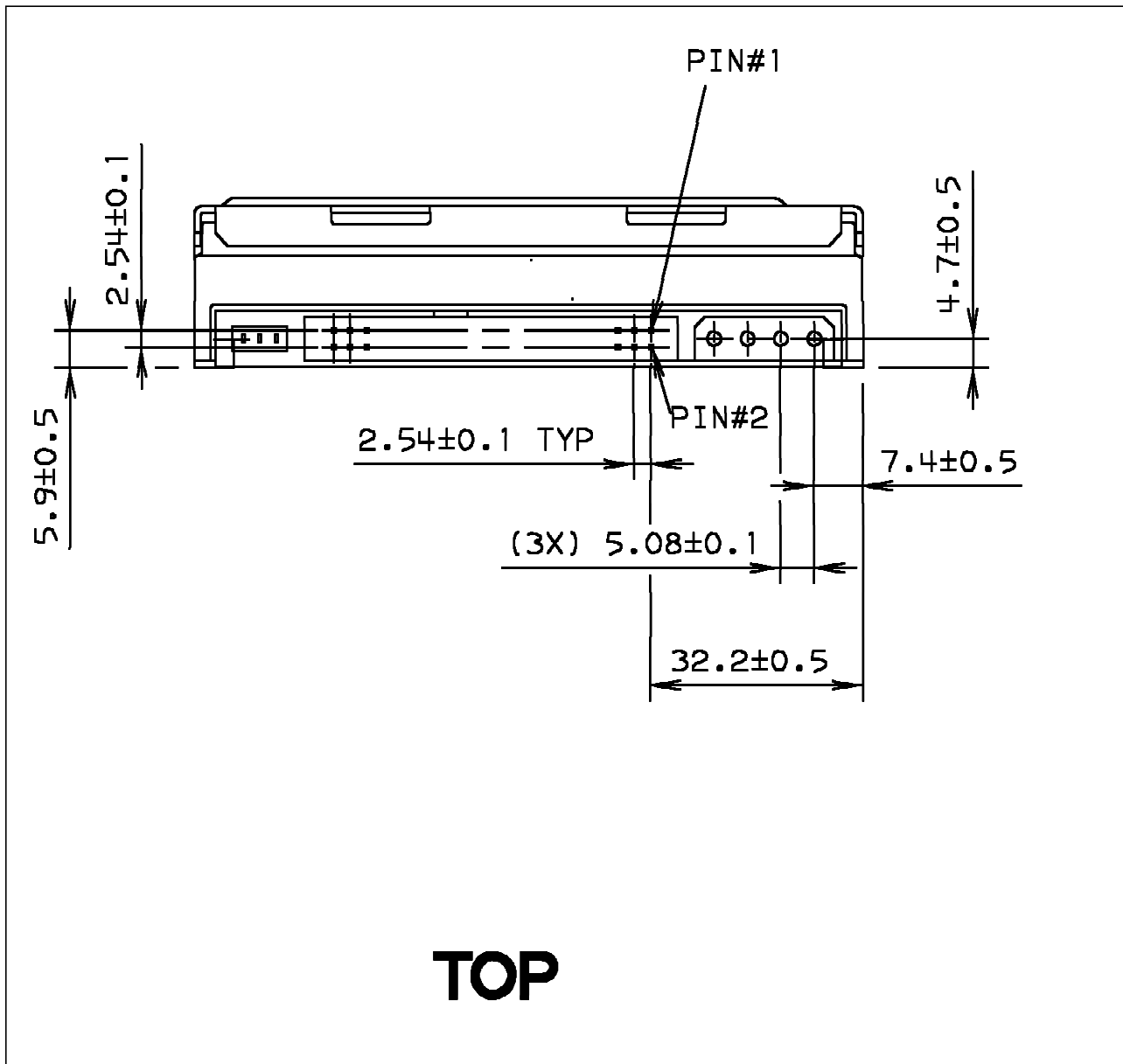


Figure 30. Interface Connector of DALA-3540

6.0 Interface

The interface conforms to the Working Draft of Information technology ATA Attachment Interface with Extensions (ATA-2) dated on July-6-1994. with certain limitations shown below.

Automatic Power Down Sequence A hard reset will disable the automatic power down sequence.

Format Track A drive will not perform a physical format. Instead it will simply write a data pattern of all zeros to the sectors which have been specified by the Format Track command. Bad sector flag which has been set by format track command will be cleared by write command.(ie. write sectors, write multiple, write DMA, write long)

Format Track Interleave Factor The drive only supports an interleave factor of 1:1, and may ignore the sector number in format table without returning an error.

Write long Write long command should be executed for the same sector after Read long command execution. Otherwise, unexpected ECC correctable error may occur. Because of the limitation of the emulation technique to support 4-byte ECC mode which is implemented in the drive.

Seek Overlap The drive will wait for the seek to complete before interrupting the host. Therefore, no seek overlap can occur. This will be transparent to the host except that performance may be degraded in certain environments where the host could perform other work while waiting for seek complete, such as multitasking operating systems.

Sleep Mode During Sleep mode the drive will be activated by any command, including, but not limited to, a soft reset.

Drive/Head Register Bits 5 and 7 of Drive/Head Register are not written to 0. (These 2 bits are always read as '1' even after host writes to '0'.)

Auto Reallocation Jumper See Figure 31 on page 40 for relation with write cache. (+)Auto reallocation jumper is checked during the initial power on reset (POR) check. Write cache becomes off when a jumper for these pins is set automatically to keep data integrity. (+)Auto reallocation jumper position needs to be OPEN when a user system wants to use write cache.

Write Cache Jumper See Figure 31 on page 40 for relation among (+)auto reallocation jumper and set features command for write cache. (+)Write cache jumper is checked during the initial POR check.

Sleep/Standby/Idle mode When entering sleep, standby or Idle mode as a result of a command the busy bit in the status register will remain set until the transition to the new state is complete.

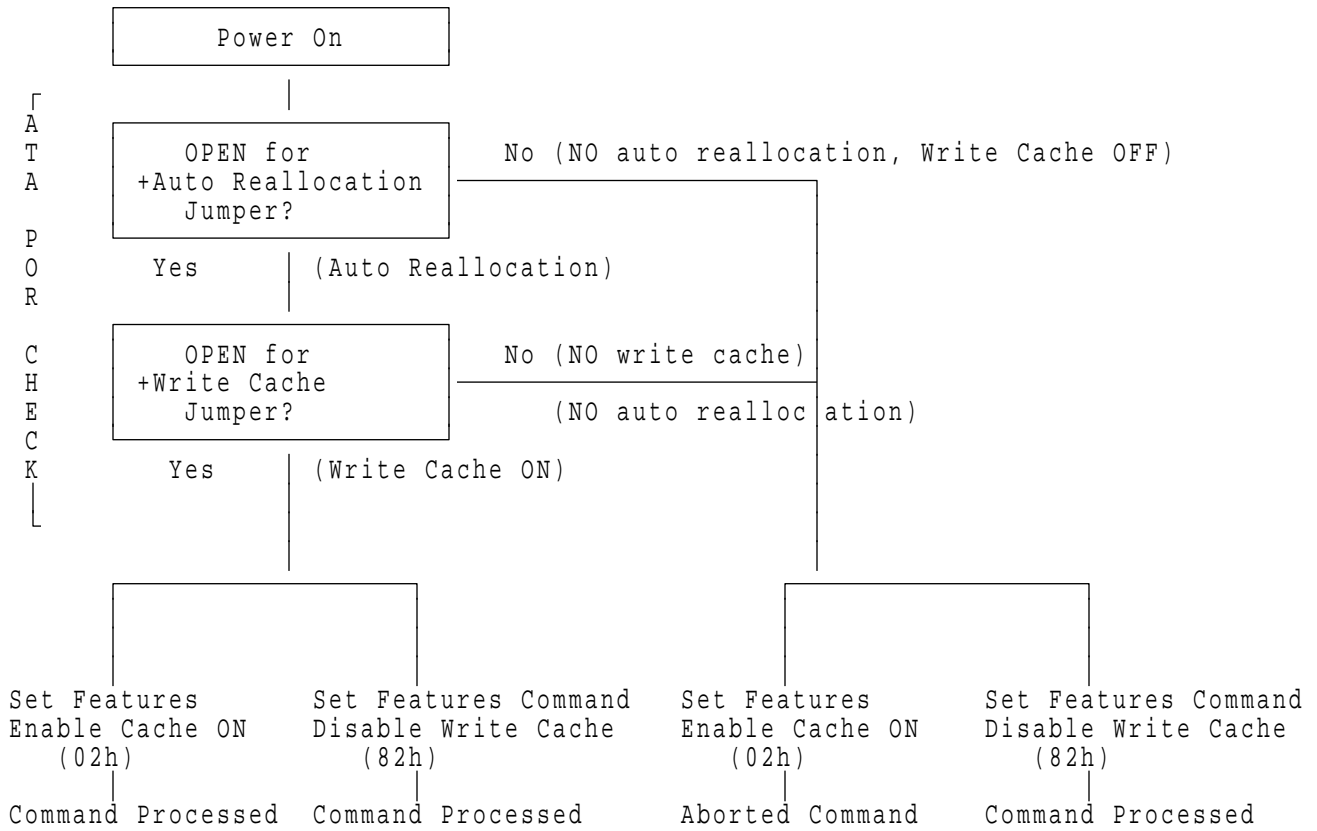


Figure 31. Relations Among Write Cache/Auto Reallocation Jumpers And Write Cache

7.0 Registers

7.1 Alternate Status Register

Alternate Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR

Figure 32. Alternate Status Register

This register contains the same information as the Status Register. The only difference is that reading this register does not imply interrupt acknowledge or clear a pending interrupt. See 7.13, “Status Register” on page 44 for the definition of the bits in this register.

7.2 Command Register

This register contains the command code being sent to the drive. Command execution begins immediately after this register is written. The command set is shown in Figure 41 on page 55.

All other registers required for the command must be set up before writing the Command Register.

7.3 Cylinder High Register

This register contains the high order bits of the starting cylinder address for any disk access. At the end of the command, this register is updated to reflect the current cylinder number.

In LBA Mode this register contains Bits 16-23. At the end of the command, this register is updated to reflect the current LBA Bits 16-23.

The cylinder number may be from zero to the number of cylinders minus one.

7.4 Cylinder Low Register

This register contains the low order 8 bits of the starting cylinder address for any disk access. At the end of the command, this register is updated to reflect the current cylinder number.

In LBA Mode this register contains Bits 8-15. At the end of the command, this register is updated to reflect the current LBA Bits 8-15.

The cylinder number may be from zero to the number of cylinders minus one.

7.5 Data Register

This register is used to transfer data blocks between the device data buffer and the host. It is also the register through which sector information is transferred on a Format Track command, and configuration information is transferred on an Identify Drive command.

All data transfers are 16 bits wide, except for ECC byte transfers, which are 8 bits wide. Data transfers are PIO only.

The register contains valid data only when DRQ=1 in the Status Register.

7.6 Device Control Register

Device Control Register							
7	6	5	4	3	2	1	0
—	—	—	—	1	SRST	-IEN	0

Figure 33. Device Control Register

Bit Definitions

- SRST (RST)** Software Reset. The drive is held reset when RST=1. Setting RST=0 re-enables the drive.
- The host must set RST=1 and wait for at least 5 μ seconds before setting RST=0, to ensure that the drive recognizes the reset.
- IEN** Interrupt Enable. When IEN=0, and the drive is selected, drive interrupts to the host will be enabled. When IEN=1, or the drive is not selected, drive interrupts to the host will be disabled.

7.7 Drive Address Register

Drive Address Register							
7	6	5	4	3	2	1	0
HIZ	-WTG	-H3	-H2	-H1	-H0	-DS1	-DS0

Figure 34. Drive Address Register

This register contains the inverted drive select and head select addresses of the currently selected drive.

Bit Definitions

- HIZ** High Impedance. This bit is not driven and will always be in a high impedance state.
- WTG** -Write Gate. This bit is 0 when writing to the disk drive is in progress.
- H3,-H2,-H1,-H0** -Head Select. These four bits are the one's complement of the binary coded address of the currently selected head. H0 is the least significant.

- DS1** -Drive Select 1. Drive select bit for drive 1, active low. DS1=0 when drive 1 (slave) is selected and active.
- DS0** -Drive Select 0. Drive select bit for drive 0, active low. DS0=0 when drive 0 (master) is selected and active.

7.8 Drive/Head Register

Drive/Head Register							
7	6	5	4	3	2	1	0
1	L	1	DRV	HS3	HS2	HS1	HS0

Figure 35. Drive/Head Register

This register contains the drive and head numbers.

Bit Definitions

- L** Binary encoded address mode select. When L=0, addressing is by CHS mode. When L=1, addressing is by LBA mode.
- DRV** Drive. When DRV=0, drive 0 (master) is selected. When DRV=1, drive 1 (slave) is selected.
- HS3,HS2,HS1,HS0** Head Select. These four bits indicate binary encoded address of the head . HS0 is the least significant bit. At a command completion, these bits are updated to reflect the currently selected head.

The head number may be from zero to the number of heads minus one.

In LBA mode, HS3 through HS0 contain bits 24-27 of the LBA. At a command completion, these bits are updated to reflect the current LBA bits 24-27.

7.9 Error Register

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDNF	0	ABRT	TK0NF	AMNF

Figure 36. Error Register

This register contains status from the last command executed by the drive, or a diagnostic code.

At the completion of any command except Execute Drive Diagnostic, the contents of this register are valid always even if ERR=0 in the Status Register.

Following a power on, a reset, or completion of an Execute Drive Diagnostic command, this register contains a diagnostic code. See Figure 40 on page 48 for the definition.

Bit Definitions

BBK	Bad Block. BBK=1 indicates a bad block mark was detected in the requested sector's ID field.
UNC	Uncorrectable Data Error. UNC=1 indicates an uncorrectable data error has been encountered.
IDNF (IDN)	ID Not Found. IDN=1 indicates the requested sector's ID field could not be found.
ABRT (ABT)	Aborted Command. ABT=1 indicates the requested command has been aborted due to a drive status error or an invalid parameter in an output register.
TK0NF (T0N)	Track 0 Not Found. T0N=1 indicates track 0 was not found during a Recalibrate command.
AMNF (AMN)	Address Mark Not Found. AMN=1 indicates the data address mark has not been found after finding the correct ID field for the requested sector.

7.10 Features Register

This register is command specific. This is used with the Set Features command.

7.11 Sector Count Register

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the drive. If the value in the register is set to 0, a count of 256 sectors is specified.

If the register is zero at command completion, the command was successful. If not successfully completed, the register contains the number of sectors which need to be transferred in order to complete the request.

The contents of the register are defined otherwise on some commands. These definitions are given in the command descriptions.

7.12 Sector Number Register

This register contains the starting sector number for any disk data access for the subsequent command. The sector number is from one to the maximum number of sectors per track.

In LBA mode, this register contains Bits 0-7. At the end of the command, this register is updated to reflect the current LBA Bits 0-7.

7.13 Status Register

Status Register							
7	6	5	4	3	2	1	0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

Figure 37. Status Register

This register contains the drive status. The contents of this register are updated whenever an error occurs and at the completion of each command.

If the host reads this register when an interrupt is pending, it is considered to be the interrupt acknowledge. Any pending interrupt is cleared whenever this register is read.

If BSY=1, no other bits in the register are valid.

Bit Definitions

BSY	Busy. BSY=1 whenever the drive is accessing the registers. The host should not read or write any registers when BSY=1. If the host reads any register when BSY=1, the contents of the Status Register will be returned.
DRDY (RDY)	Drive Ready. RDY=1 indicates that the drive is capable of responding to a command. RDY will be set to 0 during power on until the drive is ready to accept a command. If the drive detects an error while processing a command, RDY is set to 0 until the Status Register is read by the host, at which time RDY is set back to 1.
DWF	Drive Write Fault. DWF=1 indicates that the drive has detected a write fault condition. DWF is set to 0 after the Status Register is read by the host.
DSC	Drive Seek Complete. DSC=1 indicates that a seek has completed and the drive head is settled over a track. DSC is set to 0 by the drive just before a seek begins. When an error occurs, this bit is not changed until the Status Register is read by the host, at which time the bit again indicates the current seek complete status.
DRQ	Data Request. DRQ=1 indicates that the drive is ready to transfer a word or byte of data between the host and the drive. The host should not write the Command register when DRQ=1.
CORR (COR)	Corrected Data. COR=1 indicates that a correctable data error was encountered and the data has been corrected using the drive's ECC. The sector buffer contains the corrected data and multi-sector reads continue. The bit is set to 0 when a command is received. During multi-sector reads, COR=1 only while DRQ=1 for the sector or sectors containing correctable errors. During a multi-sector read verify operation, COR is set to 1 at the end of the operation if any of the verified sectors contained a correctable error.
IDX	Index. IDX=1 once per revolution. Since IDX=1 only for a very short time during each revolution, the host may not see it set to 1 even if the host is reading the Status Register continuously. Therefore the host should not attempt to use IDX for timing purposes.
ERR	Error. ERR=1 indicates that an error occurred during execution of the previous command. The Error Register should be read to determine the error type. The drive sets ERR=0 when the next command is received from the host.

8.0 Reset Response

There are three types of reset in ATA as follows:

Power On Reset (POR)

Hard Reset (Hardware Reset) RESET signal is negated in ATA Bus.

Soft Reset (Software Reset) SRST bit is set in the Drive Control Register.

The actions of each reset is shown in Figure 38

	POR	hard reset	soft reset
Aborting Host interface	—	0	0
Aborting Drive operation	—	0	Note.1
Initialization of hardware	0	0	x
Internal diagnostics.	0	0	x
Spinning spindle	0	0	x
Initialization of registers (Note.2)	0	0	0
DASP handshake	0	0	x
PDIAG handshake	0	0	0
Reverting programmed parameters to default	0	0	Note.3
— Number of CHS			
(set by Initialize Drive Parameter)			
— Multiple mode			
— Write cache			
— Read look-ahead			
— ECC bytes			
Disable automatic power down	0	0	x
Power mode	Idle	Idle	Note.4

0 — execute
x — not execute

Figure 38. Reset Response Table

Note 1. Execute after the data in write cache has been written.

Note 2. Default value on POR is shown in Figure 39 on page 48.

Note 3. The Set Features command with Feature register = CCh enables the device to revert these parameters to the power on defaults.

Note 4. In the case of sleep mode, the drive goes to idle mode. In other case, the drive does not change the current mode.

8.1.1 Register Initialization

Register	Default Value
Error	Diagnostic Code
Sector Count	01h
Sector Number	01h
Cylinder Low	00h
Cylinder High	00h
Drive/Head	A0h
Status	50h
Alternate Status	50h

Figure 39. Default Register Values

After power on, hard reset, or software reset, the register values are initialized as shown in Figure 39.

Code	Description
01h	No error detected
02h	Formatter device error
03h	Sector buffer error
04h	ECC circuitry error
05h	Controller microprocessor error
8xh	Slave drive failed

Figure 40. Diagnostic Codes

The meaning of the Error Register diagnostic codes resulting from power on, hard reset or the Execute Drive Diagnostic command are shown in Figure 40.

9.0 Command Protocol

The commands are grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined below.

For all commands, the host must first check if BSY=1, and should proceed no further unless and until BSY=0. For all commands except Execute Drive Diagnostics and Initialize Drive Parameters the host must also wait for RDY=1 before proceeding.

A device must maintain either BSY=1 or DRQ=1 at all times until the command is completed. The INTRQ signal is used by the device to signal most, but not all, times when the BSY bit is changed from 1 to 0 during command execution.

A command shall only be interrupted with a hardware or software reset. The result of writing to the Command register while BSY=1 or DRQ=1 is unpredictable and may result in data corruption. A command should only be interrupted by a reset at times when the host thinks there may be a problem, such as a device that is no longer responding.

Interrupts are cleared when the host reads the Status Register, issues a reset, or writes to the Command Register.

Figure 71 on page 99 shows the drive timeout values.

9.1 Data In Commands

These commands are:

- Identify Drive
- Read Buffer
- Read Long
- Read Multiple
- Read Sectors

Execution includes the transfer of one or more 512 bytes (>512 bytes on Read Long) sectors of data from the drive to the host.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Drive/Head Registers.
2. The host writes the command code to the Command Register.
3. For each sector (or block) of data to be transferred:
 - a. The drive sets BSY=1 and prepares for data transfer.
 - b. When a sector (or block) of data is available for transfer to the host, the drive sets BSY=0, sets DRQ=1, and interrupts the host.
 - c. In response to the interrupt, the host reads the Status Register.
 - d. The drive clears the interrupt in response to the Status Register being read.
 - e. The host reads one sector (or block) of data via the Data Register.
 - f. The drive sets DRQ=0 after the sector (or block) has been transferred to the host.

4. For the Read Long command:
 - a. The drive sets BSY=1 and prepares for data transfer.
 - b. When the sector of data is available for transfer to the host, the drive sets BSY=0, sets DRQ=1, and interrupts the host.
 - c. In response to the interrupt, the host reads the Status Register.
 - d. The drive clears the interrupt in response to the Status Register being read.
 - e. The host reads the sector of data via the Data Register.
 - f. The drive sets DRQ=0 after the sector has been transferred to the host.
 - g. The drive sets DRQ=1 when the ECC bytes are available for transfer to the host.
 - h. In response to DRQ=1, the host reads the ECC bytes via the Data Register.
 - i. The drive sets DRQ=0 after the ECC bytes have been transferred to the host.

The Read Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.

Note that the status data for a sector of data is available in the Status Register **before** the sector is transferred to the host.

If the drive detects an invalid parameter, then it will abort the command by setting BSY=0, ERR=1, ABT=1, and interrupting the host.

If an error occurs, the drive will set BSY=0, ERR=1, and DRQ=1. The drive will then store the error status in the Error Register, and interrupt the host. The registers will contain the location (CHS) of the sector in error.

If an Uncorrectable Data Error (UNC=1) occurs, the defective data will be transferred from the media to the sector buffer, and will be available to be transferred to the host, at the host's option. In case of Read Multiple command, the host should complete transfer the block which includes error from the sector buffer and terminate whatever kind of type of error occurred.

If an error occurs that is correctable by retries, the data will be corrected and the transfer will continue normally. There will be no indication to the host that any retry occurred.

All data transfers to the host through the Data Register are 16 bits, except for the ECC bytes, which are 8 bits.

9.2 Data Out Commands

These commands are:

- Format Track
- Write Buffer
- Write Long
- Write Multiple
- Write Sectors

Execution includes the transfer of one or more 512 bytes (>512 bytes on Write Long) sectors of data from the host to the drive.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Drive/Head Registers.
2. The host writes the command code to the Command Register.
3. The drive sets BSY=1.
4. For each sector (or block) of data to be transferred:
 - a. The drive sets BSY=0 and DRQ=1 when it is ready to receive a sector (or block).
 - b. The host writes one sector (or block) of data via the Data Register.
 - c. The drive sets BSY=1 after it has received the sector (or block).
 - d. When the drive has finished processing the sector (or block), it sets BSY=0, and interrupts the host.
 - e. In response to the interrupt, the host reads the Status Register.
 - f. The drive clears the interrupt in response to the Status Register being read.
5. For the Write Long command:
 - a. The drive sets BSY=0 and DRQ=1 when it is ready to receive a sector.
 - b. The host writes one sector of data via the Data Register.
 - c. The drive sets BSY=1 after it has received the sector.
 - d. When the drive has finished processing the sector, it sets BSY=0 and DRQ=1.
 - e. In response to DRQ=1, the host writes the ECC bytes via the Data Register.
 - f. After receiving the ECC bytes, the drive sets BSY=1.
 - g. After processing the ECC bytes, the drive sets BSY=0 and interrupts the host.
 - h. In response to the interrupt, the host reads the Status Register.
 - i. The drive clears the interrupt in response to the Status Register being read.

The Write Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.

If the drive detects an invalid parameter, then it will abort the command by setting BSY=0, ERR=1, ABT=1, and interrupting the host.

If an uncorrectable error occurs, the drive will set BSY=0 and ERR=1, store the error status in the Error Register, and interrupt the host. The registers will contain the location (CHS) of the sector in error.

All data transfers to the drive through the Data Register are 16 bits, except for the ECC bytes, which are 8 bits.

9.3 Non-Data Commands

These commands are:

- Check Power Mode
- Execute Drive Diagnostics
- Idle
- Idle Immediate
- Initialize Drive Parameters

- Read Verify Sectors
- Recalibrate
- Seek
- Set Features
- Set Multiple
- Sleep
- Standby
- Standby Immediate

Execution of these commands involves no data transfer.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Drive/Head Registers.
2. The host writes the command code to the Command Register.
3. The drive sets BSY=1.
4. When the drive has finished processing the command, it sets BSY=0, and interrupts the host.
5. In response to the interrupt, the host reads the Status Register.
6. The drive clears the interrupt in response to the Status Register being read.

9.4 DMA Data Transfer Commands

These commands are:

- Read DMA
- Write DMA

Data transfer using DMA commands differ in two ways from PIO transfers:

- data transfers are performed using the slave-DMA channel
- no intermediate sector interrupts are issued on multi-sector commands

Initiation of the DMA transfer commands is identical to the Read Sector or Write Sector commands except that the host initializes the slave-DMA channel prior to issuing the command.

The interrupt handler for DMA transfers is different in that:

- no intermediate sector interrupts are issued on multi-sector commands
- the host resets the DMA channel prior to reading status from the drive.

The DMA protocol allows high performance multi-tasking operating systems to eliminate processor overhead associated with PIO transfers.

1. Host initializes the slave-DMA channel
2. Host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder and Drive/Head registers.
3. Host writes command code to the Command Register
4. The drive sets DMARQ when it is ready to transfer any part of the data.

5. Host transfers the data using the DMA transfer protocol currently in effect.
6. When all of the data has been transferred, the drive generates an interrupt to the host.
7. Host resets the slave-DMA channel
8. Host reads the Status Register and, optionally, the Error Register

10.0 Command Descriptions

Command	Hex Code	Binary Code							
		7	6	5	4	3	2	1	0
Check Power Mode	E5	1	1	1	0	0	1	0	1
Check Power Mode*	98	1	0	0	1	1	0	0	0
Execute Drive Diagnostics	90	1	0	0	1	0	0	0	0
Format Track	50	0	1	0	1	0	0	0	0
Identify Drive	EC	1	1	1	0	1	1	0	0
Idle	E3	1	1	1	0	0	0	1	1
Idle*	97	1	0	0	1	0	1	1	1
Idle Immediate	E1	1	1	1	0	0	0	0	1
Idle Immediate*	95	1	0	0	1	0	1	0	1
Initialize Drive Parameters	91	1	0	0	1	0	0	0	1
Read Buffer	E4	1	1	1	0	0	1	0	0
Read DMA (retry)	C8	1	1	0	0	1	0	0	0
Read DMA (no retry)	C9	1	1	0	0	1	0	0	1
Read Long (retry)	22	0	0	1	0	0	0	1	0
Read Long (no retry)	23	0	0	1	0	0	0	1	1
Read Multiple	C4	1	1	0	0	0	1	0	0
Read Sectors (retry)	20	0	0	1	0	0	0	0	0
Read Sectors (no retry)	21	0	0	1	0	0	0	0	1
Read Verify Sectors (retry)	40	0	1	0	0	0	0	0	0
Read Verify Sectors (no retry)	41	0	1	0	0	0	0	0	1
Recalibrate	1x	0	0	0	1	—	—	—	—
Seek	7x	0	1	1	1	—	—	—	—
Set Features	EF	1	1	1	0	1	1	1	1
Set Multiple	C6	1	1	0	0	0	1	1	0
Sleep	E6	1	1	1	0	0	1	1	0
Sleep*	99	1	0	0	1	1	0	0	1
Standby	E2	1	1	1	0	0	0	1	0
Standby*	96	1	0	0	1	0	1	1	0
Standby Immediate	E0	1	1	1	0	0	0	0	0
Standby Immediate*	94	1	0	0	1	0	1	0	0

Commands marked * are alternate command codes.

Figure 41. Command Set

Command	Hex Code	Binary Code							
		7	6	5	4	3	2	1	0
Write Buffer	E8	1	1	1	0	1	0	0	0
Write DMA (retry)	CA	1	1	0	0	1	0	1	0
Write DMA (no retry)	CB	1	1	0	0	1	0	1	1
Write Long (retry)	32	0	0	1	1	0	0	1	0
Write Long (no retry)	33	0	0	1	1	0	0	1	1
Write Multiple	C5	1	1	0	0	0	1	0	1
Write Sectors (retry)	30	0	0	1	1	0	0	0	0
Write Sectors (no retry)	31	0	0	1	1	0	0	0	1
Write Verify	3C	0	0	1	1	1	1	0	0

Figure 42. Command Set ú-ÿ Continued ú-ÿ

Figure 41 on page 55 and Figure 42 shows the commands that are supported by the drive. The following symbols are used in the command descriptions:

Output Registers

- 0** Indicates that the bit must be set to 0.
- 1** Indicates that the bit must be set to 1.
- D** The drive number bit. Indicates that the drive number bit of the Drive/Head Register should be specified. Zero selects the master drive and one selects the slave drive.
- H** Head number. Indicates that the head number part of the Drive/Head Register is an output parameter and should be specified.
- L** LBA mode. Indicates the addressing mode. Zero specifies CHS mode and one does LBA addressing mode.
- R** Retry. Indicates that the Retry bit of the Command Register should be specified.
- V** Valid. Indicates that the bit is part of an output parameter and should be specified.
- x** Indicates that the hex character is not used.
- Indicates that the bit is not used.

Input Registers

- 0** Indicates that the bit is always set to 0.
- 1** Indicates that the bit is always set to 1.
- H** Head number. Indicates that the head number part of the Drive/Head Register is an input parameter and will be set by the drive.
- V** Valid. Indicates that the bit is part of an input parameter and will be set to 0 or 1 by the drive.
- Indicates that the bit is not part of an input parameter.

The command descriptions show the contents of the Status and Error Registers after the drive has completed processing the command and has interrupted the host.

10.1 Check Power Mode

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	0	1	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	0	0	-	-	0	-	V

Figure 43. Check Power Mode Command (E5h)

The Check Power Mode command will report whether the drive is spun up and the media is available for immediate access.

Input Parameters From The Drive

Sector Count The power mode code. The command returns FFh in the Sector Count Register if the spindle motor is at speed and the drive is not in Standby or Sleep mode. Otherwise, the Sector Count Register will be set to 0.

10.2 Execute Drive Diagnostics

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	-	-	-	-	-
Command	1	0	0	1	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
V	V	V	V	V	V	V	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	0	0	-	-	0	-	0

Figure 44. Execute Drive Diagnostics Command (90h)

The Execute Drive Diagnostics command performs the internal diagnostic tests implemented by the drive. The results of the test are stored in the Error Register.

The normal Error Register bit definitions do not apply to this command. Instead, the register contains a diagnostic code. See Figure 40 on page 48 for the definition.

10.3 Format Track

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H	H
Command	0	1	0	1	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 45. Format Track Command (50h)

The Format Track command formats a single track on the drive. Each good sector of data on the track will be initialized to zero. Any data previously stored on the track will be lost.

The host writes a sector containing a format table to the drive. The format table should contain two bytes for each sector on the track to be formatted. The first byte should contain a descriptor value and the second byte should contain the sector number. The descriptor value should be 0 for a good sector, 20h for an unassign sector, 40h for an assign sector, 80h for a bad sector, and any other descriptor value will be ignored. The remaining bytes of the sector following the format table are ignored.

Since drive performance is optimal at 1:1 interleave, and the drive uses relative block addressing internally, the drive will always format a track in the same way no matter what sector numbering is specified in the format table.

Output Parameters To The Drive

Sector Number In LBA mode, this register specifies LBA address bits 0-7 to be formatted. (L=1)

Cylinder High/Low The cylinder number of the track to be formatted. (L=0)

In LBA mode, this register specifies LBA address bits 8-15 (Low), 16-23 (High) to be formatted. (L=1)

H The head number of the track to be formatted. (L=0)

In LBA mode, this register specifies LBA address bits 24-27 to be formatted. (L=1)

Input Parameters From The Drive

Sector Number	In LBA mode, this register specifies current LBA address bits 0-7. (L=1)
Cylinder High/Low	In LBA mode, this register specifies current LBA address bits 8-15 (Low), 16-23 (High)
H	In LBA mode, this register specifies current LBA address bits 24-27. (L=1)
Error	The Error Register. An Abort error (ABT=1) will be returned under the following conditions: <ul style="list-style-type: none">• The descriptor value does not match the certain value. (except 00h, 20h, 40h and 80h)• The number of assign(40h) exceeds the maximum number of reassign table entry.

In LBA mode, this command formats a single track including the specified LBA.

10.4 Identify Drive

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	1	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 46. Identify Drive Command (ECh)

The Identify Drive command requests the drive to transfer configuration information to the host. The drive will transfer a sector to the host containing the information in Figure 47 on page 62.

Word	Content	Description
00	045AH	Drive classification, bit assignments: 15(=0): 1=not magnetic disk drive 14(=0): 1=format speed tolerance gap required 13(=0): 1=track offset option available 12(=0): 1=data strobe offset option available 11(=0): 1=rotational speed tolerance > 0.5% 10(=1): 1=disk transfer rate > 10 Mbps 9(=0): 1=disk transfer rate > 5 Mbps but <= 10 Mbps 8(=0): 1=disk transfer rate <= 5 Mbps 7(=0): 1=removable cartridge drive 6(=1): 1=fixed drive 5(=0): 1=spindle motor control option implemented 4(=1): 1=head switch time > 15 us 3(=1): 1=not MFM encoded 2(=0): 1=soft sectored 1(=1): 1=hard sectored 0(=0): reserved
01	Note.1	Number of cylinders in default translate mode
02	0	Number of removable cylinders
03	Note.1	Number of heads in default translate mode
04	0	Reserved
05	0	Reserved
06	Note.1	Number of sectors per track in default translate mode
07	0000H	Number of bytes of sector gap
08	0000H	Number of bytes in sync field
09	0000H	Reserved
10-19	XXXX	Serial number in ASCII (0 = not specified)
20	0003H	Controller type: 0003: dual ported, multiple sector buffer with look-ahead read
21	00C0H	Buffer size in 512-byte increments
22	0012H	Number of ECC bytes (Vendor unique length selected via set feature cmd)
23-26	XXXX	Microcode version in ASCII
27-46	Note.2	Model number in ASCII
47	0010H	Number of sectors that can be transferred per interrupt on Read and Write Multiple commands
48	0000H	Capable of double word I/O, '0000'= cannot perform
49	0F00H	Capabilities, bit assignments: 15-12(=0) Reserved 11(=1) IORDY Supported 10(=1) IORDY can be disabled 9(=1) 1=LBA Supported 8(=1) 1=DMA Supported 7- 0(=0) Reserved
50	0000H	Reserved
51	0200H	PIO data transfer cycle timing mode

Figure 47. Identify drive information

Word	Content	Description
52	0200H	DMA data transfer cycle timing mode Refer Word 62 and 63
53	0003H	Validity flag of the word 15- 2(=0) Reserved 1 1= Word 64-70 are Valid 0 1= Word 54-58 are Valid
54	XXXXH	Number of current cylinders
55	XXXXH	Number of current heads
56	XXXXH	Number of current sectors per track
57-58	XXXXH	Current capacity in sectors Word 57 specifies the low word of the capacity
59	0XXXH	Current Multiple setting. bit assignments 15- 9(=0) Reserved 8 1= Multiple Sector Setting is Valid 7- 0 xxh = Current setting for number of sectors
60-61	Note.3	Total Number of User Addressable Sectors Word 60 specifies the low word of the number
62	xx07H	Single Word DMA Transfer Capability 15- 8 Single word DMA transfer mode active 7- 0(=7) Single word DMA transfer modes supported (support mode 0,1 and 2)
63	xx03H	Multiword DMA Transfer Capability 15- 8 Multi word DMA transfer mode active 7- 0(=3) Multi word DMA transfer modes supported (support mode 0 and 1)
64	0001H	Flow Control PIO Transfer Modes Supported 15- 8(=0) Reserved 7- 0(=1) Advanced PIO Transfer Modes Supported '01' = PIO Mode 3 Supported
65	00B4H	Minimum Multiword DMA Transfer Cycle Time Per Word 15- 0(=B4h) Cycle time in nanoseconds (180ns, 11.1MB/s)
66	00B4H	Manufacturer's Recommended Multiword DMA Transfer Cycle Time 15- 0(=B4h) Cycle time in nanoseconds (180ns, 11.1MB/s)
67	00B4H	Minimum PIO Transfer Cycle Time Without Flow Control 15- 0(=B4h) Cycle time in nanoseconds (180ns, 11.1MB/s)
68	00B4H	Minimum PIO Transfer Cycle Time With IORDY Flow Control 15- 0(=B4h) Cycle time in nanoseconds (180ns, 11.1MB/s)
69-127	0000H	Reserved
128	XXXXH	Reserved
129	XXXXH	Current Set Feature Option. Bit assignments 0 Write Cache 1= Enable 1 Read Look-ahead 1= Enable 2 Reverting 1= Enable 3 Auto reassign 1= Enable 4-15 Reserved
130-255	0000H	Reserved

Figure 48. Identify drive information

Note 1. The number of cylinder/head/sector for DALA-3540 (541 MB),and DALA-3540 (541 MB) as follows.

DALA-3540 (540MB)	Cylinder 0419H, Head 10H, Sector 3FH
DALA-3540 (528MB)	Cylinder 0400H, Head 10H, Sector 3FH

Note 2. The model number in ASCII is 'IBM-DALA-3540 (541 MB)'.

Note 3. Total number of user addressable sectors is 102270h for DALA-3540 (541 MB), or FC000h for DALA-3540 (528 MB).

10.5 Idle

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	0	0	1	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 49. Idle Command (E3h)

The Idle command causes the drive to enter Idle mode.

When the Idle mode is entered, the drive is spun up to operating speed. If the drive is already spinning, the spin up sequence is not executed.

During Idle mode the drive is spinning and ready to respond to host commands immediately.

The automatic power down sequence is enabled and the timer starts counting down.

Output Parameters To The Drive

Sector Count Timeout Parameter. If zero, then the automatic power down sequence is disabled. If non-zero, then the automatic power down sequence is enabled, and the timeout interval is set to the Timeout Parameter times 5, in seconds, for the value range from 12 to 255. If the value is 1 to 11, the Timeout Parameter is 60 seconds.

When the automatic power down sequence is enabled, the drive will enter Standby mode automatically if the timeout interval expires with no drive access from the host. The timeout interval will be reinitialized if there is a drive access before the timeout interval expires.

10.6 Idle Immediate

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	0	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 50. Idle Immediate Command (E1h)

The Idle Immediate command causes the drive to enter Idle mode. The drive is spun up to operating speed. If the drive is already spinning, the spin up sequence is not executed.

During Idle mode the drive is spinning and ready to respond to host commands immediately.

The Idle Immediate command will not affect to auto power down timeout parameter.

10.7 Initialize Drive Parameters

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	H	H	H	H
Command	1	0	0	1	0	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	0	0	-	-	0	-	V

Figure 51. Initialize Drive Parameters Command (91h)

The Initialize Drive Parameters command enables the host to set the number of sectors per track and the number of heads minus 1, per cylinder. Words 54-58 in Identify Drive Information reflects these parameters.

The parameters remain in effect until following events:

- Another Initialize Drive Parameters command is received.
- The drive is powered off.
- Hard reset is occurred.
- Soft reset is occurred and the Set Feature option of CCh is set instead of 66h.

Output Parameters To The Drive

Sector Count The number of sectors per track. 0 does not mean there are 256 sectors per track, but there is no sector per track.

H The number of heads minus 1 per cylinder. The minimum is 0 and the maximum is 15. However inline with ATA-2 any other value will be accepted but drive operation is then not guaranteed.

10.8 Read Buffer

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	0	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 52. Read Buffer Command (E4h)

The Read Buffer command transfers a sector from the sector buffer to the host. The sector is transferred through the Data Register 16 bits at a time.

The sector transferred will be from the same part of the buffer written to by the last Write Buffer command. The contents of the sector may be different if any reads or writes have occurred since the Write Buffer command was issued.

10.9 Read DMA

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	1	0	0	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
V	0	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 53. Read DMA Command (C8h/C9h)

The Read DMA command transfers one or more sectors from the drive to the host. The sectors are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. The data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The drive issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Output Parameters To The Drive

Sector Count The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number The sector number of the first sector to be transferred. (L=0)
In LBA mode, this register specifies LBA address bits 0-7 to be transferred. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)
In LBA mode, this register specifies LBA address bits 8-15 (Low) 16-23 (High) to be transferred. (L=1)

H The head number of the first sector to be transferred. (L=0)
In LBA mode, this register specifies LBA bits 24-27 to be transferred. (L=1)

R The retry bit. If set to one, then retries are disabled.

Input Parameters From The Drive

Sector Count The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.

Sector Number The sector number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 0-7. (L=1)

Cylinder High/Low The cylinder number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 8-15 (Low), 16-23 (High). (L=1)

H The head number of the sector to be transferred. (L=0)
In LBA mode, this register contains current LBA bits 24-27. (L=1)

10.10 Read Long

Command Block Output Registers							
Register	7	6	5	4	3	2	1 0
Data	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-
Sector Count	0	0	0	0	0	0	0 1
Sector Number	V	V	V	V	V	V	V V
Cylinder Low	V	V	V	V	V	V	V V
Cylinder High	V	V	V	V	V	V	V V
Drive/Head	1	L	1	D	H	H	H H
Command	0	0	1	0	0	0	1 R

Command Block Input Registers							
Register	7	6	5	4	3	2	1 0
Data	-	-	-	-	-	-	-
Error	...See Below...						
Sector Count	-	-	-	-	-	-	V
Sector Number	V	V	V	V	V	V	V V
Cylinder Low	V	V	V	V	V	V	V V
Cylinder High	V	V	V	V	V	V	V V
Drive/Head	-	-	-	-	H	H	H H
Status	...See Below...						

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 54. Read Long Command (22h/23h)

The Read Long command transfers the data and ECC bytes of the designated sector from the drive to the host.

After 512 bytes of data have been transferred, the drive will set DRQ=1 to indicate that the drive is ready to transfer the ECC bytes to the host. The data is transferred 16 bits at a time, and the ECC bytes are transferred 8 bits at a time. The number of ECC bytes are 4 or 18 according to setting of Set Feature option. The default setting is 4 bytes of ECC data.

Output Parameters To The Drive

- Sector Count** The number of continuous sectors to be transferred. The Sector Count must be set to one.
- Sector Number** The sector number of the sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 0-7. (L=1)
- Cylinder High/Low** The cylinder number of the sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 8-15 (Low), 16-23 (High). (L=1)
- H** The head number of the sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 24-27. (L=1)
- R** The retry bit. If set to one, then retries are disabled.

Input Parameters From The Drive

Sector Count	The number of requested sectors not transferred.
Sector Number	The sector number of the transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0-7. (L=1)
Cylinder High/Low	The cylinder number of the transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8-15 (Low), 16-23 (High). (L=1)
H	The head number of the transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24-27. (L=1)

It should be noted that the drive internally uses 18 bytes of ECC data on all data written or read from the disk. The 4 byte mode of operation is provided via an emulation. It is recommended that for testing the effectiveness and integrity of the drives ECC functions that the 18 byte ECC mode should be used.

10.11 Read Multiple

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	0	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	V	-	V

Figure 55. Read Multiple Command (C4h)

The Read Multiple command transfers one or more sectors from the drive to the host. The sectors are transferred through the Data Register 16 bits at a time. Command execution is identical to the Read Sectors command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector.

Output Parameters To The Drive

Sector Count The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number The sector number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 0-7. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 8-15 (Low), 16-23 (High). (L=1)

H The head number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 24-27. (L=1)

Input Parameters From The Drive

Sector Count The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.

Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0-7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8-15 (Low), 16-23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24-27. (L=1)

10.12 Read Sectors

Command Block Output Registers							
Register	7	6	5	4	3	2	1 0
Data	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H
Command	0	0	1	0	0	0	R

Command Block Input Registers							
Register	7	6	5	4	3	2	1 0
Data	-	-	-	-	-	-	-
Error	...See Below...						
Sector Count	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V
Drive/Head	-	-	-	-	H	H	H
Status	...See Below...						

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	V	-	V

Figure 56. Read Sectors Command (20h/21h)

The Read Sectors command transfers one or more sectors from the drive to the host. The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Output Parameters To The Drive

- Sector Count** The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
- Sector Number** The sector number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 0-7. (L=1)
- Cylinder High/Low** The cylinder number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 8-15 (Low), 16-23 (High). (L=1)
- H** The head number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 24-27. (L=1)
- R** The retry bit. If set to one, then retries are disabled.

Input Parameters From The Drive

- Sector Count** The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.

Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0-7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8-15 (Low), 16-23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24-27. (L=1)

10.13 Read Verify

Command Block Output Registers							
Register	7	6	5	4	3	2	1 0
Data	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H
Command	0	0	1	0	0	0	R

Command Block Input Registers							
Register	7	6	5	4	3	2	1 0
Data	-	-	-	-	-	-	-
Error	...See Below...						
Sector Count	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V
Drive/Head	-	-	-	-	H	H	H
Status	...See Below...						

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	V	-	V

Figure 57. Read Verify Sectors Command (40h/41h)

The Read Verify Sectors verifies one or more sectors on the drive. No data is transferred to the host.

If an uncorrectable error occurs, the read verify will be terminated at the failing sector.

Output Parameters To The Drive

Sector Count The number of continuous sectors to be verified. If zero is specified, then 256 sectors will be verified.

Sector Number The sector number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 0-7. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 8-15 (Low), 16-23 (High). (L=1)

H The head number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 24-27. (L=1)

R The retry bit. If set to one, then retries are disabled.

Input Parameters From The Drive

Sector Count The number of requested sectors not verified. This will be zero, unless an unrecoverable error occurs.

Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0-7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8-15 (Low), 16-23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24-27. (L=1)

10.14 Recalibrate

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	0	0	0	1	-	-	-	-

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	V	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 58. Recalibrate Command (1xh)

The Recalibrate command moves the read/write heads from anywhere on the disk to cylinder 0. If the drive cannot reach cylinder 0, T0N (Track 0 Not Found) will be set in the Error Register.

10.15 Seek

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H	H
Command	0	1	1	1	-	-	-	-

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 59. Seek Command (7xh)

The Seek command initiates a seek to the designated track and selects the designated head. The drive need not be formatted for a seek to execute properly. The drive will wait for the seek to complete before setting BSY=0, DSC=1, and issuing the interrupt.

Output Parameters To The Drive

Sector Number In LBA mode, this register specifies LBA address bits 0-7 for seek. (L=1)

Cylinder High/Low The cylinder number of the seek.

In LBA mode, this register specifies LBA address bits 8-15 (Low), 16-23 (High) for seek. (L=1)

H The head number of the seek.

In LBA mode, this register specifies LBA address bits 24-27 for seek. (L=1)

Input Parameters From The Drive

Sector Number In LBA mode, this register contains current LBA bits 0-7. (L=1)

Cylinder High/Low In LBA mode, this register contains current LBA bits 8-15 (Low), 16-23 (High). (L=1)

H In LBA mode, this register contains current LBA bits 24-27. (L=1)

10.16 Set Features

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	V	V	V	V	V	V	V	V
Sector Count	Note.1							
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	1	1	1	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 60. Set Features Command (EFh)

The Set Feature command is to establish the following parameters which affect the execution of certain features as shown in below table.

ABT will be set to 1 in the Error Register if the Feature register contains any undefined values.

Output Parameters To The Drive

Feature	Destination code for this command.
02H	Enable write cache (Warning.1)
03H	Set transfer mode based on value in sector count register
44H	18 bytes of ECC apply on Read Long/Write Long commands
55H	Disable read look-ahead feature
66H	Disable reverting to power on defaults
82H	Disable write cache
AAH	Enable read look-ahead feature
BBH	4 bytes of ECC apply on Read Long/Write Long commands
CCH	Enable reverting to power on defaults

Warning 1. Hard reset or power off must not be done in 5 seconds after write command completion when write cache is enabled.

Note 1.

When Feature register is 03h (=Set Transfer mode), the Sector Count Register specifies the transfer mechanism. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value.

PIO Default Transfer Mode	00000	000
PIO Default Transfer Mode,Disable IORDY	00000	001
PIO Flow Control Transfer Mode x	00001	nnn (nnn=000,001,010,011)
Single word DMA mode x	00010	nnn (nnn=000,001,010)
Multiword DMA mode x	00100	nnn (nnn=000,001)

Note 2.

If the number of auto reassigned sector reaches the drive's reassignment capacity, the write cache function will be automatically disabled. Although the drive still accepts the Set Features command with Feature register = 02h without error, but the write cache function will remains disabled. For current write cache function status, please refer to Identify Drive Information(129word) by Identify Drive command.

Note 3.

After power on reset, the drive is set to the following features as default.

Write cache	:	Enable
ECC bytes	:	4 bytes
Read look-ahead	:	Enable
Reverting to power on defaults	:	Disable

10.17 Set Multiple

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	0	0	0	1	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 61. Set Multiple Command (C6h)

The Set Multiple command enables the drive to perform Read and Write Multiple commands and establishes the block size for these commands. The block size is the number of sectors to be transferred for each interrupt.

The default block size after power up, soft reset, or hard reset is 0, and Read Multiple and Write Multiple commands are disabled.

If an invalid block size is specified, an Abort error will be returned to the host, and Read Multiple and Write Multiple commands will be disabled.

Output Parameters To The Drive

Sector Count. The block size to be used for Read Multiple and Write Multiple commands. Valid block sizes can be selected from 0, 2, 4, 8 or 16. If 0 is specified, then Read Multiple and Write Multiple commands are disabled.

10.18 Sleep

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	0	1	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 62. Sleep Command (E6h)

The Sleep command causes the drive to enter into sleep mode, which is its minimal power mode. If the drive is not already spun down, the spin down sequence is executed. After the disk rotation has stopped, BSY is cleared and an interrupt is requested to a host.

The drive in the sleep mode will respond to commands, but there may be a delay while waiting for the disk to rotate at the operating speed.

10.19 Standby

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	0	0	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 63. Standby Command (E2h)

The Standby command causes the drive to enter the Standby Mode.

When the Standby mode is entered, the drive is spun down but the interface remains active. If the drive is already spun down, the spin down sequence is not executed.

During the Standby mode the drive will respond to commands, but there is a delay while waiting for the spindle to reach operating speed.

The automatic power down sequence is enabled and the timer starts counting down when the drive returns to Idle mode.

Output Parameters To The Drive

Sector Count Timeout Parameter. If zero, then the automatic power down sequence is disabled. If non-zero, then the automatic power down sequence is enabled, and the timeout interval is set to the Timeout Parameter times 5, in seconds, for the value range from 12 to 255. If the value is 1 to 11, the Timeout Parameter is 60 seconds.

When the automatic power down sequence is enabled, the drive will enter Standby mode automatically if the timeout interval expires with no drive access from the host. The timeout interval will be reinitialized if there is a drive access before the timeout interval expires.

10.20 Standby Immediate

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 64. Standby Immediate Command (E0h)

The Standby Immediate command causes the drive to enter Standby mode immediately. The drive is spun down but the interface remains active. If the drive is already spun down, the spin down sequence is not executed.

During the Standby mode, the drive will respond to commands, but there is a delay while waiting for the spindle to reach operating speed.

The Standby Immediate command will not affect to auto power down timeout parameter.

10.21 Write Buffer

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	1	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 65. Write Buffer Command (E8h)

The Write Buffer command transfers a sector of data from the host to the sector buffer. The sectors of data are transferred through the Data Register 16 bits at a time.

The Read Buffer and Write Buffer commands are synchronized such that sequential Write Buffer and Read Buffer commands access the same 512 bytes within buffer.

10.22 Write DMA

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	1	0	1	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 66. Write DMA Command (CAh/CBh)

The Write DMA command transfers one or more sectors of data from the host to the drive. The sectors of data are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. Data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The drive issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Output Parameters To The Drive

Sector Count The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number The sector number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 0-7. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 8-15 (Low), 16-23 (High). (L=1)

H The head number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 24-27. (L=1)

R The retry bit. If set to one, then retries are disabled. But ignored, when write cache is enabled. (Ignoring the retry bit is in violation of ATA-2.)

Input Parameters From The Drive

Sector Count The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.

Sector Number The sector number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 0-7. (L=1)

Cylinder High/Low The cylinder number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 8-15 (Low), 16-23 (High). (L=1)

H The head number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 24-27. (L=1)

10.23 Write Long

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	0	0	0	0	0	0	0	1
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H	H
Command	0	0	1	1	0	0	1	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 67. Write Long Command (32h/33h)

The Write Long command transfers the data and ECC bytes of the designated sector from the host to the drive.

After 512 bytes of data have been transferred, the drive will set DRQ=1 to indicate that the drive is ready to receive the ECC bytes from the host. The data is transferred 16 bits at a time, and the ECC bytes are transferred 8 bits at a time. The number of ECC bytes are 4 or 18 according to setting of Set Feature option. The default number after power on is 4 bytes.

Output Parameters To The Drive

- Sector Count** The number of continuous sectors to be transferred. The Sector Count must be set to one.
- Sector Number** The sector number of the sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 0-7. (L=1)
- Cylinder High/Low** The cylinder number of the sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 8-15 (Low), 16-23 (High). (L=1)
- H** The head number of the sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 24-27. (L=1)
- R** The retry bit. If set to one, then retries are disabled.

Input Parameters From The Drive

Sector Count	The number of requested sectors not transferred.
Sector Number	The sector number of the sector to be transferred. (L=0) In LBA mode, this register contains current LBA bits 0-7. (L=1)
Cylinder High/Low	The cylinder number of the sector to be transferred. (L=0) In LBA mode, this register contains current LBA bits 8-15 (Low), 16-23 (High). (L=1)
H	The head number of the sector to be transferred. (L=0) In LBA mode, this register contains current LBA bits 24-27. (L=1)

The file internally uses 18 bytes of ECC on all data read or writes. The 4 byte mode of operation is provided via an emulation technique. As a consequence of this emulation it is recommended that 18 byte ECC mode is used for all tests to confirm the operation of the files ECC hardware. Unexpected results may occur if such testing is performed using 4 byte mode.

The last 2 bytes for 18 bytes ECC data should be always 00H data.

10.24 Write Multiple

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	0	1	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 68. Write Multiple Command (C5h)

The Write Multiple command transfers one or more sectors from the host to the drive. Command execution is identical to the Write Sectors command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector. The sectors are transferred through the Data Register 16 bits at a time.

Output Parameters To The Drive

Sector Count The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number The sector number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 0-7. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 8-15 (Low), 16-23 (High). (L=1)

H The head number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 24-27. (L=1)

Input Parameters From The Drive

Sector Count The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.

Sector Number The sector number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 0-7. (L=1)

Cylinder High/Low The cylinder number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 8-15 (Low), 16-23 (High).
(L=1)

H The head number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 24-27. (L=1)

10.25 Write Sectors

Command Block Output Registers							
Register	7	6	5	4	3	2	1 0
Data	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H
Command	0	0	1	1	0	0	R

Command Block Input Registers							
Register	7	6	5	4	3	2	1 0
Data	-	-	-	-	-	-	-
Error	...See Below...						
Sector Count	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V
Drive/Head	-	-	-	-	H	H	H
Status	...See Below...						

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 69. Write Sectors Command (30h/31h)

The Write Sectors command transfers one or more sectors from the host to the drive. The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Output Parameters To The Drive

- Sector Count** The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
- Sector Number** The sector number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 0-7. (L=1)
- Cylinder High/Low** The cylinder number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 8-15 (Low), 16-23 (High). (L=1)
- H** The head number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 24-27. (L=1)
- R** The retry bit. If set to one, then retries are disabled. But ignored, when write cache is enabled. (Ignoring the retry bit is in violation of ATA-2.)

Input Parameters From The Drive

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0-7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8-15 (Low), 16-23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24-27. (L=1)

10.26 Write Verify

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H	H
Command	0	0	1	1	1	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	V	-	V

Figure 70. Write Verify Command (3Ch)

The Write Verify command transfers one or more sectors from the host to the drive. The sectors are transferred through the Data Register 16 bits at a time. After the sectors are transferred to the drive, a verify operation is performed for each sector.

If an uncorrectable error occurs, the write will be terminated at the failing sector. Any errors encountered during the verify operation will be returned at the final interrupt.

Output Parameters To The Drive

Sector Count The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number The sector number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 0-7. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 8-15 (Low), 16-23 (High). (L=1)

H The head number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 24-27. (L=1)

Input Parameters From The Drive

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0-7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8-15 (Low), 16-23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24-27. (L=1)

11.0 Timings

The timing of BSY and DRQ in Status Register are shown in Figure 71

FUNCTION	INTERVAL	START	STOP	TIMEOUT
Power On	Drive Busy After Power On	Power On	Status Register BSY=1	400 ns
	Drive Ready After Power On	Power On	Status Register BSY=0 and RDY=1	31 sec
Software Reset	Drive Busy After Software Reset	Device Control Register RST=1	Status Register BSY=1	400 ns
	Drive Ready After Software Reset	Device Control Register RST=1	Status Register BSY=0 and RDY=1	6 sec
Hard Reset	Drive Busy After Hard Reset	Bus RESET Signal Asserted	Status Register BSY=1	400 ns
	Drive Ready After Hard Reset	Bus RESET Signal Asserted	Status Register BSY=0 and RDY=1	31 sec
Data In Command	Drive Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns
	Interrupt, DRQ For Data Transfer In	Status Register BSY=1	Status Register BSY=0 and DRQ=1, Interrupt	10 sec
	Drive Busy After Data Transfer In	256th Read From Data Register	Status Register BSY=1	10 us
Data Out Command	Drive Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns
	Data Request For Data Transfer Out	Status Register BSY=1	Status Register BSY=0 and DRQ=1	900 us
	Drive Busy After Data Transfer Out	256th Write From Data Register	Status Register BSY=1	5 us
	Interrupt For Data Transfer Out	Status Register BSY=1	Interrupt	10 sec
Non-Data Command	Drive Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns
	Interrupt For Command Complete	Status Register BSY=1	Interrupt	6 sec

Figure 71. Timeout Values

FUNCTION	INTERVAL	START	STOP	TIMEOUT
DMA Data Transfer Command	Drive Busy after Command Code Out	Out to Command Register	Status Register BSY=1	400 ns

Figure 72. Timeout Values ú-ÿ Continued ú-ÿ

Command category is referred to 9.0, “Command Protocol” on page 49.

The abbreviations "ns", "us", "ms" and "sec" mean nanoseconds, microseconds, milliseconds and seconds, respectively.

12.0 Vendor Unique Functions

12.1 Write Cache Function

Write cache is a performance enhancement whereby the drive reports as completing the write command (Write Sectors and Write Multiple) to the host as soon as the drive has received all of the data into its buffer. And the drive assumes responsibility to write the data subsequently onto the disk.

12.1.1 Attention

- While writing data after completed acknowledgment of a write command, soft reset does not affect its operation. But hard reset or power off terminates writing operation immediately and unwritten data are to be lost. So hard reset or power off must not be done in 5 seconds after the completion of a write command.
- The retry bit of Write Sectors is ignored when write cache is enabled. This is in violation of ATA-2.



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