



OEM HARD DISK DRIVE SPECIFICATIONS

for

DJAA-31270/31700 (1270/1700 MB)

3.5-Inch Hard Disk Drive with ATA Interface

Revision (2.3)



OEM HARD DISK DRIVE SPECIFICATIONS

for

DJAA-31270/31700 (1270/1700 MB)

3.5-Inch Hard Disk Drive with ATA Interface

Revision (2.3)

1st Edition (1.0) S29H-7278-00 (August 11, 1995)
2nd Edition (1.1) S29H-7278-01 (October 11, 1995)
3rd Edition (2.0) S29H-7278-02 (January 10, 1996)
4th Edition (2.1) S29H-7278-03 (January 17, 1996)
5th Edition (2.2) S29H-7278-04 (April 9, 1996)
6th Edition (2.3) S29H-7278-05 (June 21, 1996)

The following paragraph does not apply to the United Kingdom or any country where such provisions are inconsistent with local law: INTERNATIONAL BUSINESS MACHINES CORPORATION PROVIDES THIS PUBLICATION “AS IS” WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Some states do not allow disclaimer or express or implied warranties in certain transactions, therefore, this statement may not apply to You.

This publication could include technical inaccuracies or typographical errors. Changes are periodically made to the information herein; these changes will be incorporated in new editions of the publication. IBM may make improvements and/or changes in the product(s) and/or the program(s) described in this publication at any time.

It is possible that this publication may contain reference to, or information about, IBM products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that IBM intends to announce such IBM products, programming, or services in your country.

Technical information about this product is available from your local IBM representative or at **<http://www.ibm.com/harddrive>**

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Armonk, NY 10577.

© Copyright International Business Machines Corporation 1996. All rights reserved.

Note to U.S. Government Users —Documentation related to restricted rights —Use, duplication or disclosure is subject to restrictions set forth in GSA ADP Schedule Contract with IBM Corp.

Contents

1.0 General	1
1.1 Glossary	1
1.2 General Caution	1
2.0 General Features	3
<hr/>	
Part 1. Functional Specification	5
3.0 Drive Characteristics	7
3.1 Logical Drive Format	7
3.2 Data Sheet	7
3.3 Performance Characteristics	8
3.3.1 Command Overhead	8
3.3.2 Mechanical Positioning	9
3.3.3 Drive Ready Time	11
3.3.4 Data Transfer Speed	11
3.3.5 Buffering Operation (Lookahead/Write Cache)	11
3.3.6 Throughput	12
3.3.7 Operating Mode Definition	13
4.0 Data Integrity	15
4.1 Data loss on Power Off or Hard Reset	15
4.2 Write Cache	15
4.3 Equipment Status	15
5.0 Physical Format	17
5.1 Shipped Format	17
6.0 Specification	19
6.1 Electrical interface specification	19
6.1.1 Connectors	19
6.1.2 Signal Definition	20
6.1.3 Signal Description	21
6.1.4 Interface Logic Signal Levels	23
6.1.5 Reset timings	23
6.1.6 PIO Timings	24
6.1.7 DMA Timings (Single Word)	26
6.1.8 DMA Timings (Multiword)	27
6.1.9 Addressing of drive Registers	28
6.1.10 Cabling	28
6.1.11 Jumper Settings	29
7.0 Specification	33
7.1 Environment	33
7.1.1 Temperature and Humidity	33
7.2 DC Power Requirements	34
7.3 Reliability	35
7.3.1 Cable Noise Interference	35
7.3.2 Contact Start Stop(CSS)	35
7.3.3 Preventive Maintenance	35

7.3.4	Data Reliability	35
7.3.5	Seek/ID Mis-compare Errors	36
7.3.6	Equipment Errors	36
7.4	Mechanical Specifications	37
7.4.1	Outline	37
7.4.2	Mechanical Dimensions and Weight	37
7.4.3	Connector Locations	39
7.4.4	Hole Locations	40
7.4.5	Mounting Orientation	41
7.4.6	Shipping Zone and Lock	41
7.5	Vibration and Shock	42
7.5.1	Operating Vibration	42
7.5.2	Non-Operating Vibrations	43
7.5.3	Operating Shock	44
7.5.4	Non-Operating Shock	44
7.6	Acoustics	45
7.6.1	Sound Power Levels	45
7.6.2	Sound Power Acceptance Criteria	45
7.7	Identification	46
7.7.1	Labels	46
7.8	Electromagnetic Compatibility	46
7.9	Safety	47
7.9.1	Underwriters Lab(UL) Approval	47
7.9.2	Canadian Standards Authority(CSA) Approval	47
7.9.3	IEC Compliance	47
7.9.4	German Safety Mark	47
7.9.5	Flammability	47
7.9.6	Secondary Circuit Protection	47
7.10	Packaging	47

Part 2. ATA Interface Specification	49
8.0 Interface	51
9.0 Vendor Specific Options	53
10.0 Registers	55
10.1 Alternate Status Register	56
10.2 Command Register	56
10.3 Cylinder High Register	56
10.4 Cylinder Low Register	56
10.5 Data Register	57
10.6 Device Control Register	57
10.7 Drive Address Register	57
10.8 Drive/Head Register	58
10.9 Error Register	58
10.10 Features Register	59
10.11 Sector Count Register	59
10.12 Sector Number Register	59
10.13 Status Register	59
11.0 Reset Response	61
11.1.1 Register Initialization	62

12.0 Command Protocol	63
12.1 Data In Commands	63
12.2 Data Out Commands	64
12.3 Non-Data Commands	65
12.4 DMA Data Transfer Commands	66
13.0 Command Descriptions	69
13.1 Check Power Mode	71
13.2 Execute Drive Diagnostics	72
13.3 Execute S.M.A.R.T. FUNCTION	73
13.3.1 Read Attribute Values (subcommand = D0h)	74
13.3.2 Read Attribute Thresholds (subcommand = D1h)	74
13.3.3 Enable/Disable Attribute Autosave (subcommand = D2h)	74
13.3.4 Save Attribute Values (subcommand = D3h)	74
13.3.5 Enable S.M.A.R.T. Operations (subcommand = D8h)	74
13.3.6 Disable S.M.A.R.T. Operations (subcommand = D9h)	74
13.3.7 Return S.M.A.R.T. Status (subcommand = DAh)	75
13.3.8 Drive Attributes Data Structure	75
13.3.9 Drive Attribute Thresholds Data Structure	77
13.3.10 Attribute Values Saving Function	77
13.4 Format Track	79
13.5 Identify Drive	81
13.6 Idle	85
13.7 Idle Immediate	86
13.8 Initialize Drive Parameters	87
13.9 Read Buffer	88
13.10 Read DMA	89
13.11 Read Long	91
13.12 Read Multiple	93
13.13 Read Sectors	95
13.14 Read Verify	97
13.15 Recalibrate	99
13.16 Seek	100
13.17 Set Features	101
13.18 Set Multiple	103
13.19 Sleep	104
13.20 Standby	105
13.21 Standby Immediate	106
13.22 Write Buffer	107
13.23 Write DMA	108
13.24 Write Long	110
13.25 Write Multiple	112
13.26 Write Sectors	114
14.0 Timings	117
14.1 Write Cache Function	119
14.1.1 Attention	119
Index	121

1.0 General

This document describes the characteristics of the following IBM 3.5-inch, ATA interface hard disk drives:

- DJAA-31270 (1270 MB)
- DJAA-31700 (1700 MB)

1.1 Glossary

<i>Word</i>	<i>Meaning</i>
Kbpi	1 000 Bit Per Inch
Mbps	1 000 000 Bit per second
MB	1 000 000 bytes
KB	1 000 bytes
32 KB	32 x 1 024 bytes
64 KB	64 x 1 024 bytes
Mb/sq.in	1 000 000 bits per square inch
MLC	Machine Level Control

1.2 General Caution

The drive can be easily damaged by shocks or ESD (Electric Static Discharge), so any damages applied to the drive after taking out from shipping package and opening ESD protective bag are user's responsibilities.

2.0 General Features

- Sector format of 512 bytes/sector
- Closed-loop actuator servo (Embedded Sector Servo)
- Dedicated head landing zone
- Automatic Actuator lock
- Interleave factor 1:1
- Segmented to 32 Kbytes of buffer implementation
- Seek time of 12 msec in Read Operation
- Write Cache for sequential write operation
- Size of sector buffer is 96 Kbytes
- Advanced ECC On The Fly (EOF)
- Addition to the above, Automatic Error Recovery procedures for read and write commands
- Self Diagnostics on Power on and resident diagnostics
- PIO Data Transfer - Mode 4
- DMA Data Transfer
 - Single Word mode : mode 2 (8.3 MB/sec)
 - Multiword mode : mode 2 (16.6 MB/sec)
- CHS and LBA mode
- Transparent Defect Management with ADR (Automatic Defect Reallocation) during Write Cache
- Power Saving modes
- Spindle 4500 rpm
- S.M.A.R.T. function support

Part 1. Functional Specification

3.0 Drive Characteristics

This chapter provides the characteristics of the drives.

3.1 Logical Drive Format

The customer usable data capacity is as shown below.

Figure 1. Drive Parameter		
Descriptions	DJAA-31270	DJAA-31700
Logical Head Number	16	16
Logical Sectors/Track	63	63
Logical Cylinder Number	2480	3308
Logical Sector Size	512	512
Total Customer Usable Data Sectors	2 499 840	3 334 464
Total Customer Usable Data Bytes	1270 MB (1,279,918,080)	1700 MB (1,707,245,568)

3.2 Data Sheet

Figure 2. Data Sheet	
Media transfer rate [Mb/sec]	38.7 - 62.1
Interface transfer rate [MB/sec]	16.6 MB/sec Max
Data buffer size [KB]	96 KB (3 x 32 KB) (Read/Write)
Rotational speed [RPM]	4500
Average latency [msec]	6.67
Recording density [Kbpi]	99.1 Maximum
Track density [TPI]	6684 Maximum
Areal density [Mb/sq.in.]	662 Maximum
Number of zone	8
Number of disks DJAA-31270 DJAA-31700	2 2
Servo design method	Embedded sector servo

3.3 Performance Characteristics

A file performance is characterized by the following parameters:

- Command Overhead
- Mechanical Positioning
 - Seek Time
 - Latency
- Data Transfer Speed
- Buffering Operation (Lookahead/Write cache)

Note: All the above parameters contribute to file performance. There are other parameters that contribute to the performance of the actual system. This specification tries to define the bare file characteristics, not the system throughput which will depend on the system and the application.

3.3.1 Command Overhead

Command overhead is defined as the time required:

- From the time that the drive is selected
- to the time available for the first data byte of a READ command when the requested data is not in the buffer
- exclude
 - Physical seek time
 - Latency time

Command Case (File is in quiescence state)	Time
Read (Cache not hit)	< 0.7 [msec]
Read (Cache hit)	< 0.6 [msec]
Write	< 0.5 [msec]
Seek	< 0.5 [msec]

Note: The above table gives an average time.

3.3.2 Mechanical Positioning

3.3.2.1 Average Seek Time (Including Settling)

Figure 4. Mechanical Positioning Performance		
Command Type	Typical	Max
Read	12 [msec]	13 [msec]
Write	13 [msec]	14 [msec]

“Typical” and “Max” are given throughout the performance specification by;

Typical Average of the drive population tested at nominal environmental and voltage conditions.
Max Maximum value measured on any one drive over the full range of the environmental and voltage conditions. (See 7.1, “ Environment” on page 33 and 7.2, “ DC Power Requirements” on page 34 for ranges.)

The seek time is measured from the start of actuator's motion to the start of a **reliable read or write operation**. Reliable read or write implies that error correction/recovery is not used to correct arrival problems. The average seek time is measured as the weighted average of all possible seek combinations.

$$\text{Weighted Average} = \frac{\sum_{n=1}^{\max} (\max + 1 - n) (T_{n.in} + T_{n.out})}{(\max + 1) (\max)}$$

Where:

max = Maximum seek length

n = Seek length (1 to max)

T_{n.in} = Inward measured seek time for an n track seek

T_{n.out} = Outward measured seek time for an n track seek

3.3.2.2 Single Track Seek Time

Figure 5. Single Track Seek Time		
Function	Typical	Max.
Read [msec]	2.08	2.41
Write [msec]	2.93	3.80

Single track seek is measured as the average of one (1) single track seek from every track with a **random head switch** in both direction (inward and outward).

The single track seek time is the average of the 1000 single track seeks.

3.3.2.3 Full Stroke Seek

Figure 6. Full Stroke Seek Time		
Function	Typical	Max.
Read [msec]	25	28
Write [msec]	27	30

Full stroke seek is measured as the average of 1000 full stroke seeks with a **random head switch** from both directions (inward and outward).

3.3.2.4 Cylinder Switch Time (Cylinder Skew)

Figure 7. Cylinder Skew	
	Typical
Cylinder Skew	4.2 [msec]

A cylinder switch time is defined as the amount of time required by the fixed disk access the next sequential block after reading the last sector in the current cylinder.

The measured method is given in 3.3.6, “Throughput” on page 12.

3.3.2.5 Head Switch Time (Head Skew)

Figure 8. Head Skew	
	Typical
Head Skew	3.1 [msec]

3.3.2.6 Average Latency

Figure 9. Latency Time		
Rotation	Time for a revolution	Average Latency
4500 [RPM]	13.3 [msec]	6.67 [msec]

3.3.3 Drive Ready Time

Figure 10. Drive Ready Time		
Condition	Typical	Max.
Power On to Ready	10 [sec]	31 [sec]

Ready The condition in which the drive is able to perform a media access command (eg. read, write) immediately.

Power On This includes the time required for the internal self diagnostics.

3.3.4 Data Transfer Speed

Figure 11. Data Transfer Speed	
Description	Typical
Disk-Buffer Transfer (Zone 0)	
(Instantaneous)	6.3 [Mbyte/sec]
(Sustained)	5.0 [Mbyte/sec]
Disk-Buffer Transfer (Zone 7)	
(Instantaneous)	3.9 [Mbyte/sec]
(Sustained)	3.1 [Mbyte/sec]
Buffer-Host	16.6 [Mbyte/sec] (Max)

- Instantaneous disk-buffer transfer rate (Mbyte/sec) is derived by:
 $(\text{Number of sectors on a track}) * 512 * (\text{revolution/sec})$

Note: Number of sectors per track will vary because of the linear density recording.

- Sustained disk-buffer transfer rate (Mbyte/sec) is defined by considering head/cylinder change time. This gives a local average data transfer rate. It is derived by:
 $(\text{Sustained Transfer Rate}) = A / (B + C + D)$

$$A = (\text{Number of data sectors per cylinder}) * 512$$

$$B = ((\text{\# of Surface per cylinder}) - 1) * (\text{Head switch time})$$

$$C = (\text{Cylinder change time})$$

$$D = (\text{\# of Surface}) * (\text{One revolution time})$$

- Instantaneous Buffer-Host Transfer Rate (Mbyte/sec) defines the maximum data transfer rate on AT Bus. It also depends on the speed of the host.

The measurement method is given in 3.3.6, "Throughput" on page 12.

3.3.5 Buffering Operation (Lookahead/Write Cache)

In order to improve the total performance, the file utilizes it's own buffer for lookahead. The total of 96K bytes of the buffer is divided into three segmented blocks. One segment is used for write buffer, and the remaining segments are for read buffers.

Write data will be cached in the buffer for the consecutive blocks request.

3.3.6 Throughput

3.3.6.1 Simple Sequential Access

Figure 12. Simple Sequential Access Performance		
Operation	Typical	Max
Sequential Read/Write (Zone 0)	4.2 [sec]	4.4 [sec]
Sequential Read/Write (Zone 7)	6.3 [sec]	6.6 [sec]

The above table gives the time required to read/write for a total of 8000x consecutive blocks (16,777,216 bytes) accessed by 128 read/write commands. Typical and Max values are given by 105% and 110% of T respectively throughputs following performance description.

Note: Assumes a host system responds instantaneously.

$$T = (A * 128) + B + C + 16,777,216/D + 512/E * 128 + DRQ * 32768 \quad (\text{READ})$$

$$T = (A * 128) + B + C + 16,777,216/D + DRQ * 32768 \quad (\text{WRITE})$$

where:

T = Calculated Time (sec)

A = Command Process Time (Pre/Post Command overhead)

B = Average Seek Time

C = Average Latency

D = Sustained Disk-Buffer Transfer Rate (Mbyte/sec)

E = Buffer-Host Transfer Rate (Mbyte/sec)

3.3.6.2 Random Access

Figure 13. Random Access Performance		
Operation	Typical	Max
Random Read	80 [sec]	88 [sec]
Random Write	83 [sec]	91 [sec]

The above table gives the time required to execute a total of 1000x read/write commands which access a random LBA.

$$T = (A + B + C + 512/D + 512/E + DRQ) * 4096 \quad (\text{READ})$$

$$T = (A + B + C + 512/D) * 4096 \quad (\text{WRITE})$$

where:

T = Calculated Time (sec)

A = Command Process Time (Pre/Post Command overhead)

B = Average Seek Time

C = Average Latency

D = Sustained Disk-Buffer Transfer Rate (Mbyte/sec)

E = Buffer-Host Transfer Rate (Mbyte/sec)

DRQ = Data ReQuest interval (micro second)

3.3.7 Operating Mode Definition

Operating Mode	Description
Spin-Up	Start up time period from spindle stop or power down.
Seek	Seek operation mode
Write	Write operation mode
Read	Read operation mode
Idle	Spindle motor and servo system are working normally. Commands can be received and processed immediately.
Standby	Spindle motor is stopped. Commands can be received immediately, but write or read operations cannot begin until the spindle is spun-up and the Servo system is ready.

Notes:

1. Upon Power down or Spindle stopped, a head locking mechanism will secure the heads in the ID parking position.
2. Recovering from Standby mode does not need soft reset nor hard reset.
3. Sleep command is handled as Standby command.

3.3.7.1 Mode Transition Time

Figure 14. Mode Transition Time			
From	To	Typical	Max
Standby	Idle	8 [sec]	31 [sec]
Idle	Standby	Immediate	N/A

Note: The actual spin down time will exist, however the command will be processed immediately.

4.0 Data Integrity

4.1 Data loss on Power Off or Hard Reset

- Power off or hard reset during any operations except for write operation will not cause any data loss.
- Power off or hard reset during write operation causes the loss of the data which the drive has received but not written on the disk media.
- There is a possibility that power off or hard reset during write operation might make a maximum of 1 sector of data unreadable. This state can be recovered by a re-write operation.

4.2 Write Cache

- When write cache is enabled, there is a possibility that the write command completes before the actual disk write operation finishes. This means that there is a possibility that power off or hard reset¹ even after write command completion might cause the loss of the data which the drive has received but not written on the disk.
- There are three ways to check if the data in the write cache have been written onto the disk. Checking just before power off or hard reset¹ is recommended to prevent data loss.
 - To confirm negation of -DASP signal.
 - To confirm successful completion of Software Reset.
 - To confirm successful completion of the following commands.
Check Power Mode, Execute Drive Diagnostics, Format Track, Identify Drive, Idle, Idle Immediate, Initialize Drive Parameters, Recalibrate, Seek, Set Features, Set Multiple, Sleep, Standby, Standby Immediate.

4.3 Equipment Status

Equipment status is available to the host system any time the drive is not ready to read, write, or seek. This status normally exists at power-on time and will be maintained until the following conditions are satisfied:

- Access recalibration/tuning is complete.
- Spindle speed meets requirements for reliable operation.
- Self-check of drive is complete.

Appropriate error status is made available to the host system if any of the following conditions occur after the drive has once become ready:

- Spindle speed outside requirements for reliable operation.
- Occurrence of a WRITE FAULT condition.

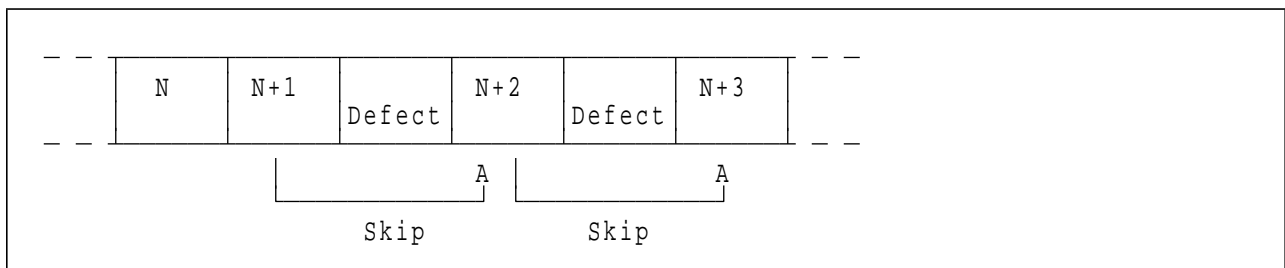
¹ MLC code E15496 (Microcode revision A74B) or later, all data in write cache are flushed onto disk media prior to implementation of Hard Reset.

5.0 Physical Format

Media defects are remapped to the next available sector during Format Process in manufacturing. The mapping from LBA to the physical locations is calculated by an internal maintained table.

5.1 Shipped Format

- Data areas are optimally used.
- No extra sector is wasted as a spare throughout user data areas.
- All pushes generated by defects are absorbed by spare tracks of inner zone.



Defects are skipped without any constraint, such as track or cylinder boundary. The calculation from LBA to physical is done automatically by internal table.

6.0 Specification

6.1 Electrical interface specification

6.1.1 Connectors

6.1.1.1 Power

The DC power connector is designed to mate with AMP (part 1-480424-0) using AMP pins (part 350078-4) strip or (part 61173-4) loose piece, or their equivalents. Pin assignments are shown below.

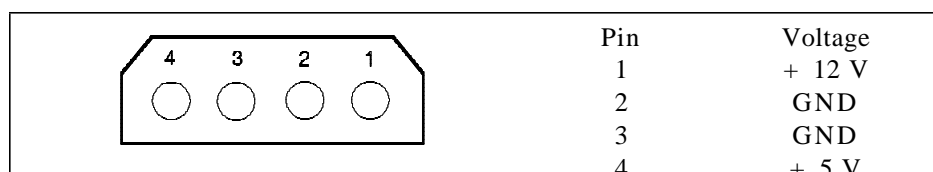


Figure 15. Power Connector Pin Assignments

6.1.1.2 AT Signal Connector

The AT signal connector is a 40-pin connector.

6.1.2 Signal Definition

The pin assignments of interface signals are listed as follows:

PIN	SIGNAL	I/O	Type	PIN	SIGNAL	I/O	Type
01	—HRESET	I	TTL	02	GND		
03	HD07	I/O	3-state	04	HD08	I/O	3-state
05	HD06	I/O	3-state	06	HD09	I/O	3-state
07	HD05	I/O	3-state	08	HD10	I/O	3-state
09	HD04	I/O	3-state	10	HD11	I/O	3-state
11	HD03	I/O	3-state	12	HD12	I/O	3-state
13	HD02	I/O	3-state	14	HD13	I/O	3-state
15	HD01	I/O	3-state	16	HD14	I/O	3-state
17	HD00	I/O	3-state	18	HD15	I/O	3-state
19	GND			(20)	Key		
21	DMARQ	0	3-state	22	GND		
23	—HIOW	I	TTL	24	GND		
25	—HIOR	I	TTL	26	GND		
27	HIORDY	0	OC	28	CSEL	I	TTL
29	—DMACK	I	TTL	30	GND		
31	HIRQ	0	3-state	32	—HIOCS16	0	OC
33	HA01	I	TTL	34	—PDIAG	I/O	OC
35	HA00	I	TTL	36	HA02	I	TTL
37	—HCS0	I	TTL	38	—HCS1	I	TTL
39	—DASP	I/O	OC	40	GND		

Figure 16. Table of Signals

Notes:

1. "O" designates an output from the Drive.
2. "I" designates an input to the Drive.
3. "I/O" designates an input/output common.
4. "OC" designates Open-Collector or Open-Drain output.

6.1.3 Signal Description

- HD00-HD15** 16-bit bi-directional data bus between the host and the drive. The lower 8 lines, HD00-07, are used for Register and ECC access. All 16 lines, HD00-15, are used for data transfer. These are Three-State lines that have a 24 mA current sink capability.
- HA00-HA02** Address used to select the individual register in the drive.
- HCS0** Chip select signal generated from the Host address bus. When active, one of the Command Block Registers (Data, Error{Features when written}, Sector Count, Sector Number, Cylinder Low, Cylinder High, Drive/Head and Status{Command when written} register) can be selected.
(See Figure 21 on page 28.)
- HCS1** Chip select signal generated from the Host address bus. When active, one of the Control Block Registers (Alternate Status{Device Control when written} and Drive Address register) can be selected.
(See Figure 21 on page 28.)
- HRESET** This line is used to reset the drive. It shall be kept at a Low logic state during power up and kept High thereafter for normal operation.
- HIOW** The rising edge clocks data from the host data bus to a register or data register of the drive.
- HIOR** When low, this signal enables data from a register or data register of the drive onto data bus. The data on the bus shall be latched on the rising edge of -HIOR.
- HIRQ** Interrupt is enabled only when the drive is selected, and the host activates the -IEN bit in the Device Control Reg. Otherwise, this signal is in high impedance state regardless of the state of the IRQ bit. The interrupt is set when the IRQ bit is set by the drive CPU. IRQ is reset to zero by a host read of the status register or a write to the Command Reg. This signal is a 3-State line with 24 mA sink capability.
- IORDY** Indication to host that the drive is ready to complete current I/O cycle. This line is driven low at the falling edge of -HIOR or -HIOW, when the drive needs some additional WAIT cycle(s) to extend PIO cycle. This line can be connected to host IORDY signal in order to insert WAIT state(s) in the host PIO cycle. This is an Open-Drain output with 24 mA sink capability.
- CSEL** This signal is monitored to determine the drive address, Master or Slave, when the jumper on the interface connector is at Position-3. (Refer to Figure 23 on page 30 for jumper position.)
When CSEL is ground or at a low level, the drive works as a Master. If CSEL is open or a high level, the drive works as a Slave.
The signal level of CSEL to one drive should be different from the signal level to another drive on the same AT interface cable, to avoid master-master or slave-slave configurations. Signal level of CSEL should be constant while the drives are on the AT interface.
- HIOCS16** Indication to the host that 16-bit wide data register has been addressed and that the drive is prepared to send or receive a 16-bit wide data word. This signal is an Open-Drain output with 24 mA sink capability and an external resistor is needed to pull this line to 5 Volt.
- DASP** This is a time-multiplexed signal which indicates that a drive is active, or that drive 1 is present. This signal is driven by an Open Collector driver and internally pulled-up to 5 Volt through 10Kohm resistor.
During Power-On initialization or after -RESET is negated, -DASP shall be asserted by Drive 1 within 400 msec to indicate that drive 1 is present. Drive 0 shall allow up to

450msec for drive 1 to assert -DASP. If drive 1 is not present, drive 0 may assert -DASP to drive a LED indicator.

-DASP shall be negated following acceptance of the first valid command by drive 1 or after 31 seconds, whichever comes first.

Anytime after negation of -DASP, either drive may assert -DASP to indicate that a drive is active.

When write cache is enabled, drive asserts -DASP until completion of actual disk write operation.

-PDIAG

This signal shall be asserted by drive 1 to indicate to drive 0 that it has completed diagnostics. This line is pulled-up to 5 Volt in the drive through a 10Kohm resistor.

Following a Power On Reset, software reset or -HRESET, drive 1 shall negate -PDIAG within 1 msec (to indicate to drive 0 that it is busy). Drive 1 shall then assert -PDIAG within 30 seconds to indicate that it is no longer busy, and is able to provide status. After the assertion of -PDIAG, drive 1 may be unable to accept commands until it has finished its reset procedure and is ready (DRDY=1).

Following the receipt of a valid Execute Drive Diagnostics command, drive 1 shall negate -PDIAG within 1 msec to indicate to drive 0 that it is busy and has not yet passed its drive diagnostics. If drive 1 is present then drive 0 shall wait for up to 5 seconds from the receipt of a valid Execute Drive Diagnostics command for drive 1 to assert -PDIAG. Drive 1 should clear BSY before asserting -PDIAG, as -PDIAG is used to indicate that drive 1 has passed its diagnostics and is ready to post status.

If -DASP was not asserted by drive 1 during reset initialization, drive 0 shall post its own status immediately after it completes diagnostics, and clear the drive 1 Status register to 00h. Drive 0 may be unable to accept commands until it has finished its reset procedure and is ready (DRDY=1).

KEY

Pin position 20 has no connection pin. It is recommended to key or blank the respective position of the cable connector in order to avoid wrong insertion by mistake.

-DMACK

This signal shall be used by the host in response to DMARQ to either acknowledge that data has been accepted, or that data is available.

DMARQ

This signal, used for DMA data transfers between host and drive, shall be asserted by the drive when it is ready to transfer data to or from the host. The direction of data transfer is controlled by -HIOR and -HIOW. This signal is used on a handshake manner with -DMACK. This signal is a 3-state line with 24mA sink capability and internally pulled-down to GND through 10KOhm resistor.

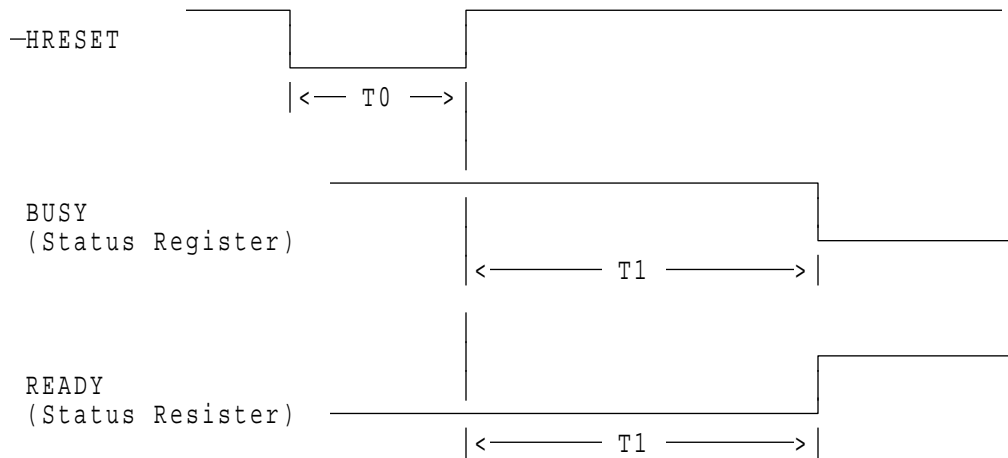
6.1.4 Interface Logic Signal Levels

The interface logic signal have the following electrical specifications:

Inputs :	Input High Voltage	—	2.0 V min.
	Input Low Voltage	—	0.8 V max.
Outputs :	Output High Voltage	—	2.4 V min.
	Output Low Voltage	—	0.5 V max.

6.1.5 Reset timings

Reset timings of the drive are shown below.

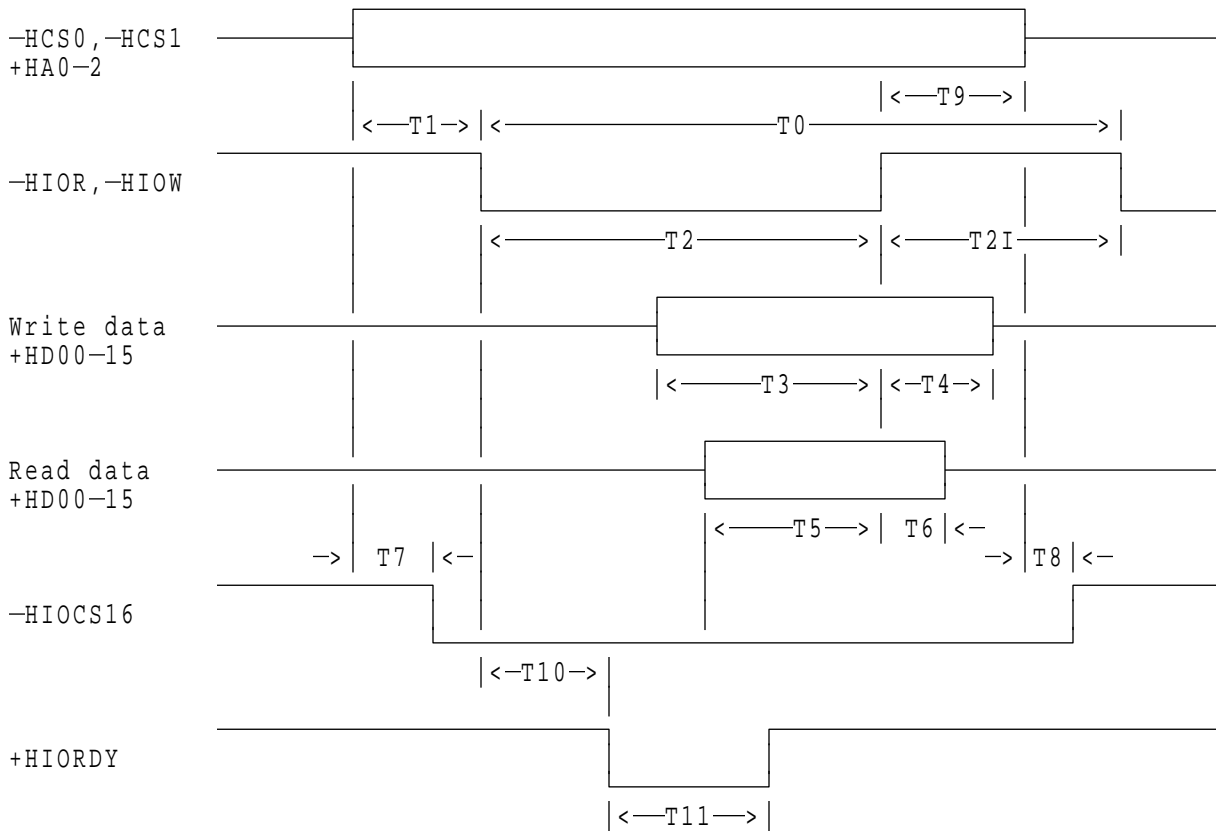


	PARAMETER DESCRIPTION	Min (usec)	Typ (sec)	Max (sec)
T0	-HRESET low width	25	—	—
T1	-HRESET high to Not BUSY	—	6	18

Figure 17. System Reset timings

6.1.6 PIO Timings

The PIO cycle timings meet Mode 4 of the ATA-2 description.



	PARAMETER DESCRIPTION	MIN (nsec)	MAX (nsec)	Note
T0	Cycle time	120	—	
T1	-HCS0-1, +HA00-02 valid to -HIOR, -HIOW active	25	—	
T2	-HIOR, -HIOW pulse width	70	—	
T2I	-HIOR, -HIOW recovery	25	—	
T3	+HD00-15 setup to -HIOW high	20	—	
T4	-HIOW high to +HD00-15 hold	10	—	
T5	+HD00-15 setup to -HIOW high	20	—	
T6	-HIOW high to +HD00-15 hold	5	—	
T7	-HCS0-1, +HA00-02 valid to -HIOCS16 assertion	—	30	
T8	-HCS0-1, +HA00-02 invalid to -HIOCS16 negation	—	30	
T9	-HIOR, -HIOW high to -HCS0-1, +HA00-02 hold	10	—	
T10	-HIOR, -HIOW low to +HIORDY low	—	35	
T11	+HIORDY pulse width	—	1250	

Figure 18. PIO cycle timings

6.1.6.1 Write DRQ Interval Time

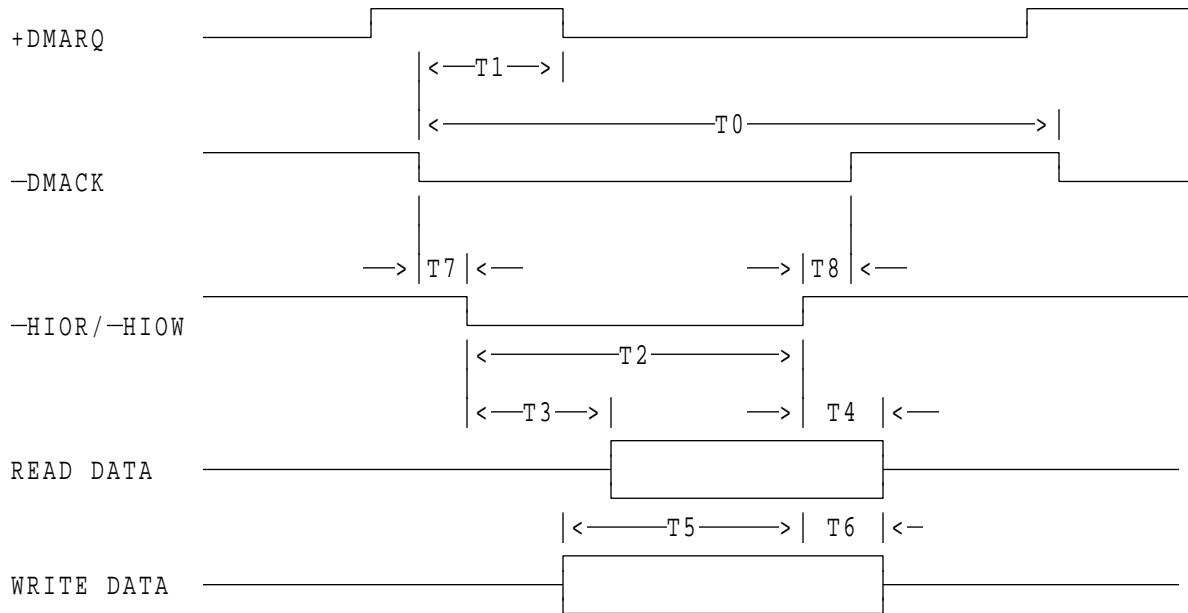
For write sectors and write multiple operations, 15usec is inserted from the end of negation of the DRQ bit until setting of the next DRQ bit.

6.1.6.2 Read DRQ Interval Time

For read sectors and read multiple operations, the interval from the end of negation of the DRQ bit until setting of the next DRQ bit is 15usec.

6.1.7 DMA Timings (Single Word)

The Single Word DMA timing meets Mode 2 of the ATA-2 description.

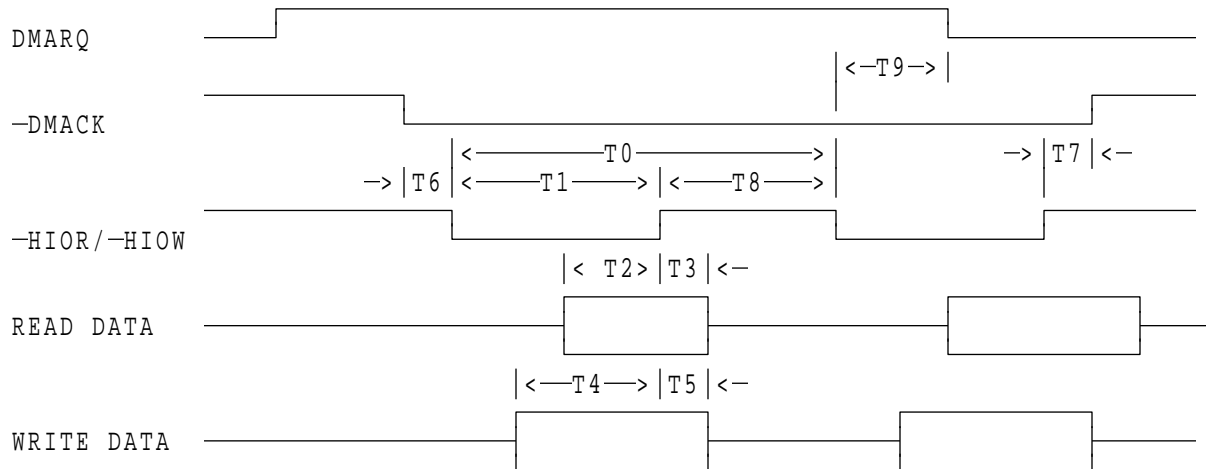


	PARAMETER DESCRIPTION	MIN (nsec)	MAX (nsec)	Note
T0	Cycle time	240	—	
T1	-DMA active to +DMARQ inactive	—	80	
T2	-HIOR, -HIOW pulse width	120	—	
T3	-HIOR data access	—	60	
T4	-HIOR data hold	5	—	
T5	-HIOW data setup	35	—	
T6	-HIOW data hold	20	—	
T7	-DMACK to -HIOR/-HIOW setup	0	—	
T8	-HIOR/-HIOW to -DMACK hold	0	—	

Figure 19. DMA (Single Word) cycle timings

6.1.8 DMA Timings (Multiword)

The Multiword DMA timing meets Mode 2 of the ATA-2 description.



	PARAMETER DESCRIPTION	MIN (nsec)	MAX (nsec)	Note
T0	Cycle time	120	—	
T1	-HIOR, -HIOW pulse width	70	—	
T2	-HIOR data setup	20	—	
T3	-HIOR data hold	5	—	
T4	-HIOW data setup	20	—	
T5	-HIOW data hold	10	—	
T6	-DMACK to -HIOR/-HIOW setup	0	—	
T7	-HIOR/-HIOW to -DMACK hold	5	—	
T8	-HIOR/-HIOW negated pulse width	25	—	
T9	-HIOR/-HIOW to -DMARQ delay	—	35	

Figure 20. DMA (Multi Word) cycle timings

6.1.9 Addressing of drive Registers

The host addresses the drive through a set of registers called a Task File. These registers are mapped into the host's I/O space. Two chip select lines (-HCS0 and -HCS1) and three address lines (HA00-02) are used to select one of these registers, while a -HIOR or -HIOW is provided at the specified time.

The -HCS0 is used to address Command Block registers, while the -HCS1 is used to address Control Block registers.

The following table shows the I/O address map.

Addr.	-CS0	-CS1	HA2	HA1	HA0	-IOR = 0 (Read)	-IOW = 0 (Write)
Command Block Registers							
1F0	0	1	0	0	0	Data Reg.	Data Reg.
1F1	0	1	0	0	1	Error Reg.	Features Reg.
1F2	0	1	0	1	0	Sector count Reg.	Sector count Reg.
1F3	0	1	0	1	1	Sector number Reg.	Sector number Reg.
1F4	0	1	1	0	0	Cylinder low Reg.	Cylinder low Reg.
1F5	0	1	1	0	1	Cylinder high Reg.	Cylinder high Reg.
1F6	0	1	1	1	0	Drive/Head Reg.	Drive/Head Reg.
1F7	0	1	1	1	1	Status Reg.	Command Reg.
Control Block Registers							
3F6	1	0	1	1	0	Alt. Status Reg.	Device control Reg
3F7	1	0	1	1	1	Drive address Reg.	—

Figure 21. Register Address

Note: "Addr." field is shown just as an example.

During DMA operation (from writing to the command register until an interrupt), all registers are not accessible.

For example, the host is not supposed to read status register contents before interrupt (the value is invalid).

6.1.10 Cabling

The maximum cable length from the host system to the HDD plus circuit pattern length in the host system shall not exceed 18 inches.

For higher data transfer application (>8.3MB/sec), the cable length should be shorter than 18 inches since data transfer characteristics depends on the driver circuits of the system and hard drive, and/or cabling.

6.1.11 Jumper Settings

The 7 positions jumper block shown below is to select Master or Slave, Cable Selection and Write Cache.

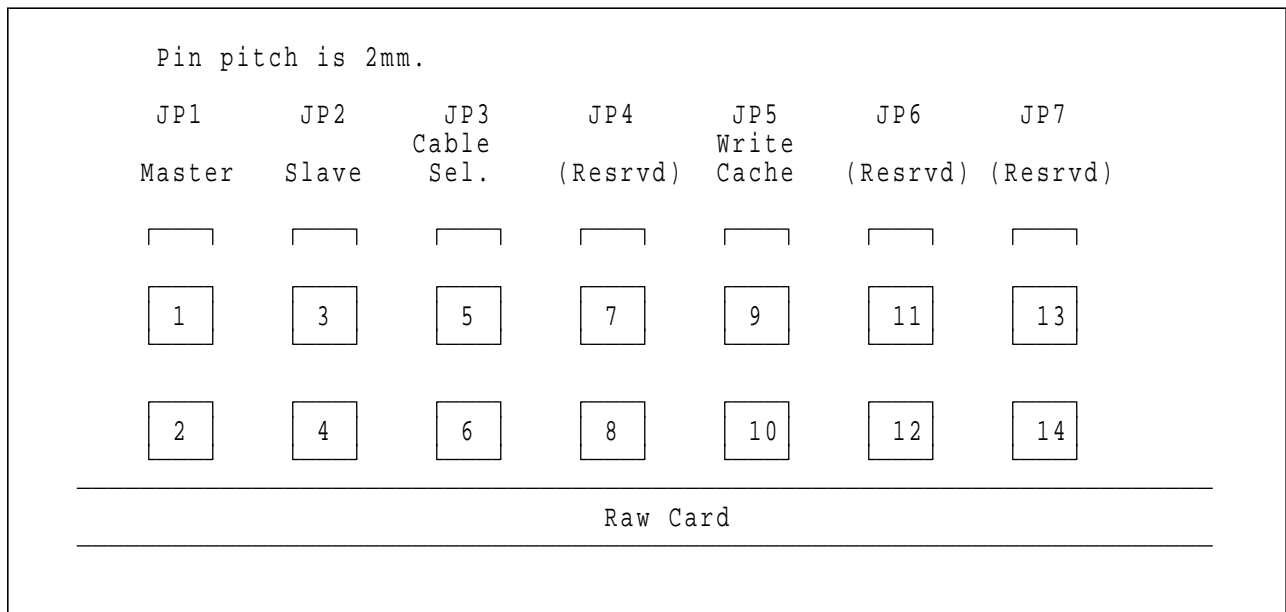


Figure 22. Jumper Pins

Notes:

1. The jumper positions of JP1, 2, and 3 should not be selected concurrently.
2. JP1 is the position for Master, JP2 is for Slave, and JP3 is for Cable Selection mode.
3. To enable the CSEL mode (cable selection mode), the JP3 jumper must be installed. In the CSEL mode, the drive address is determined as follows:
 - When CSEL is grounded or at a low level, the drive address is 0 (Master).
 - When CSEL is open or at a high level, the drive address is 1 (Slave).
4. When JP5 jumper is installed, write cache function is disabled.

6.1.11.1 The Pin Assignment

Figure 23. Jumper Pin Assignment				
JP#	Pin #	Status	Description	Signal Name
1	1	-	GND	
	2	In	-Device Address Select Line	-C/+D
2	3	-	NC (Slave position)	
	4	-	NC	
3	5	In	Cable Selection (28 PIN)	
	6	In	-Device Address Select Line	-C/+D
4	7	-	GND	
	8	-	(Reserved)	
5	9	-	GND	
	10	-	+Write Cache ON (If Open)	
6	11	-	GND	
	12	-	(Reserved)	
7	13	-	GND	
	14	-	(Reserved)	

6.1.11.2 Shipping Default Condition

The default shipping conditions are, device ID set of Master, write cache on and auto reallocation on.

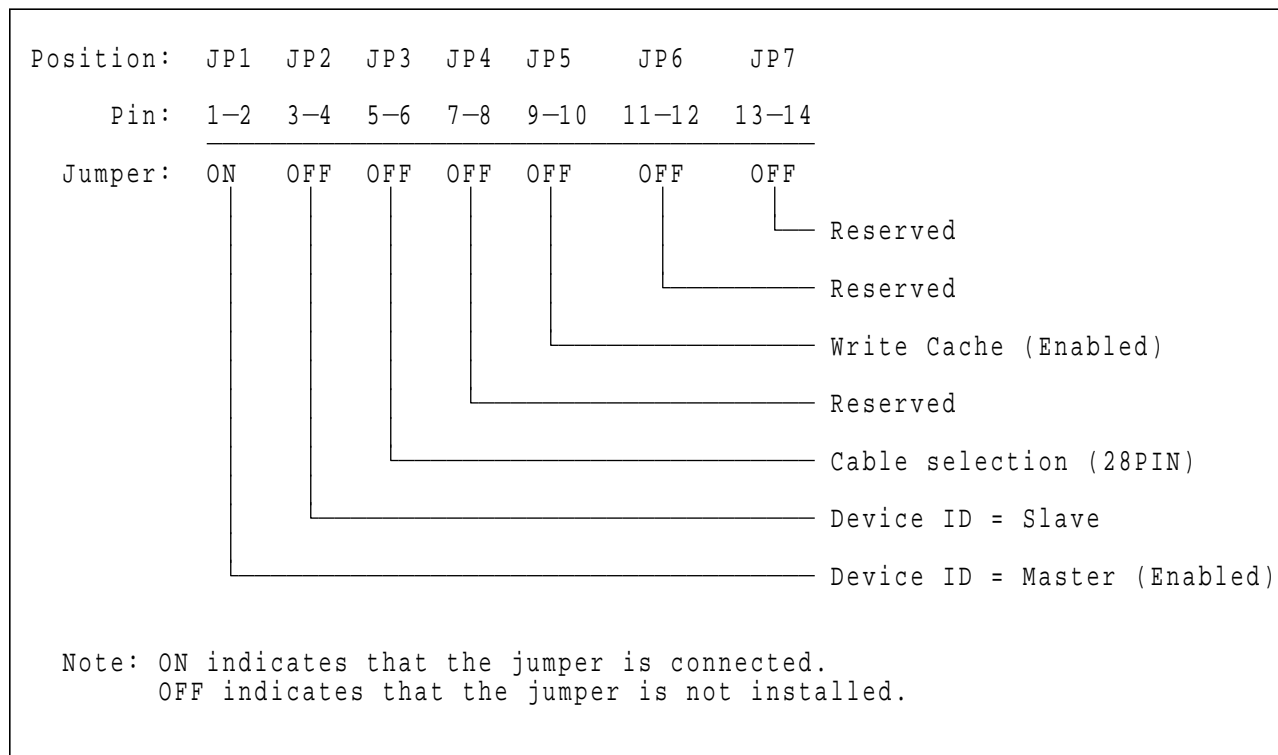


Figure 24. Default Jumper Setting

6.1.11.3 Mechanical Outline

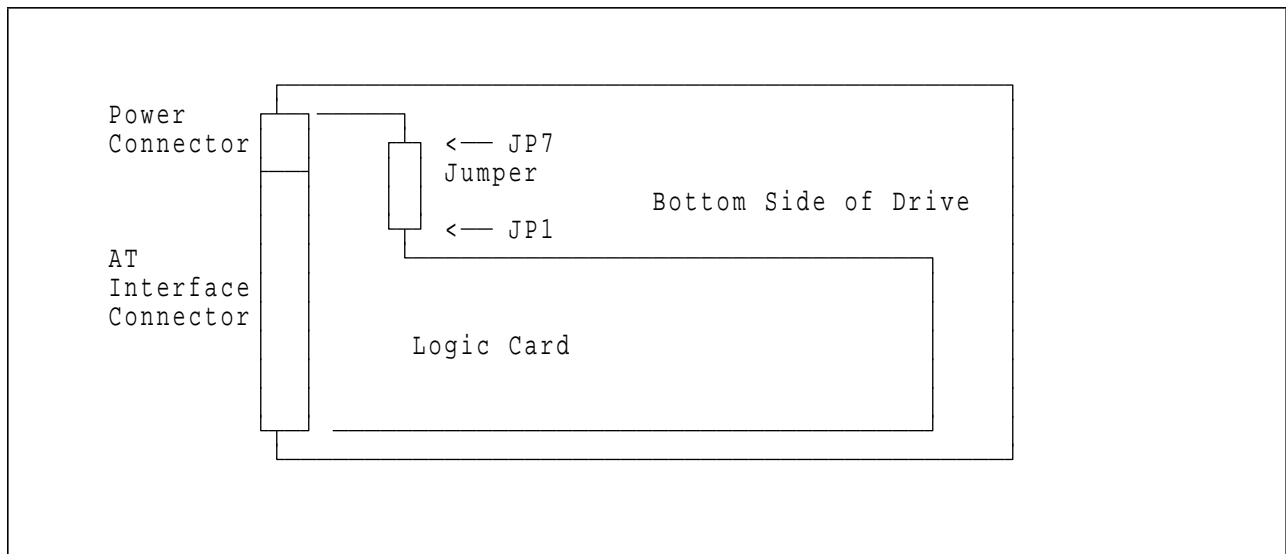


Figure 25. Mechanical Outline

7.0 Specification

7.1 Environment

7.1.1 Temperature and Humidity

Figure 26. Environmental Condition	
Operating Conditions	
Temperature	5 to 55[°C] (See note)
Relative Humidity	8 to 90 [% RH] non-condensing
Maximum Wet Bulb Temperature	29.4[°C] non-condensing
Maximum Temperature Gradient	15[°C / Hour]
Altitude	- 300 to 3048 [m]
Non-Operating Conditions	
Temperature	- 40 to 65[°C]
Relative Humidity	5 to 95 [% RH] non-condensing
Maximum Wet Bulb Temperature	40[°C] non-condensing
Maximum Temperature Gradient	20[°C / Hour]
Altitude	- 300 to 12,000 [m]
Note: The system has to provide sufficient ventilation to maintain a surface temperature below 60[°C] at the center of the top cover of the drive. Non-operating condition should not continue beyond one year.	

7.2 DC Power Requirements

Connection to the product should be made in isolated secondary circuits (SELV). The following voltage specification is applied at the power connector of the drive. Damage to the file electronics may result if the power supply cable is connected or disconnected while power is being applied to the file (No hot plug/unplug is allowed). There is no special power on/off sequencing required.

Figure 27. Input Voltage		
	During run and spin up	Absolute max voltage
+ 5 Volts Supply	5V +/- 5%	7V
+12 Volts Supply	12V +10% , - 8%	15V

Figure 28. Power Supply Current (with the SCSI termination power enabled)					
(All values in Amps.)	+5Volts		+12Volts		Total (W)
	Pop Mean	Std.Dev	Pop Mean	Std.Dev	
Idle Average	0.32	0.02	0.17	0.02	3.6
Idle ripple (peak-to-peak)	0.15	0.02	0.20	0.03	
Seek peak (*1)	0.50	0.04	0.55	0.13	
Seek average (*1)	0.40	0.02	0.37	0.02	6.4
Start up (max)	0.55	0.04	1.20	0.05	
RND R/W peak (*2)	0.60	0.02	0.60	0.16	
RND R/W average (*2)	0.45	0.02	0.28	0.02	5.6
Standby/Sleep average	0.15	0.01	0.02	0.01	1.0

Notes:

1. Random Seeks at 100% duty cycle.
2. Seek Duty = 30%, W/R Duty = 45%, Idle Duty = 25%.

Figure 29. Power Supply Generated Ripple as seen at file power connector		
	Maximum	Notes
+5 V DC	100 [mV pp]	0-10 [MHz]
+12 V DC	150 [mV pp]	0-10 [MHz]

During file start up and seeking, 12 volt ripple is generated by the file (referred to as dynamic loading). If several files have their power daisy chained together then the power supply ripple plus other file's dynamic loading must remain within the regulation tolerance of +10/-8%. A common supply with separate power leads to each file is a more desirable method of power distribution.

To prevent external electrical noise from interfering with the file's performance, the file must be held by four screws in a user system frame which has no electrical level difference at the four screws position, and has less than +/-300 millivolts peak to peak level difference to the file power connector ground.

7.3 Reliability

7.3.1 Cable Noise Interference

To avoid any degradation of performance throughput or error when the interface cable is routed on top or comes in contact with the HDA assembly, the drive must be grounded electrically to the system frame by four screws. The common mode noise or voltage level difference between the system frame and power cable ground or AT interface cable ground should be in the allowable level specified in the power requirement section.

7.3.2 Contact Start Stop(CSS)

The drive is designed to withstand a minimum of 40,000 contact start/stop cycle under 40 °C environment.

7.3.3 Preventive Maintenance

None.

7.3.4 Data Reliability

- Probability of not recovering data 1 in 10¹³ bits read
- ECC implementation

A Reed Solomon Error Code of degree-8 with non-interleaved is used to cover the data field. The ECC polynomial is derived from

$$g(X) = (X + 1)(X + A)(X + A^2) \dots (X + A^7)$$

On-The-Fly correction implemented in the file covers four or less symbols of error in one sector. (One symbol is 10 bits.)

7.3.5 Seek/ID Mis-compare Errors

A non-recoverable seek/ID mis-compare error is defined as a seek operation that cannot be corrected by fixed disk error recovery procedure. Seek errors occurring for field format operations are considered to be non-recoverable.

No drive has more than one non-recoverable seek/ID mis-compare error per 5 million seek operations (1 in 5×10^6) when operated at the full range of voltage and environmental conditions.

Non-recoverable seek/ID mis-compare errors indicate a defective drive.

7.3.6 Equipment Errors

A recoverable equipment error is any error other than a seek/ID mis-compare error or read error that is detected and corrected by the drive error recovery procedure. Examples are Write Fault, Drive Not Ready and internal drive errors.

No drive has more than one recoverable equipment error per 10^8 reads, 10^6 writes or 10^6 seeks operations when operated at the full range of voltage and environmental conditions.

Non-recoverable equipment errors indicate a defective drive.

7.4 Mechanical Specifications

7.4.1 Outline

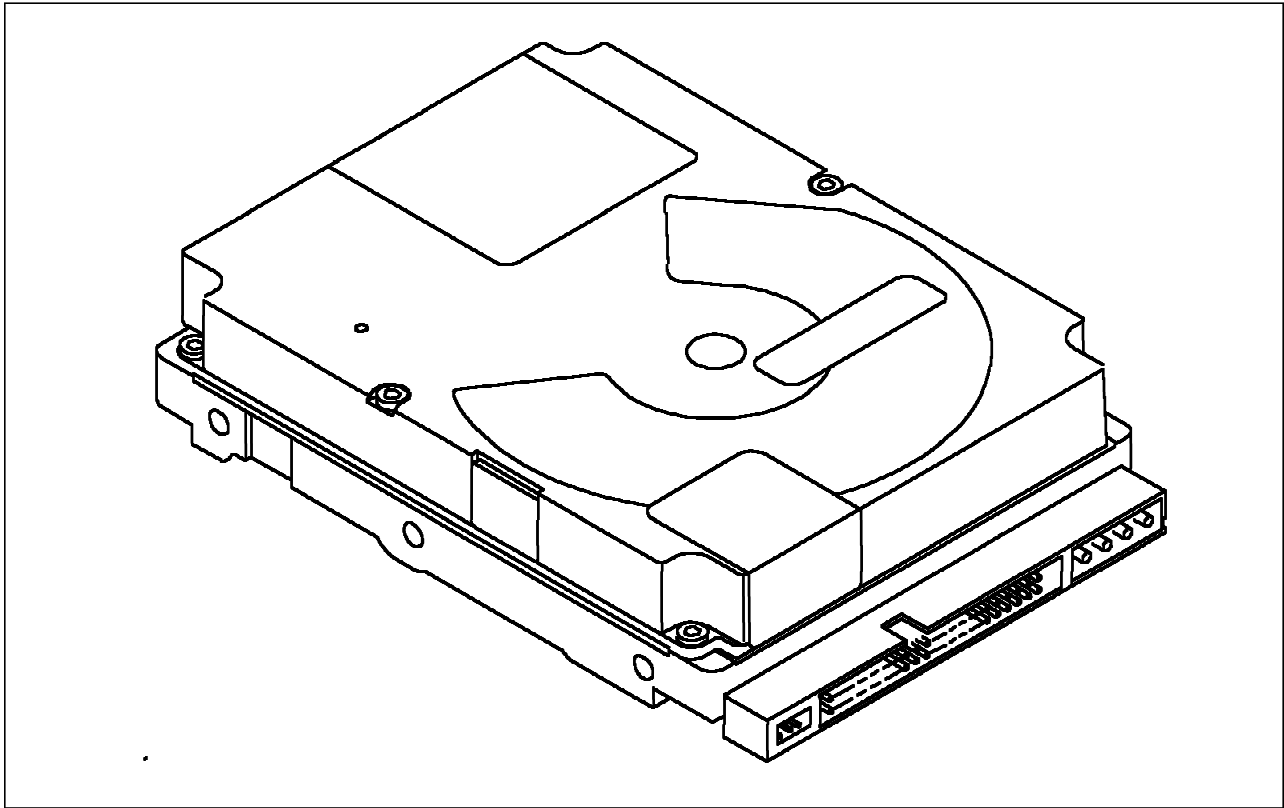


Figure 30. Outline of DJAA-31270/31700

7.4.2 Mechanical Dimensions and Weight

The following chart describes the dimensions for the 3.5" hard disk drive form factor.

	DJAA-31270/31700
Height (mm)	25.4 ± 0.4
Width (mm)	101.6 ± 0.4
Length (mm)	146.0 ± 0.6
Weight (gram)	530 Max

Figure 31. Physical Dimension and Weight

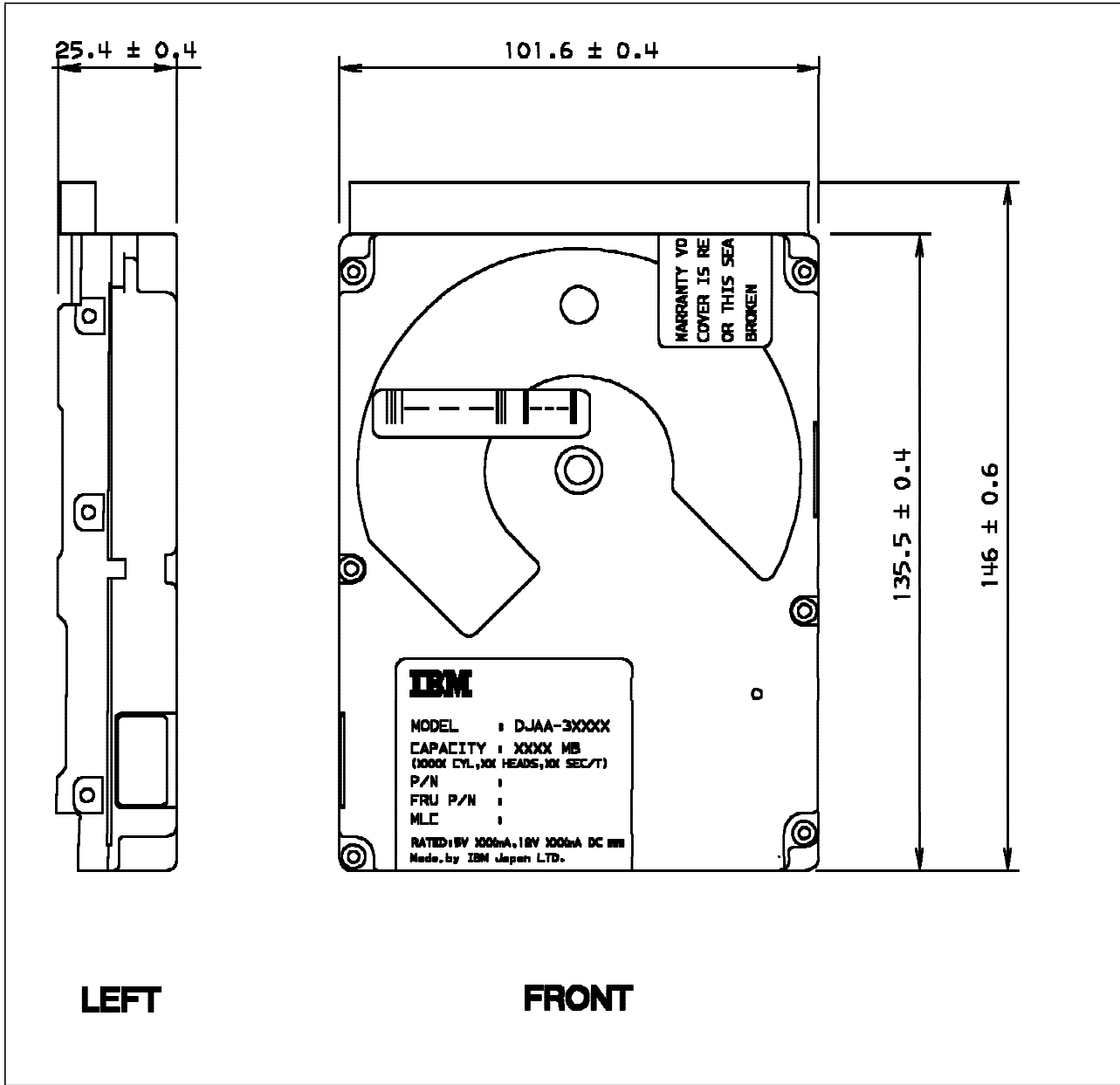


Figure 32. Mechanical Dimension

7.4.3 Connector Locations

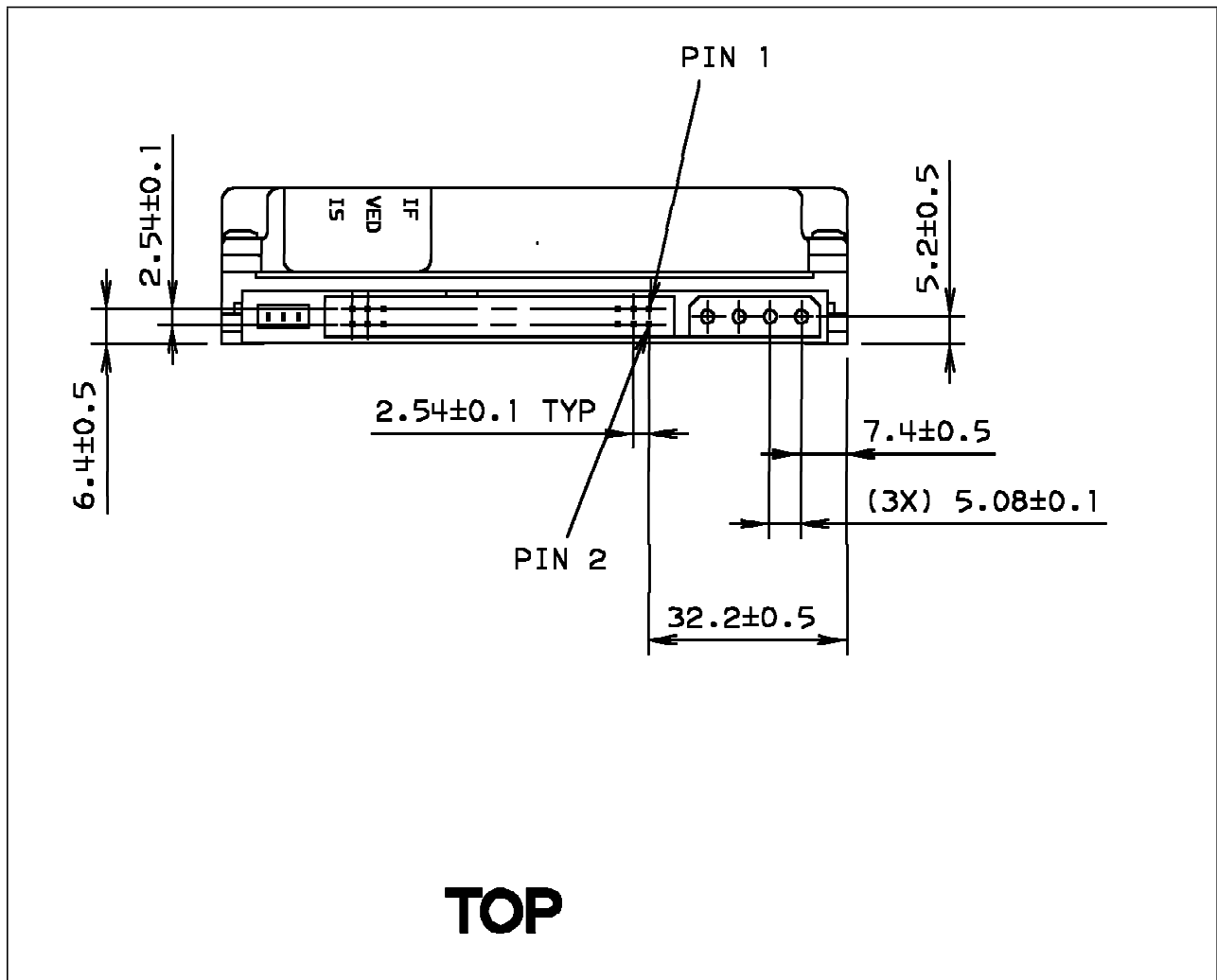


Figure 33. Connector Locations

7.4.4 Hole Locations

The Figure 34 on page 40 shows the outline of DJAA-31270/31700 which includes the hole locations.

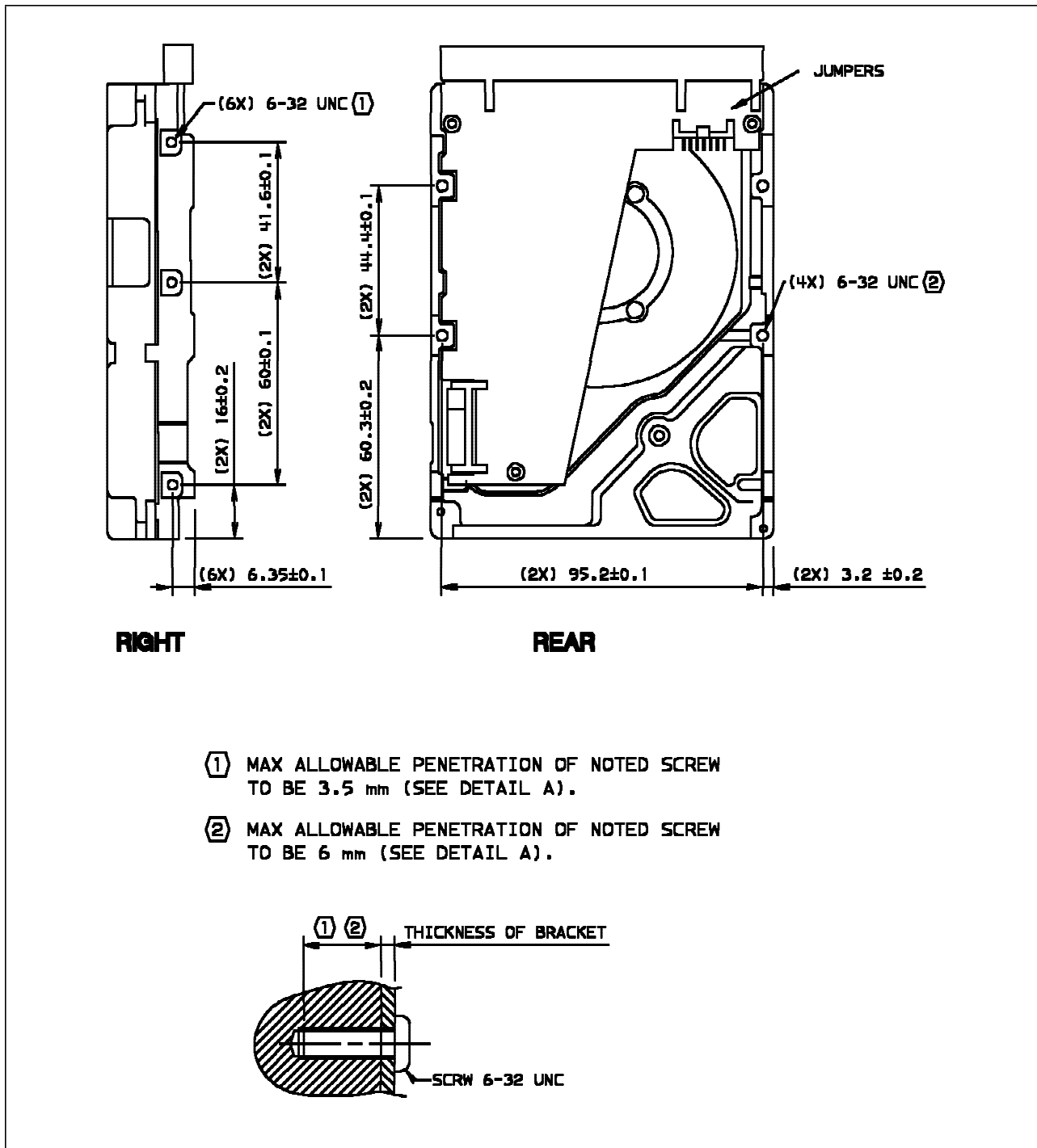


Figure 34. Mounting Positions and the Tappings

7.4.5 Mounting Orientation

The drive will operate in all axes (6 directions). The drive will operate within the specified error rates when tilted ± 5 degree from these positions.

Performance and error rate will stay within specification limits if the drive is operated in the other permissible orientations from which it was formatted. Thus a drive formatted in a horizontal orientation will be able to run vertically and vice versa.

The recommended mounting **screw torque** is **0.6 - 1.0** [Nm] (6 - 10 [Kgf.cm]).

The recommended mounting screw depth is 6 [mm] Max for bottom and 3.5 [mm] Max for horizontal mounting.

The system is responsible for mounting the drive securely enough to prevent from excessive motion or vibration of the drive at seek operation or spindle rotation, using appropriate screws or equivalent mounting hardware.

Vibration test and shock test are to be conducted by mounting the drive to the table using bottom four screws.

7.4.6 Shipping Zone and Lock

A "shipping" (or "landing") zone on the disk, not on the data area of the disk, is provided to protect the disk data during shipping, movement, or storage. Upon power down, a head locking mechanism will secure the heads in this zone. See Non-Operating Shock section for additional details.

7.5 Vibration and Shock

All vibration and shock measurements in this section are made with the drive that has no mounting attachments for the systems. The input power for the measurements is applied to the normal drive mounting points.

7.5.1 Operating Vibration

7.5.1.1 Random Vibration

The drive operates with no unrecoverable errors while being subjected to the following vibration levels.

The measurements are carried out during 30 minutes of random vibration using the power spectral density (PSD) levels specified in IBM standards as V5L. The vibration test level for V5L is 0.67G (RMS).

Figure 35. Random Vibration PSD Profile Breakpoints (Operating)									
Hz	Random Vibration PSD Profile Breakpoints (Operating)								
[Hz]	5	17	45	48	62	65	150	200	500
$\times 10^{-3}$ [G ² /Hz]	0.02	1.1	1.1	8.0	8.0	1.0	1.0	0.5	0.5

Note: The specified levels are measured at the mounting points.

7.5.1.2 Swept Sine Vibration

The hard disk drive will meet the criteria shown below while operating in respective conditions.

No errors 0.5 G 0-peak, 5-300-5 Hz sine wave, 0.5 oct/min sweep rate
with 3 minutes dwells at 2 major resonances

No data loss 1 G 0-peak, 5-300-5 Hz sine wave, 0.5 oct/min sweep rate
with 3 minutes dwells at 2 major resonances

7.5.2 Non-Operating Vibrations

The drive does not sustain permanent damage or loss of recorded data after being subjected to the environment described below.

7.5.2.1 Random Vibration

The test consists of a random vibration applied for each of three mutually perpendicular axes with the time duration of 15 minutes per axis. The PSD levels for the test simulates the shipping and relocation environment which is shown below.

Figure 36. Random Vibration PSD Profile Breakpoints (Non-Operating)							
Hz	Random Vibration PSD Profile Breakpoints (Non-Operating)						
Hz	2	4	8	40	55	70	200
[G ² /Hz]	0.001	0.03	0.03	0.003	0.01	0.01	0.001

Overall RMS (Root Mean Square) level of vibration is 1.04G (RMS).

7.5.2.2 Swept Sine Vibration

- 2 G (Zero to peak), 5 to 500 to 5 Hz sine wave
- 0.5 oct/min sweep rate
- 3 minutes dwell at two major resonances

7.5.3 Operating Shock

The drive meets the following criteria while operating in respective conditions described below. The shock test consists of ten shocks inputs in each axis and direction for total of 60. There must be a delay between shock pulses, long enough to allow the drive to complete all necessary error recovery procedures.

No errors 5 G, 11 ms half-sine shock pulse

No data loss, seek errors or permanent damage
10 G, 11 ms half-sine shock pulse

No data loss or permanent damage
15 G, 5 ms half-sine shock pulse
30 G, 4 ms half-sine shock pulse

7.5.4 Non-Operating Shock

The drive will operate with no degradation of performance or permanent damage after subjected to shock pulses with the following characteristics.

7.5.4.1 Trapezoidal Shock Wave

- Approximate square (trapezoidal) pulse shape.
- Approximate rise and fall time of pulse = 1 ms.
- Averaged acceleration level = 50 G.
(Averaged response curve value during the time following the 1 ms rise time and before the 1 ms fall with a time "duration of 11 msec")
- Minimum velocity change = 4.23 meters/sec.

7.5.4.2 Sinusoidal Shock Wave

- Approximate half-sine pulse shape.
- Maximum acceleration level = 75G.
- Shock duration = 11 msec.

All shock input shall be applied in each direction of the drive's three mutually perpendicular axes. The heads are not displaced from the landing zone as a result of this test.

7.6 Acoustics

7.6.1 Sound Power Levels

The upper limit criteria of the octave sound power levels are given in Bels relative to 1 pico Watt and are shown in the following table with A-weighted levels.

Figure 37. Octave band sound power levels								
	Octave Band Center Frequency (Hz)							
Mode	125	250	500	1k	2k	4k	8k	LwAu
Idle	4.8	4.1	3.6	3.6	3.9	3.9	3.6	4.5
Operating	5.0	4.3	4.2	4.2	4.2	4.2	3.8	4.8

Background power levels of the acoustic test chamber for each octave band are to be recorded.

Sound power tests are to be conducted with the drive supported by spacers so that the lower surface of the drive be located at 25 +/- 3mm height from the chamber floor. No sound absorbing material shall be used.

The acoustical characteristics of the disk drive subsystem are measured under the following conditions.

Idle mode :

Power on, disks spinning, track following, unit ready to receive and respond to control line commands.

Operating mode :

Continuous random cylinder selection and seek operation of actuator with a dwell time at each cylinder. Seek rate for the drive can be calculated as shown below.

$$\text{Dwell time} = (0.5 + N) \times 60/\text{RPM}$$

$$\text{Seek rate} = 1/(\text{Average seek time} + \text{Dwell time})$$

Where N = number of maximum data surfaces (n=4 for &Model17000.)

7.6.2 Sound Power Acceptance Criteria

Statistical upper limit $(L_{W_{oct}})_{stat}$ is calculated with following formula.

$$(L_{W_{oct}})_{stat} = (L_{W_{oct}})_m + k \times (s_t)_{W_{oct}}$$

where:

$(L_{W_{oct}})_m$ is the mean value of the sound power level for a sample of N drives.

$(s_t)_{W_{oct}}$ is the total standard deviation for sound power level at each octave band.

$$(s_t)_{W_{oct}} = \text{SQRT}((s_R)_W^2 + (s_P)_{W_{oct}}^2)$$

$(s_R)_W$ is the standard deviation of reproducibility for sound power level.

Assume $(s_R)_W = 0.075$ B.

$(s_P)_{W_{oct}}$ is the standard deviation of the samples for sound power level at each octave band.

k is a coefficient determined by number of samples (N) as shown below.

N	3	4	5	6	7	8	9	10	11	12	13	14	15
k	3.19	2.74	2.74	2.49	2.33	2.22	2.13	2.07	2.01	1.97	1.93	1.90	1.87

The calculated left hand side of the criterion equation above is referred to as LWU and is rounded to the nearest 0.05 bel. The individual terms may be rounded to the nearest 0.01 bel before calculation.

7.7 Identification

7.7.1 Labels

The following labels are affixed to every disk drive .

1. A label containing IBM logo, IBM part number and the statement 'Made by IBM' or equivalent.
2. A label containing drive model number, date code, formatted capacity, place of manufacture, and UL/CSA/TUV logos.
3. A bar code label containing the drive serial number.

The labels may be integrated with other labels.

7.8 Electromagnetic Compatibility

The drive, when installed in a suitable enclosure and exercised with a random accessing routine at maximum data rate, shall meet the worldwide EMC requirements listed below.

IBM will provide technical support to assist users in complying with the EMC requirements.

- United States Federal Communications Commission (FCC) Rules and Regulations (Class B), Part 15.
- European Economic Community (EEC) directive number 76/889 related to the control of radio frequency interference and the Verband Deutscher Elektrotechniker (VDE) requirements of Germany (GOP).

7.9 Safety

7.9.1 Underwriters Lab(UL) Approval

DJAA-31270/31700 complies with UL 1950.

7.9.2 Canadian Standards Authority(CSA) Approval

DJAA-31270/31700 complies with CSA C22.2, #950-M89.

7.9.3 IEC Compliance

DJAA-31270/31700 complies with IEC 950.

7.9.4 German Safety Mark

DJAA-31270/31700 are approved by TUV on Test Requirement:

EN 60 950:1988/A1:1990/A2:1991.

7.9.5 Flammability

Printed Circuit boards used in this product are made of material with a UL recognized flammability rating of V-1 or better. The flammability rating is marked or etched on the board. All other parts not considered electrical components are made of material with a UL recognized flammability rating of V-1 or better except minor mechanical parts.

7.9.6 Secondary Circuit Protection

Fuses are provided in both 5V and 12V input of the hard disk drive for over current protection.

7.10 Packaging

Drives are shipped in ESD protective bags.

Part 2. ATA Interface Specification

8.0 Interface

The interface conforms to the Working Draft of Information technology ATA Attachment Interface with Extensions (ATA-2) dated on July-6-1994 with certain limitations shown below.

Automatic Power Down Sequence A hard reset will disable the automatic power down sequence.

Format Track A drive will not perform a physical format. Instead it will simply write a data pattern of all zeros to the sectors which have been specified by the Format Track command. Bad sectors which has been set by format track command will be cleared by write command (i.e. write sectors, write multiple, write DMA, write long).

Format Track Interleave Factor The drive only supports an interleave factor of 1:1, and may ignore the sector number in format table without returning an error.

Write Long Write long command should be executed for the same sector after read long command execution. Otherwise, unexpected ECC correctable error may occur. Because of the limitation of the emulation technique to support 4-byte ECC mode which is implemented in the drive.

Seek Overlap The drive will wait for the seek to complete before interrupting the host. Therefore, no seek overlap can occur. This will be transparent to the host except that performance may be degraded in certain environments where the host could perform other work while waiting for seek complete, such as multitasking operating systems.

Sleep Mode During Sleep mode the drive will be activated by any command, including, but not limited to, a soft reset.

Drive/Head Register Bits 5 and 7 of Drive/Head Register are not written to 0 (These 2 bits are always read as '1' even after host writes to '0').

Write Cache Jumper See Figure 38 on page 52 for the relationship between (+)write cache jumper and set features command. (+)Write cache jumper is checked during the initial POR check.

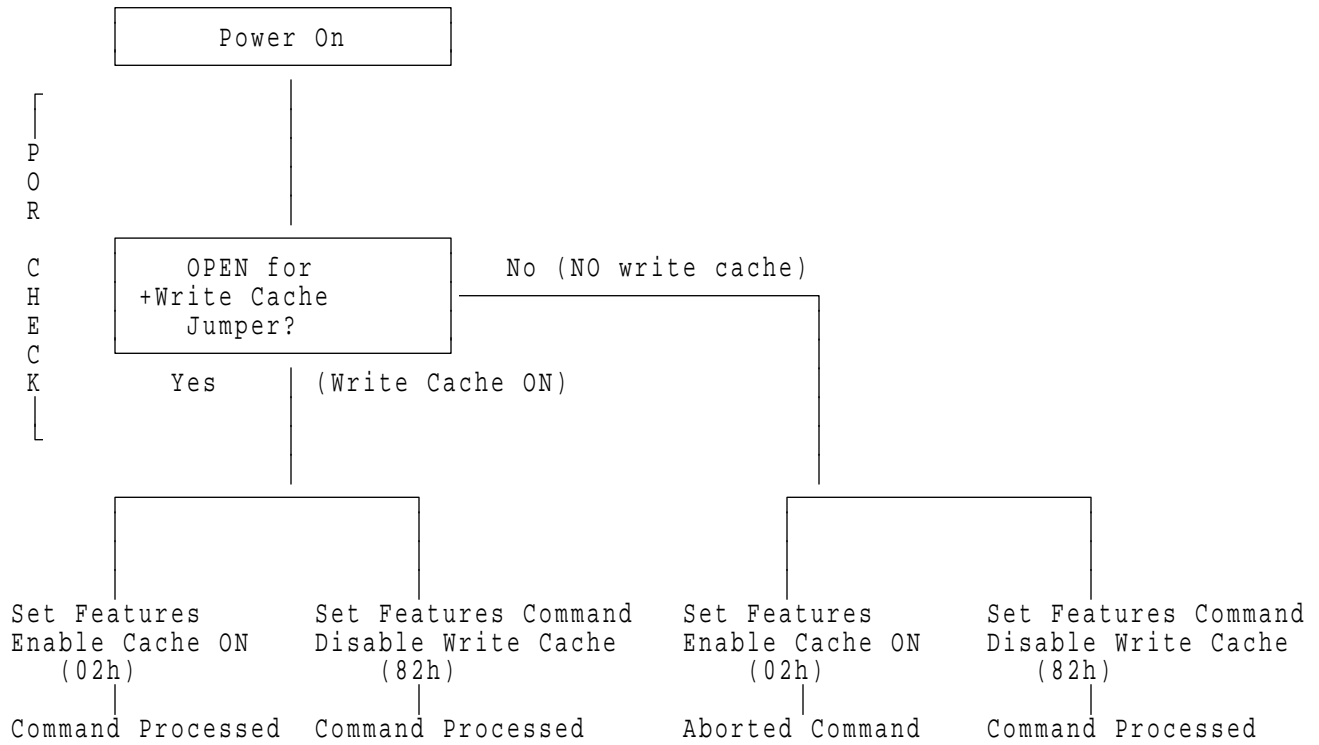


Figure 38. Relations Between Write Cache And Set Features Command

9.0 Vendor Specific Options

The drive conforms to the referenced specifications, with vendor specific options described below.

Seek Overlap

When a seek command is issued the drive will wait for the seek to complete before resetting the busy bit in the interface status register.

Sleep/Standby/Idle mode

When entering sleep, standby or Idle mode as a result of a command the busy bit in the status register will remain set until the transition to the new state is complete.

10.0 Registers

Addresses					Functions	
CS0-	CS1-	DA2	DA1	DA0	READ(DIOR-)	WRITE(DIOW-)
N	N	x	x	x	Data bus high imped*1	Not used
					Control block registers	
N	A	0	x	x	Data bus high imped	Not used
N	A	1	0	x	Data bus high imped	Not used
N	A	1	1	0	Alternate Status	Device Control
N	A	1	1	1	Drive Address	Not used
					Command block registers	
A	N	0	0	0	Data	Data
A	N	0	0	1	Error Register	Features
A	N	0	1	0	Sector Count	Sector Count
A	N	0	1	1	Sector Number	Sector Number
A	N	0	1	1	*2 LBA bits 0-7	*2 LBA bits 0-7
A	N	1	0	0	Cylinder Low	Cylinder Low
A	N	1	0	0	*2 LBA bits 8-15	*2 LBA bits 8-15
A	N	1	0	1	Cylinder High	Cylinder High
A	N	1	0	1	*2 LBA bits 16-23	*2 LBA bits 16-23
A	N	1	1	0	Drive/Head	Drive/Head
A	N	1	1	0	*2 LBA bits 24-27	*2 LBA bits 24-27
A	N	1	1	1	Status	Command
A	A	x	x	x	Invalid address	Invalid address

*1 "imped" stands for "impedance".
 *2 Mapping of registers in LBA mode

Logic conventions : A = signal asserted
 N = signal negated
 x = does not matter which it is

Figure 39. Register Set

Communication to or from the drive is through an I/O Register that routes the input or output data to or from registers addressed by the signals from the host (CS0-, CS1-, DA2, DA1, DA0, DIOR- and DIOW-).

The Command Block Registers are used for sending commands to the drive or posting status from the drive.

The Control Block Registers are used for drive control and to post alternate status.

10.1 Alternate Status Register

Alternate Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR

Figure 40. Alternate Status Register

This register contains the same information as the Status Register. The only difference is that reading this register does not imply interrupt acknowledge or clear a pending interrupt. See 10.13, “Status Register” on page 59 for the definition of the bits in this register.

10.2 Command Register

This register contains the command code being sent to the drive. Command execution begins immediately after this register is written. The command set is shown in Figure 49 on page 69.

All other registers required for the command must be set up before writing the Command Register.

10.3 Cylinder High Register

This register contains the high order bits of the starting cylinder address for any disk access. At the end of the command, this register is updated to reflect the current cylinder number.

In LBA Mode this register contains Bits 16-23. At the end of the command, this register is updated to reflect the current LBA Bits 16-23.

The cylinder number may be from zero to the number of cylinders minus one.

10.4 Cylinder Low Register

This register contains the low order 8 bits of the starting cylinder address for any disk access. At the end of the command, this register is updated to reflect the current cylinder number.

In LBA Mode this register contains Bits 8-15. At the end of the command, this register is updated to reflect the current LBA Bits 8-15.

The cylinder number may be from zero to the number of cylinders minus one.

10.5 Data Register

This register is used to transfer data blocks between the device data buffer and the host. It is also the register through which sector information is transferred on a Format Track command, and configuration information is transferred on an Identify Drive command.

All data transfers are 16 bits wide, except for ECC byte transfers, which are 8 bits wide. Data transfers are PIO only.

The register contains valid data only when DRQ=1 in the Status Register.

10.6 Device Control Register

Device Control Register							
7	6	5	4	3	2	1	0
—	—	—	—	1	SRST	-IEN	0

Figure 41. Device Control Register

Bit Definitions

- SRST (RST)** Software Reset. The drive is held reset when RST=1. Setting RST=0 re-enables the drive.
- The host must set RST=1 and wait for at least 5 microseconds before setting RST=0, to ensure that the drive recognizes the reset.
- IEN** Interrupt Enable. When IEN=0, and the drive is selected, drive interrupts to the host will be enabled. When IEN=1, or the drive is not selected, drive interrupts to the host will be disabled.

10.7 Drive Address Register

Drive Address Register							
7	6	5	4	3	2	1	0
HIZ	-WTG	-H3	-H2	-H1	-H0	-DS1	-DS0

Figure 42. Drive Address Register

This register contains the inverted drive select and head select addresses of the currently selected drive.

Bit Definitions

- HIZ** High Impedance. This bit is not driven and will always be in a high impedance state.
- WTG** -Write Gate. This bit is 0 when writing to the disk drive is in progress.
- H3,-H2,-H1,-H0** -Head Select. These four bits are the one's complement of the binary coded address of the currently selected head. -H0 is the least significant.

- DS1** -Drive Select 1. Drive select bit for drive 1, active low. DS1=0 when drive 1 (slave) is selected and active.
- DS0** -Drive Select 0. Drive select bit for drive 0, active low. DS0=0 when drive 0 (master) is selected and active.

10.8 Drive/Head Register

Drive/Head Register							
7	6	5	4	3	2	1	0
1	L	1	DRV	HS3	HS2	HS1	HS0

Figure 43. Drive/Head Register

This register contains the drive and head numbers.

Bit Definitions

- L** Binary encoded address mode select. When L=0, addressing is by CHS mode. When L=1, addressing is by LBA mode.
- DRV** Drive. When DRV=0, drive 0 (master) is selected. When DRV=1, drive 1 (slave) is selected.
- HS3,HS2,HS1,HS0** Head Select. These four bits indicate binary encoded address of the head. HS0 is the least significant bit. At command completion, these bits are updated to reflect the currently selected head.

The head number may be from zero to the number of heads minus one.

In LBA mode, HS3 through HS0 contain bits 24-27 of the LBA. At command completion, these bits are updated to reflect the current LBA bits 24-27.

10.9 Error Register

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDNF	0	ABRT	TK0NF	AMNF

Figure 44. Error Register

This register contains status from the last command executed by the drive, or a diagnostic code.

At the completion of any command except Execute Drive Diagnostic, the contents of this register are valid always even if ERR=0 in the Status Register.

Following a power on, a reset, or completion of an Execute Drive Diagnostic command, this register contains a diagnostic code. See Figure 48 on page 62 for the definition.

Bit Definitions

BBK	Bad Block. BBK=1 indicates a bad block mark was detected in the requested sector's ID field.
UNC	Uncorrectable Data Error. UNC=1 indicates an uncorrectable data error has been encountered.
IDNF (IDN)	ID Not Found. IDN=1 indicates the requested sector's ID field could not be found.
ABRT (ABT)	Aborted Command. ABT=1 indicates the requested command has been aborted due to a drive status error or an invalid parameter in an output register.
TK0NF (T0N)	Track 0 Not Found. T0N=1 indicates track 0 was not found during a Recalibrate command.
AMNF (AMN)	Address Mark Not Found. AMN=1 indicates the data address mark has not been found after finding the correct ID field for the requested sector.

10.10 Features Register

This register is command specific. This is used with the Set Features command.

10.11 Sector Count Register

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the drive. If the value in the register is set to 0, a count of 256 sectors is specified.

If the register is zero at command completion, the command was successful. If not successfully completed, the register contains the number of sectors which need to be transferred in order to complete the request.

The contents of the register are defined otherwise on some commands. These definitions are given in the command descriptions.

10.12 Sector Number Register

This register contains the starting sector number for any disk data access for the subsequent command. The sector number is from one to the maximum number of sectors per track.

In LBA mode, this register contains Bits 0-7. At the end of the command, this register is updated to reflect the current LBA Bits 0-7.

10.13 Status Register

Status Register							
7	6	5	4	3	2	1	0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

Figure 45. Status Register

This register contains the drive status. The contents of this register are updated whenever an error occurs and at the completion of each command.

If the host reads this register when an interrupt is pending, it is considered to be the interrupt acknowledge. Any pending interrupt is cleared whenever this register is read.

If BSY=1, no other bits in the register are valid.

Bit Definitions

BSY Busy. BSY=1 whenever the drive is accessing the registers. The host should not read or write any registers when BSY=1. If the host reads any register when BSY=1, the contents of the Status Register will be returned.

DRDY (RDY) Drive Ready. RDY=1 indicates that the drive is capable of responding to a command. RDY will be set to 0 during power on until the drive is ready to accept a command. If the drive detects an error while processing a command, RDY is set to 0 until the Status Register is read by the host, at which time RDY is set back to 1.

DWF Drive Write Fault. DWF=1 indicates that the drive has detected a write fault condition. DWF is set to 0 after the Status Register is read by the host.

DSC Drive Seek Complete. DSC=1 indicates that a seek has completed and the drive head is settled over a track. DSC is set to 0 by the drive just before a seek begins. When an error occurs, this bit is not changed until the Status Register is read by the host, at which time the bit again indicates the current seek complete status.

DRQ Data Request. DRQ=1 indicates that the drive is ready to transfer a word or byte of data between the host and the drive. The host should not write the Command register when DRQ=1.

CORR (COR) Corrected Data. COR=1 indicates that a correctable data error was encountered and the data has been corrected using the drive's ECC. The sector buffer contains the corrected data and multi-sector reads continue. The bit is set to 0 when a command is received.

During multi-sector reads, COR=1 only while DRQ=1 for the sector or sectors containing correctable errors.

During a multi-sector read verify operation, COR is set to 1 at the end of the operation if any of the verified sectors contained a correctable error.

IDX Index. IDX=1 once per revolution. Since IDX=1 only for a very short time during each revolution, the host may not see it set to 1 even if the host is reading the Status Register continuously. Therefore the host should not attempt to use IDX for timing purposes.

ERR Error. ERR=1 indicates that an error occurred during execution of the previous command. The Error Register should be read to determine the error type. The drive sets ERR=0 when the next command is received from the host.

11.0 Reset Response

There are three types of reset in ATA as follows:

Power On Reset (POR)

Hard Reset (Hardware Reset) RESET- signal is negated in ATA Bus.

Soft Reset (Software Reset) SRST bit is set in the Drive Control Register.

The actions of each reset is shown in Figure 46

	POR	hard reset	soft reset
Aborting Host interface	—	0	0
Aborting Drive operation	—	0	Note.1
Initialization of hardware	0	0	x
Internal diagnostics.	0	0	x
Spinning spindle	0	x	x
Initialization of registers (Note.2)	0	0	0
DASP handshake	0	0	x
PDIAG handshake	0	0	0
Reverting programmed parameters to default	0	0	Note.3
— Number of CHS			
(set by Initialize Drive Parameter)			
— Multiple mode			
— Write cache			
— Read look-ahead			
— ECC bytes			
Disable automatic power down	0	0	x
Power mode	Idle	Idle	Note.4

0 — execute
x — not execute

Figure 46. Reset Response Table

Note 1. Execute after the data in write cache has been written.

Note 2. Default value on POR is shown in Figure 47 on page 62.

Note 3. The Set Features command with Feature register = CCh enables the device to revert these parameters to the power on defaults.

Note 4. In the case of sleep mode, the drive goes to idle mode. In other case, the drive does not change current mode.

11.1.1 Register Initialization

Register	Default Value
Error	Diagnostic Code
Sector Count	01h
Sector Number	01h
Cylinder Low	00h
Cylinder High	00h
Drive/Head	A0h
Status	50h
Alternate Status	50h

Figure 47. Default Register Values

After power on, hard reset, or software reset, the register values are initialized as shown in Figure 47.

Code	Description
01h	No error detected
02h	Formatter device error
03h	Sector buffer error
04h	ECC circuitry error
05h	Controller microprocessor error
8xh	Slave drive failed

Figure 48. Diagnostic Codes

The meaning of the Error Register diagnostic codes resulting from power on, hard reset or the Execute Drive Diagnostic command are shown in Figure 48.

12.0 Command Protocol

The commands are grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined below.

For all commands, the host must first check if BSY=1, and should proceed no further unless and until BSY=0. For all commands except Execute Drive Diagnostics and Initialize Drive Parameters the host must also wait for RDY=1 before proceeding.

A device must maintain either BSY=1 or DRQ=1 at all times until the command is completed. The INTRQ signal is used by the device to signal most, but not all, times when the BSY bit is changed from 1 to 0 during command execution.

A command shall only be interrupted with a hardware or software reset. The result of writing to the Command register while BSY=1 or DRQ=1 is unpredictable and may result in data corruption. A command should only be interrupted by a reset at times when the host thinks there may be a problem, such as a device that is no longer responding.

Interrupts are cleared when the host reads the Status Register, issues a reset, or writes to the Command Register.

Figure 84 on page 117 shows the drive timeout values.

12.1 Data In Commands

These commands are:

- Execute S.M.A.R.T. Function (Read Attribute Values)
- Execute S.M.A.R.T. Function (Read Attribute Thresholds)
- Identify Drive
- Read Buffer
- Read Long
- Read Multiple
- Read Sectors

Execution includes the transfer of one or more 512 byte (>512 bytes on Read Long) sectors of data from the drive to the host.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Drive/Head Registers.
2. The host writes the command code to the Command Register.
3. For each sector (or block) of data to be transferred:
 - a. The drive sets BSY=1 and prepares for data transfer.
 - b. When a sector (or block) of data is available for transfer to the host, the drive sets BSY=0, sets DRQ=1, and interrupts the host.
 - c. In response to the interrupt, the host reads the Status Register.
 - d. The drive clears the interrupt in response to the Status Register being read.

- e. The host reads one sector (or block) of data via the Data Register.
 - f. The drive sets DRQ=0 after the sector (or block) has been transferred to the host.
4. For the Read Long command:
- a. The drive sets BSY=1 and prepares for data transfer.
 - b. When the sector of data is available for transfer to the host, the drive sets BSY=0, sets DRQ=1, and interrupts the host.
 - c. In response to the interrupt, the host reads the Status Register.
 - d. The drive clears the interrupt in response to the Status Register being read.
 - e. The host reads the sector of data via the Data Register.
 - f. The drive keeps DRQ=1 after the sector has been transferred to the host to indicate the ECC bytes are available for transfer to the host.
 - g. The host reads the ECC bytes via the Data Register.
 - h. The drive sets DRQ=0 after the ECC bytes have been transferred to the host.

The Read Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.

Note that the status data for a sector of data is available in the Status Register **before** the sector is transferred to the host.

If the drive detects an invalid parameter, then it will abort the command by setting BSY=0, ERR=1, ABT=1, and interrupting the host.

If an error occurs, the drive will set BSY=0, ERR=1, and DRQ=1. The drive will then store the error status in the Error Register, and interrupt the host. The registers will contain the location (CHS) of the sector in error.

If an Uncorrectable Data Error (UNC=1) occurs, the defective data will be transferred from the media to the sector buffer, and will be available to be transferred to the host, at the host's option. In case of Read Multiple command, the host should complete transfer the block which includes error from the sector buffer and terminate whatever kind of type of error occurred.

If an error occurs that is correctable by retries, the data will be corrected and the transfer will continue normally. There will be no indication to the host that any retry occurred.

All data transfers to the host through the Data Register are 16 bits, except for the ECC bytes, which are 8 bits.

12.2 Data Out Commands

These commands are:

- Format Track
- Write Buffer
- Write Long
- Write Multiple
- Write Sectors

Execution includes the transfer of one or more 512 byte (>512 bytes on Write Long) sectors of data from the host to the drive.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Drive/Head Registers.
2. The host writes the command code to the Command Register.
3. The drive sets BSY=1.
4. For each sector (or block) of data to be transferred:
 - a. The drive sets BSY=0 and DRQ=1 when it is ready to receive a sector (or block).
 - b. The host writes one sector (or block) of data via the Data Register.
 - c. The drive sets BSY=1 after it has received the sector (or block).
 - d. When the drive has finished processing the sector (or block), it sets BSY=0, and interrupts the host.
 - e. In response to the interrupt, the host reads the Status Register.
 - f. The drive clears the interrupt in response to the Status Register being read.
5. For the Write Long command:
 - a. The drive sets BSY=0 and DRQ=1 when it is ready to receive a sector.
 - b. The host writes one sector of data via the Data Register.
 - c. The drive keeps DRQ=1 after it has received the sector to request ECC bytes.
 - d. The host writes the ECC bytes via the Data Register.
 - e. After receiving the ECC bytes, the drive sets BSY=1.
 - f. After processing the sector and ECC bytes, the drive sets BSY=0 and interrupts the host.
 - g. In response to the interrupt, the host reads the Status Register.
 - h. The drive clears the interrupt in response to the Status Register being read.

The Write Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.

If the drive detects an invalid parameter, then it will abort the command by setting BSY=0, ERR=1, ABT=1, and interrupting the host.

If an uncorrectable error occurs, the drive will set BSY=0 and ERR=1, store the error status in the Error Register, and interrupt the host. The registers will contain the location (CHS) of the sector in error.

All data transfers to the drive through the Data Register are 16 bits, except for the ECC bytes, which are 8 bits.

12.3 Non-Data Commands

These commands are:

- Check Power Mode
- Erase Prepare
- Execute Drive Diagnostics
- Execute S.M.A.R.T. Function (Enable/Disable Attribute Autosave)

- Execute S.M.A.R.T. Function (Save Attribute Values)
- Execute S.M.A.R.T. Function (Enable S.M.A.R.T. Operations)
- Execute S.M.A.R.T. Function (Disable S.M.A.R.T. Operations)
- Execute S.M.A.R.T. Function (Return S.M.A.R.T. Status)
- Freeze Lock
- Idle
- Idle Immediate
- Initialize Drive Parameters
- Read Verify Sectors
- Recalibrate
- Seek
- Set Features
- Set Multiple
- Sleep
- Standby
- Standby Immediate

Execution of these commands involves no data transfer.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Drive/Head Registers.
2. The host writes the command code to the Command Register.
3. The drive sets BSY=1.
4. When the drive has finished processing the command, it sets BSY=0, and interrupts the host.
5. In response to the interrupt, the host reads the Status Register.
6. The drive clears the interrupt in response to the Status Register being read.

12.4 DMA Data Transfer Commands

These commands are:

- Read DMA
- Write DMA

Data transfer using DMA commands differ in two ways from PIO transfers:

- data transfers are performed using the slave-DMA channel
- no intermediate sector interrupts are issued on multi-sector commands

Initiation of the DMA transfer commands is identical to the Read Sector or Write Sector commands except that the host initializes the slave-DMA channel prior to issuing the command.

The interrupt handler for DMA transfers is different in that:

- no intermediate sector interrupts are issued on multi-sector commands

- the host resets the DMA channel prior to reading status from the drive.

The DMA protocol allows high performance multi-tasking operating systems to eliminate processor overhead associated with PIO transfers.

1. Host initializes the slave-DMA channel
2. Host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder and Drive/Head registers.
3. Host writes command code to the Command Register
4. The drive sets DMARQ when it is ready to transfer any part of the data.
5. Host transfers the data using the DMA transfer protocol currently in effect.
6. When all of the data has been transferred, the drive generates an interrupt to the host.
7. Host resets the slave-DMA channel
8. Host reads the Status Register and, optionally, the Error Register

13.0 Command Descriptions

Command	Hex Code	Binary Code							
		7	6	5	4	3	2	1	0
Check Power Mode	E5	1	1	1	0	0	1	0	1
Check Power Mode*	98	1	0	0	1	1	0	0	0
Execute Drive Diagnostics	90	1	0	0	1	0	0	0	0
Execute S.M.A.R.T. Function	B0	1	0	1	1	0	0	0	0
Format Track	50	0	1	0	1	0	0	0	0
Identify Drive	EC	1	1	1	0	1	1	0	0
Idle	E3	1	1	1	0	0	0	1	1
Idle*	97	1	0	0	1	0	1	1	1
Idle Immediate	E1	1	1	1	0	0	0	0	1
Idle Immediate*	95	1	0	0	1	0	1	0	1
Initialize Drive Parameters	91	1	0	0	1	0	0	0	1
Read Buffer	E4	1	1	1	0	0	1	0	0
Read DMA (retry)	C8	1	1	0	0	1	0	0	0
Read DMA (no retry)	C9	1	1	0	0	1	0	0	1
Read Long (retry)	22	0	0	1	0	0	0	1	0
Read Long (no retry)	23	0	0	1	0	0	0	1	1
Read Multiple	C4	1	1	0	0	0	1	0	0
Read Sectors (retry)	20	0	0	1	0	0	0	0	0
Read Sectors (no retry)	21	0	0	1	0	0	0	0	1
Read Verify Sectors (retry)	40	0	1	0	0	0	0	0	0
Read Verify Sectors (no retry)	41	0	1	0	0	0	0	0	1
Recalibrate	1x	0	0	0	1	—	—	—	—
Seek	7x	0	1	1	1	—	—	—	—
Set Features	EF	1	1	1	0	1	1	1	1
Set Multiple	C6	1	1	0	0	0	1	1	0
Sleep	E6	1	1	1	0	0	1	1	0
Sleep*	99	1	0	0	1	1	0	0	1
Standby	E2	1	1	1	0	0	0	1	0
Standby*	96	1	0	0	1	0	1	1	0
Standby Immediate	E0	1	1	1	0	0	0	0	0
Standby Immediate*	94	1	0	0	1	0	1	0	0

Commands marked * are alternate command codes for previous defined commands.

Figure 49. Command Set

Command	Hex Code	Binary Code							
		7	6	5	4	3	2	1	0
Write Buffer	E8	1	1	1	0	1	0	0	0
Write DMA (retry)	CA	1	1	0	0	1	0	1	0
Write DMA (no retry)	CB	1	1	0	0	1	0	1	1
Write Long (retry)	32	0	0	1	1	0	0	1	0
Write Long (no retry)	33	0	0	1	1	0	0	1	1
Write Multiple	C5	1	1	0	0	0	1	0	1
Write Sectors (retry)	30	0	0	1	1	0	0	0	0
Write Sectors (no retry)	31	0	0	1	1	0	0	0	1

Figure 50. Command Set --- Continued ---

Figure 49 on page 69 and Figure 50 shows the commands that are supported by the drive. The following symbols are used in the command descriptions:

Output Registers

- 0** Indicates that the bit must be set to 0.
- 1** Indicates that the bit must be set to 1.
- D** The drive number bit. Indicates that the drive number bit of the Drive/Head Register should be specified. Zero selects the master drive and one selects the slave drive.
- H** Head number. Indicates that the head number part of the Drive/Head Register is an output parameter and should be specified.
- L** LBA mode. Indicates the addressing mode. Zero specifies CHS mode and one does LBA addressing mode.
- R** Retry. Indicates that the Retry bit of the Command Register should be specified.
- V** Valid. Indicates that the bit is part of an output parameter and should be specified.
- x** Indicates that the hex character is not used.
- Indicates that the bit is not used.

Input Registers

- 0** Indicates that the bit is always set to 0.
- 1** Indicates that the bit is always set to 1.
- H** Head number. Indicates that the head number part of the Drive/Head Register is an input parameter and will be set by the drive.
- V** Valid. Indicates that the bit is part of an input parameter and will be set to 0 or 1 by the drive.
- Indicates that the bit is not part of an input parameter.

The command descriptions show the contents of the Status and Error Registers after the drive has completed processing the command and has interrupted the host.

13.1 Check Power Mode

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	0	1	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	0	0	-	-	0	-	V

Figure 51. Check Power Mode Command (E5h)

The Check Power Mode command will report whether the drive is spun up and the media is available for immediate access.

Input Parameters From The Drive

Sector Count The power mode code. The command returns FFh in the Sector Count Register if the spindle motor is at speed and the drive is not in Standby or Sleep mode. Otherwise, the Sector Count Register will be set to 0.

13.2 Execute Drive Diagnostics

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	-	-	-	-	-
Command	1	0	0	1	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
V	V	V	V	V	V	V	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	0	0	-	-	0	-	0

Figure 52. Execute Drive Diagnostics Command (90h)

The Execute Drive Diagnostics command performs the internal diagnostic tests implemented by the drive. The results of the test are stored in the Error Register.

The normal Error Register bit definitions do not apply to this command. Instead, the register contains a diagnostic code. See Figure 48 on page 62 for the definition.

13.3 Execute S.M.A.R.T. FUNCTION

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - -
Feature	V V V V V V V V
Sector Count	- - - - -
Sector Number	- - - - -
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Drive/Head	1 - 1 D - - - -
Command	1 0 1 1 0 0 0 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - -
Error	...See Below...
Sector Count	- - - - -
Sector Number	- - - - -
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Drive/Head	- - - - -
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	TON	AMN
0	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 53. Execute S.M.A.R.T. FUNCTION Command (B0h)

The Execute S.M.A.R.T. FUNCTION command provides access to Attribute Values, Attribute Thresholds and other low level subcommands.

Output Parameters To The Drive

Feature S.M.A.R.T. subcommand code.

- D0h** Read Attribute Values
- D1h** Read Attribute Thresholds
- D2h** Enable/Disable Attribute Autosave
- D3h** Save Attribute Values
- D8h** Enable S.M.A.R.T. Operations
- D9h** Disable S.M.A.R.T. Operations
- DAh** Return S.M.A.R.T. Status

Cylinder Low 4Fh (key value)

Cylinder High C2h (key value)

13.3.1 Read Attribute Values (subcommand = D0h)

This subcommand returns the Attribute Values to the host. Upon receipt of the subcommand from host, the drive saves any updated Attribute Values to the disk, and then transfer the 512 bytes of Attribute Value information described in 13.3.8, “Drive Attributes Data Structure” on page 75 to the host.

13.3.2 Read Attribute Thresholds (subcommand = D1h)

This subcommand returns the Attribute Thresholds to the host. Upon receipt of the subcommand from host, the drive saves any updated Attribute Values to the disk, and then transfer the 512 bytes of Attribute Thresholds information described in 13.3.9, “Drive Attribute Thresholds Data Structure” on page 77 to the host. The Attribute Thresholds Data are read from the disk at power-on time and kept in the volatile memory of the drive.

13.3.3 Enable/Disable Attribute Autosave (subcommand = D2h)

The valid value written by host into the Sector Count register is 00h or F1h.

This subcommand is supported for the system which might require that the drive responds without error for the subcommand. The Attribute Values are saved as described in 13.3.10, “Attribute Values Saving Function” on page 77 regardless of the value of the Sector Count register.

Upon receipt of the subcommand from host, the drive saves any updated Attribute Values to the disk.

13.3.4 Save Attribute Values (subcommand = D3h)

This subcommand causes the drive to immediately save any updated Attribute Values to the disk.

13.3.5 Enable S.M.A.R.T. Operations (subcommand = D8h)

This subcommand enables access to all S.M.A.R.T. capabilities within the drive. The state of S.M.A.R.T. (either enabled or disabled) is preserved by the drive across power cycles.

Upon receipt of the subcommand from host, the drive saves any updated Attribute Values to the disk.

13.3.6 Disable S.M.A.R.T. Operations (subcommand = D9h)

This subcommand disables access to all S.M.A.R.T. capabilities within the drive. The state of S.M.A.R.T. (either enabled or disabled) is preserved by the drive across power cycles.

Upon receipt of the subcommand from host, the drive saves any updated Attribute Values to the disk.

Any Attribute Values supported by DJAA-3xxxx are monitored and saved by the drive regardless the state of S.M.A.R.T..

13.3.7 Return S.M.A.R.T. Status (subcommand = DAh)

This subcommand is used to communicate the reliability status of the drive to the host at the host's request. Upon receipt of the subcommand from host, the drive saves any updated Attribute Values to the disk and compare them to the Attribute Thresholds.

The drive sets S.M.A.R.T. status into the Cylinder Low and the Cylinder High register as below.

If the drive does not detect a Threshold Exceeded Condition,

Cylinder Low 4Fh

Cylinder High C2h

If the drive does detect a Threshold Exceeded Condition,

Cylinder Low F4h

Cylinder High 2Ch

13.3.8 Drive Attributes Data Structure

Byte Offset	Bytes	Contents	Description
0 - 1	2	0005H	Data Structure Revision Number
2 - 13	12	see below	1st Drive Attribute
..			
..			
350 - 361	12	see below	30th Drive Attribute
362 - 367	6	0000H	Off-line Data Correction Status
368 - 369	2	0002H	S.M.A.R.T. capability
370 - 385	16	0000H	Reserved
386 - 510	125	XXXXH	Vendor Unique
511	1	XXH	Checksum

Figure 54. Drive Attributes Data Structure

Byte Offset	Bytes	Contents	Description
0	1	XXH	Attribute ID Number
1 - 2	2	XXH	Status Flags bit 0 : Pre-Failure/Advisory bit 1 - 5 : Vendor Specific bit 6 - 15 : Reserved
3	1	XXH	Attribute Value
4 - 11	8	XXH	Vendor Unique

Figure 55. Individual Attribute Data Structure

13.3.8.1 Supported Attributes

DJAA-3xxx supports 6 Attributes described below.

1st Attribute	Spin Up Time	
	Attribute ID	03H
	Pre-Failure/Advisory Flag	1
2nd Attribute	Start/Stop Count	
	Attribute ID	04H
	Pre-Failure/Advisory Flag	0
3rd Attribute	Reallocated Sector Count	
	Attribute ID	05H
	Pre-Failure/Advisory Flag	1
4th Attribute	Power-On Hours	
	Attribute ID	09H
	Pre-Failure/Advisory Flag	0
5th Attribute	Spin Retry Count	
	Attribute ID	0AH
	Pre-Failure/Advisory Flag	1
6th Attribute	Power Cycle Count	
	Attribute ID	0CH
	Pre-Failure/Advisory Flag	0

13.3.9 Drive Attribute Thresholds Data Structure

Byte Offset	Bytes	Contents	Description
0 - 1	2	0005H	Data Structure Revision Number
2 - 13	12	see below	1st Drive Attribute
..			
..			
350 - 361	12	see below	30th Drive Attribute
362 - 379	18	0000H	Reserved
380 - 510	131	XXXXH	Vendor Unique
511	1	XXH	Checksum

Figure 56. Drive Attribute Thresholds Data Structure

Byte Offset	Bytes	Contents	Description
0	1	XXH	Attribute ID Number
1	1	XXH	Attribute Threshold
2 - 11	10	00H	Reserved

Figure 57. Individual Threshold Data Structure

13.3.10 Attribute Values Saving Function

The drive saves its Reallocated Sector Count upon the event listed below.

- Automatic Sector Reallocation
- FORMAT TRACK command with ASSIGN or UNASSIGN descriptor

The drive saves any Attribute Values Data other than the Reallocated Sector Count upon the event listed below.

- After initialization by Power-On or Hard Reset
- S.M.A.R.T. commands
- Power Mode commands
 - IDLE IMMEDIATE
 - IDLE

- STANDBY IMMEDIATE
- STANDBY
- SLEEP

Though the drive supports Auto-Standby function, it does not save its Attribute Values upon transition from an Idle state to the Auto- Standby state.

13.4 Format Track

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H	H
Command	0	1	0	1	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 58. Format Track Command (50h)

The Format Track command formats a single track on the drive. Each good sector of data on the track will be initialized to zero. Any data previously stored on the track will be lost.

The host writes a sector containing a format table to the drive. The format table should contain two bytes for each sector on the track to be formatted. The first byte should contain a descriptor value and the second byte should contain the sector number. The descriptor value should be

- 00h for a good sector,
- 20h for an unassign sector from an alternate location,
- 40h for an alternate sector,
- 80h for a bad sector,

and any other descriptor value will be ignored. The remaining bytes of the sector following the format table are ignored.

Since drive performance is optimal at 1:1 interleave, and the drive uses relative block addressing internally, the drive will always format a track in the same way no matter what sector numbering is specified in the format table.

Output Parameters To The Drive

Sector Number In LBA mode, this register specifies LBA address bits 0 - 7 to be formatted. (L=1)

Cylinder High/Low The cylinder number of the track to be formatted. (L=0)
In LBA mode, this register specifies LBA address bits 8 - 15 (Low), 16 - 23 (High) to be formatted. (L=1)

H The head number of the track to be formatted. (L=0)
In LBA mode, this register specifies LBA address bits 24 - 27 to be formatted. (L=1)

Input Parameters From The Drive

Sector Number In LBA mode, this register specifies current LBA address bits 0-7. (L=1)

Cylinder High/Low In LBA mode, this register specifies current LBA address bits 8 - 15 (Low), 16 - 23 (High)

H In LBA mode, this register specifies current LBA address bits 24 - 27. (L=1)

Error The Error Register. An Abort error (ABT=1) will be returned under the following conditions:

- The descriptor value does not match the certain value. (except 00h, 20h, 40h and 80h)
- The number of assign(40h) exceeds the maximum number of reassign table entry.

In LBA mode, this command formats a single track including the specified LBA.

13.5 Identify Drive

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	1	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 59. Identify Drive Command (ECh)

The Identify Drive command requests the drive to transfer configuration information to the host. The drive will transfer a sector to the host containing the information in Figure 60 on page 82.

Word	Content	Description
00	045AH	Drive classification, bit assignments: 15(=0): 1=not magnetic disk drive 14(=0): 1=format speed tolerance gap required 13(=0): 1=track offset option available 12(=0): 1=data strobe offset option available 11(=0): 1=rotational speed tolerance > 0.5% 10(=1): 1=disk transfer rate > 10 Mbps 9(=0): 1=disk transfer rate > 5 Mbps but <= 10 Mbps 8(=0): 1=disk transfer rate <= 5 Mbps 7(=0): 1=removable cartridge drive 6(=1): 1=fixed drive 5(=0): 1=spindle motor control option implemented 4(=1): 1=head switch time > 15 us 3(=1): 1=not MFM encoded 2(=0): 1=soft sectoring 1(=1): 1=hard sectoring 0(=0): reserved
01	Note.1	Number of cylinders in default translate mode
02	0	Number of removable cylinders
03	Note.1	Number of heads in default translate mode
04	0	Reserved
05	0	Reserved
06	Note.1	Number of sectors per track in default translate mode
07	0000H	Number of bytes of sector gap
08	0000H	Number of bytes in sync field
09	0000H	Reserved
10-19	XXXX	Serial number in ASCII (0 = not specified)
20	0003H	Controller type: 0003: dual ported, multiple sector buffer with look-ahead read
21	0080H	Buffer size in 512-byte increments
22	0010H	Number of ECC bytes as currently selected via the set features command
23-26	XXXX	Microcode version in ASCII
27-46	Note.1	Model number in ASCII
47	0010H	Number of sectors that can be transferred per interrupt on Read and Write Multiple commands
48	0000H	Capable of double word I/O, '0000'= cannot perform
49	0F00H	Capabilities, bit assignments: 15-12(=0) Reserved 11(=1) IORDY Supported 10(=1) IORDY can be disabled 9(=1) 1=LBA Supported 8(=1) 1=DMA Supported 7- 0(=0) Reserved
50	0000H	Reserved
51	0200H	PIO data transfer cycle timing mode

Figure 60. Identify drive information

Word	Content	Description
52	0000H	DMA data transfer cycle timing mode Refer Word 62 and 63
53	0003H	Validity flag of the word 15- 2(=0) Reserved 1 1= Word 64-70 are Valid 0 1= Word 54-58 are Valid
54	XXXXH	Number of current cylinders
55	XXXXH	Number of current heads
56	XXXXH	Number of current sectors per track
57-58	XXXXH	Current capacity in sectors Word 57 specifies the low word of the capacity
59	0XXXH	Current Multiple setting. bit assignments 15- 9(=0) Reserved 8 1= Multiple Sector Setting is Valid 7- 0 xxh = Current setting for number of sectors
60-61	Note.1	Total Number of User Addressable Sectors Word 60 specifies the low word of the number
62	xx07H	Single Word DMA Transfer Capability 15- 8 Single word DMA transfer mode active 7- 0(=7) Single word DMA transfer modes supported (support mode 0,1 and 2)
63	xx07H	Multiword DMA Transfer Capability 15- 8 Multi word DMA transfer mode active 7- 0(=7) Multi word DMA transfer modes supported (support mode 0,1 and 2)
64	0003H	Flow Control PIO Transfer Modes Supported 15- 8(=0) Reserved 7- 0(=3) Advanced PIO Transfer Modes Supported '03' = PIO Mode 4 Supported
65	0078H	Minimum Multiword DMA Transfer Cycle Time Per Word 15- 0(=078) Cycle time in nanoseconds (120ns, 16.6MB/s)
66	0078H	Manufacturer's Recommended Multiword DMA Transfer Cycle Time 15- 0(=078) Cycle time in nanoseconds (120ns, 16.6MB/s)
67	00C8H	Minimum PIO Transfer Cycle Time Without Flow Control 15- 0(=0C8) Cycle time in nanoseconds (200ns, 8.3MB/s)
68	0078H	Minimum PIO Transfer Cycle Time With IORDY Flow Control 15- 0(=078) Cycle time in nanoseconds (120ns, 16.6MB/s)
69-127	0000H	Reserved

Figure 61. Identify drive information --- Continued ---

Word	Content	Description
128	XXXXH	Reserved
129	XXXXH	Current Set Feature Option. Bit assignments 0 Write Cache 1= Enable 1 Read Look-ahead 1= Enable 2 Reverting 1= Enable 3 Auto reassign 1= Enable 4-15 Reserved
130	XXXXH	Reserved
131-255	0000H	Reserved

Figure 62. Identify drive information --- Continued ---

Note 1. The number of cylinders, heads, sectors per track, total number of user addressable sectors and the model number in ASCII are as follows.

Model	Cylinders	Heads	Sectors	Total LBAs	Model Number in ASCII
DJAA-31270	09B0H	10H	3FH	262500H	'IBM-DJAA-31270'
DJAA-31700	0CECH	10H	3FH	32E140H	'IBM-DJAA-31700'

13.6 Idle

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	0	0	1	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 63. Idle Command (E3h)

The Idle command causes the drive to enter Idle mode.

When the Idle mode is entered, the drive is spun up to operating speed. If the drive is already spinning, the spin up sequence is not executed.

During Idle mode the drive is spinning and ready to respond to host commands immediately.

The automatic power down sequence is enabled and the timer starts counting down.

Output Parameters To The Drive

Sector Count Timeout Parameter. If zero, then the automatic power down sequence is disabled. If non-zero, then the automatic power down sequence is enabled, and the timeout interval is set at the Timeout Parameter times 5, in seconds, for the value range from 12 to 255. If the value is 1 to 11, the Timeout Value is 60 seconds.

When the automatic power down sequence is enabled, the drive will enter Standby mode automatically if the timeout interval expires with no drive access from the host. The timeout interval will be reinitialized if there is a drive access before the timeout interval expires.

13.7 Idle Immediate

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	0	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 64. Idle Immediate Command (E1h)

The Idle Immediate command causes the drive to enter Idle mode. The drive is spun up to operating speed. If the drive is already spinning, the spin up sequence is not executed.

During Idle mode the drive is spinning and ready to respond to host commands immediately.

The Idle Immediate command will not affect to auto power down timeout parameter.

13.8 Initialize Drive Parameters

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	—	—	—	—	—	—	—	—
Feature	—	—	—	—	—	—	—	—
Sector Count	V	V	V	V	V	V	V	V
Sector Number	—	—	—	—	—	—	—	—
Cylinder Low	—	—	—	—	—	—	—	—
Cylinder High	—	—	—	—	—	—	—	—
Drive/Head	1	0	1	D	H	H	H	H
Command	1	0	0	1	0	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	—	—	—	—	—	—	—	—
Error	—	—	—	—	—	—	—	—
Sector Count	—	—	—	—	—	—	—	—
Sector Number	—	—	—	—	—	—	—	—
Cylinder Low	—	—	—	—	—	—	—	—
Cylinder High	—	—	—	—	—	—	—	—
Drive/Head	—	—	—	—	—	—	—	—
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	0	0	—	—	0	—	V

Figure 65. Initialize Drive Parameters Command (91h)

The Initialize Drive Parameters command enables the host to set the number of sectors per track and the number of heads minus 1, per cylinder. Words 54-58 in Identify Drive Information reflects these parameters.

The parameters remain in effect until following events:

- Another Initialize Drive Parameters command is received.
- The drive is powered off.
- Hard reset is occurred.
- Soft reset is occurred and the Set Feature option of CCh is set instead of 66h.

Output Parameters To The Drive

Sector Count The number of sectors per track. 0 does not mean there are 256 sectors per track, but there is no sector per track.

H The number of heads minus 1 per cylinder. The minimum is 0 and the maximum is 15. However inline with ATA-2 any other value will be accepted but drive operation is then not guaranteed.

13.9 Read Buffer

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	0	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 66. Read Buffer Command (E4h)

The Read Buffer command transfers a sector from the sector buffer to the host. The sector is transferred through the Data Register 16 bits at a time.

The sector transferred will be from the same part of the buffer written to by the last Write Buffer command. The contents of the sector may be different if any reads or writes have occurred since the Write Buffer command was issued.

R The retry bit. If set to one, then retries are disabled.

Input Parameters From The Drive

Sector Count The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.

Sector Number The sector number of the last transferred sector. (L=0)

In LBA mode, this register contains current LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the last transferred sector. (L=0)

In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H The head number of the sector to be transferred. (L=0)

In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

- H** The head number of the sector to be transferred. (L=0)
 In LBA mode, this register contains LBA bits 24-27. (L=1)
- R** The retry bit. If set to one, then retries are disabled.

Input Parameters From The Drive

- Sector Count** The number of requested sectors not transferred.
- Sector Number** The sector number of the transferred sector. (L=0)
 In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
- Cylinder High/Low** The cylinder number of the transferred sector. (L=0)
 In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High).
 (L=1)
- H** The head number of the transferred sector. (L=0)
 In LBA mode, this register contains current LBA bits 24-27. (L=1)

It should be noted that the drive internally uses 18 bytes of ECC data on all data written or read from the disk. The 4 byte mode of operation is provided via an emulation. It is recommended that for testing the effectiveness and integrity of the drives ECC functions that the 18 byte ECC mode should be used.

Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

Sector Number The sector number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High).
(L=1)

H The head number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

Note 1.

When Feature register is 03h (=Set Transfer mode), the Sector Count Register specifies the transfer mechanism. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value.

PIO Default Transfer Mode	00000	000
PIO Default Transfer Mode,Disable IORDY	00000	001
PIO Flow Control Transfer Mode x	00001	nnn (nnn=000,001,010,011,100)
Single word DMA mode x	00010	nnn (nnn=000,001,010)
Multiword DMA mode x	00100	nnn (nnn=000,001)

Note 2.

If the number of auto reassigned sector reaches the drive's reassignment capacity, the write cache function will be automatically disabled. Although the drive still accepts the Set Features command with Feature register = 02h without error, but the write cache function will remains disabled. For current write cache function status, please refer to Identify Drive Information(129word) by Identify Drive command.

Note 3.

After power on reset, the drive is set to the following features as default.

Write cache	:	Enable
ECC bytes	:	4 bytes
Read look-ahead	:	Enable
Reverting to power on defaults	:	Disable

13.18 Set Multiple

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	— — — — — — — —
Feature	— — — — — — — —
Sector Count	V V V V V V V V
Sector Number	— — — — — — — —
Cylinder Low	— — — — — — — —
Cylinder High	— — — — — — — —
Drive/Head	1 0 1 D — — — —
Command	1 1 0 0 0 1 1 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	— — — — — — — —
Error	...See Below...
Sector Count	— — — — — — — —
Sector Number	— — — — — — — —
Cylinder Low	— — — — — — — —
Cylinder High	— — — — — — — —
Drive/Head	— — — — — — — —
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	—	—	0	—	V

Figure 75. Set Multiple Command (C6h)

The Set Multiple command enables the drive to perform Read and Write Multiple commands and establishes the block size for these commands. The block size is the number of sectors to be transferred for each interrupt.

The default block size after power up, soft reset, or hard reset is 0, and Read Multiple and Write Multiple commands are disabled.

If an invalid block size is specified, an Abort error will be returned to the host, and Read Multiple and Write Multiple commands will be disabled.

Output Parameters To The Drive

Sector Count. The block size to be used for Read Multiple and Write Multiple commands. Valid block sizes can be selected from 0, 2, 4, 8, or 16. If 0 is specified, then Read Multiple and Write Multiple commands are disabled.

13.19 Sleep

Command Block Output Registers							
Register	7	6	5	4	3	2	1 0
Data	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V V
Sector Number	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-
Command	1	1	1	0	0	1	1 0

Command Block Input Registers							
Register	7	6	5	4	3	2	1 0
Data	-	-	-	-	-	-	-
Error	...See Below...						
Sector Count	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-
Status	...See Below...						

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 76. Sleep Command (E6h)

This command is handled as Standby command.

13.21 Standby Immediate

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							-

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 78. Standby Immediate Command (E0h)

The Standby Immediate command causes the drive to enter Standby mode immediately. The drive is spun down but the interface remains active. If the drive is already spun down, the spin down sequence is not executed.

During the Standby mode, the drive will respond to commands, but there is a delay while waiting for the spindle to reach operating speed.

The Standby Immediate command will not affect to auto power down timeout parameter.

13.22 Write Buffer

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	1	0	1	D	-	-	-	-
Command	1	1	1	0	1	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Drive/Head	-	-	-	-	-	-	-	-
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	-	V

Figure 79. Write Buffer Command (E8h)

The Write Buffer command transfers a sector of data from the host to the sector buffer. The sectors of data are transferred through the Data Register 16 bits at a time.

The Read Buffer and Write Buffer commands are synchronized such that sequential Write Buffer and Read Buffer commands access the same 512 byte within buffer.

R The retry bit. If set to one, then retries are disabled. But ignored, when write cache is enabled. (Ignoring the retry bit is in violation of ATA-2.)

Input Parameters From The Drive

Sector Count The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.

Sector Number The sector number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H The head number of the last transferred sector. (L=0)
In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

Input Parameters From The Drive

Sector Count	The number of requested sectors not transferred.
Sector Number	The sector number of the sector to be transferred. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the sector to be transferred. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the sector to be transferred. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

The drive internally uses 18 bytes of ECC on all data read or writes. The 4 byte mode of operation is provided via an emulation technique. As a consequence of this emulation it is recommended that 18 byte ECC mode is used for all tests to confirm the operation of the drives ECC hardware. Unexpected results may occur if such testing is performed using 4 byte mode.

The last 2 bytes for 18 bytes ECC data should be always 00H data.

13.25 Write Multiple

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	0	1	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	-	-	-	-	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	-	V

Figure 82. Write Multiple Command (C5h)

The Write Multiple command transfers one or more sectors from the host to the drive. Command execution is identical to the Write Sectors command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector. The sectors are transferred through the Data Register 16 bits at a time.

Output Parameters To The Drive

Sector Count The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number The sector number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H The head number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 24 - 27. (L=1)

Input Parameters From The Drive

Sector Count The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.

Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

13.26 Write Sectors

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	–	–	–	–	–	–	–	–
Feature	–	–	–	–	–	–	–	–
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	1	L	1	D	H	H	H	H
Command	0	0	1	1	0	0	0	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	–	–	–	–	–	–	–	–
Error	...See Below...							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Drive/Head	–	–	–	–	H	H	H	H
Status	...See Below...							

Error Register							
7	6	5	4	3	2	1	0
BBK	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DWF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	–	0	–	V

Figure 83. Write Sectors Command (30h/31h)

The Write Sectors command transfers one or more sectors from the host to the drive. The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Output Parameters To The Drive

- Sector Count** The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
- Sector Number** The sector number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 0 - 7. (L=1)
- Cylinder High/Low** The cylinder number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
- H** The head number of the first sector to be transferred. (L=0)
In LBA mode, this register contains LBA bits 24 - 27. (L=1)
- R** The retry bit. If set to one, then retries are disabled. But ignored, when write cache is enabled. (Ignoring the retry bit is in violation of ATA-2.)

Input Parameters From The Drive

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

14.0 Timings

The timing of BSY and DRQ in Status Register are shown in Figure 84

FUNCTION	INTERVAL	START	STOP	TIMEOUT
Power On	Drive Busy After Power On	Power On	Status Register BSY=1	400 ns
	Drive Ready After Power On	Power On	Status Register BSY=0 and RDY=1	31 sec
Software Reset	Drive Busy After Software Reset	Device Control Register RST=1	Status Register BSY=1	400 ns
	Drive Ready After Software Reset	Device Control Register RST=1	Status Register BSY=0 and RDY=1	6 sec
Hard Reset	Drive Busy After Hard Reset	Bus RESET Signal Asserted	Status Register BSY=1	400 ns
	Drive Ready After Hard Reset	Bus RESET Signal Asserted	Status Register BSY=0 and RDY=1	31 sec
Data In Command	Drive Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns
	Interrupt, DRQ For Data Transfer In	Status Register BSY=1	Status Register BSY=0 and DRQ=1, Interrupt	30 sec
	Drive Busy After Data Transfer In	256th Read From Data Register	Status Register BSY=1	10 us
Data Out Command	Drive Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns
	Data Request For Data Transfer Out	Status Register BSY=1	Status Register BSY=0 and DRQ=1	900 us
	Drive Busy After Data Transfer Out	256th Write From Data Register	Status Register BSY=1	5 us
	Interrupt For Data Transfer Out	Status Register BSY=1	Interrupt	30 sec
Non-Data Command	Drive Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns
	Interrupt For Command Complete	Status Register BSY=1	Interrupt	6 sec

Figure 84. Timeout Values

FUNCTION	INTERVAL	START	STOP	TIMEOUT
DMA Data Transfer Command	Drive Busy after Command Code Out	Out to Command Register	Status Register BSY=1	400 ns

Figure 85. Timeout Values --- Continued ---

Command category is referred to 12.0, "Command Protocol" on page 63.

The abbreviations "ns", "us", "ms" and "sec" mean nanoseconds, microseconds, milliseconds and seconds, respectively.

14.1 Write Cache Function

Write cache is a performance enhancement whereby the drive reports as completing the write command (Write Sectors and Write Multiple) to the host as soon as the drive has received all of the data into its buffer. And the drive assumes responsibility to write the data subsequently onto the disk.

14.1.1 Attention

- While writing data after completed acknowledgment of a write command, soft reset does not affect its operation. But hard reset or power off terminates writing operation immediately and unwritten data are to be lost. So hard reset or power off must not be done in 5 seconds after the completion of a write command.
- The retry bit of Write Sectors is ignored when write cache is enabled. This is in violation of ATA-2.

Index

A

ABRT 59
ABT 59
AMN 59
AMNF 59
 Features Register
 Sector Count Register
 Sector Number Register
 Status Register
Automatic Power Down Sequence 105

B

BBK 59
BSY 60

C

Check Power Mode 65, 71
Command
 Check Power Mode 71
 Execute Drive Diagnostics 72
 Execute S.M.A.R.T. FUNCTION 73
 Format Track 79
 Identify Drive 81
 Idle 85
 Idle Immediate 86
 Initialize Drive Parameters 87
 Read Buffer 88
 Read DMA 89
 Read Long 91
 Read Multiple 93
 Read Sectors 95
 Read Verify 97
 Recalibrate 99
 Seek 100
 Seek Overlap 53
 Set Features 101
 Set Multiple 103
 Sleep 104
 Standby 105
 Standby Immediate 106
 Write Buffer 107
 Write DMA 108
 Write Long 110
 Write Multiple 112
 Write Sectors 114
COR 60
CORR 60

D

D 70

Diagnostic Codes 58, 62, 72
DRDY 60
DRQ 60
DRV 58
DS0 58
 Drive/Head Register
DS1 57
DSC 60
DWF 60

E

Erase Prepare 65
ERR 60
Error Register
 Diagnostic Codes 62
Execute Drive Diagnostics 65, 72
Execute S.M.A.R.T. FUNCTION 73
Execute S.M.A.R.T. Function (Disable S.M.A.R.T.
 Operations) 66
Execute S.M.A.R.T. Function (Enable S.M.A.R.T.
 Operations) 66
Execute S.M.A.R.T. Function (Enable/Disable Attribute
 Autosave) 65
Execute S.M.A.R.T. Function (Read Attribute Thresh-
 olds) 63
Execute S.M.A.R.T. Function (Read Attribute
 Values) 63
Execute S.M.A.R.T. Function (Return S.M.A.R.T.
 Status) 66
Execute S.M.A.R.T. Function (Save Attribute
 Values) 65

F

Format Track 64, 79
Freeze Lock 66

H

H 70
H0 57
H1 57
H2 57
H3 57
HS0 58
HS1 58
HS2 58
HS3 58
 Error Register 58

I

Identify Drive 63, 81

Idle 66, 85
Idle Immediate 66, 86
IDN 59
IDNF 59
IDX 60
IEN 57
 Drive Address Register
Initialize Drive Parameters 66, 87

L
L 58, 70

M
Master 58

R
R 70
RDY 60
Read Buffer 63, 88
Read DMA 66, 89
Read Long 63, 91
Read Multiple 63, 93
Read Sectors 63, 95
Read Verify 97
Read Verify Sectors 66
Recalibrate 66, 99
Register
 Alternate Status Register 56
 Command Register 56
 Cylinder High Register
 Cylinder Low Register 56
 Data Register
 Device Control Register
 Register Initialization 62
Register Initialization 62
Reset
 Register Initialization 62
RST 57

S
Seek 66, 100
Set Features 66, 101
Set Multiple 66, 103
Slave 58
Sleep 66, 104
SRST 57
Standby 66, 105
Standby Immediate 66, 106

T
TON 59
Timeout Interval 57, 115
Timeout Parameter 85, 105

TK0NF 59

U
UNC 59

V
V 70

W
Write Buffer 64, 107
Write Cache 119
Write DMA 66, 108
Write Long 64, 110
Write Multiple 64, 112
Write Sectors 64, 114
WTG 57

X
x 70



S29H-7278-05