OEM Manual

Hard Disk Drive Specifications
Travelstar C4K60-60/40/30/20

REV.1

Models: HTC426060G9AT00
HTC426040G9AT00
HTC426030G7AT00
HTC426020G7AT00

⚠ Caution for Safety
Read Safety descriptions carefully.
Read and recommend drive usage cautions to your end user.
Keep this manual with care.

(Total 146 pages)

H I T A C H I

K6610168
Rev.1
Nov 19, 2004

⚠ To use this product safely

This manual is for the original purchaser of Travelstar C4K60-60/4030/20 and intendes to provide information about handling, installation, specifications, principles of operation and interface command implementation.
To use the product, read safety descriptions below and understand thoroughly.
Keep this manual with care to insure unlimited use.

- **General Caution for Safety**

The followings are general cautions for safe use of this product.

(Caution before Product Use)

- Please read and follow all instructions and cautions described on "Safety Instructions" (Page 5) and "1.2 General Caution" (Page 12) before attempting to use this product.
- Follow all instructions and cautions indicated throughout this manual and the product. Failure to follow these instructions and cautions may cause injury, fire and product damage.

- **Advise your end user of the safety caution**

Read and recommend that your end users read the caution for drive usage in this manual.

- **Protect yourself**

The safety instructions in this manual were thoroughly considered, but unexpected situations can occur. Not only follow the instructions on this manual, but also be careful for the safety of yourself.

- **Headline of safety caution**

Safety instructions and cautions are indicated as the following headline, which consists a word of "Caution". The indication and meaning are as follows:

⚠ Caution: This symbol indicates that potential danger may exist which may cause slight or medium grade bodily injury ,if safety instructions are not followed.

Caution: This symbol indicates that potential danger may exist which may cause damage to the product or to the neighboring property ,if safety instructions are not followed.

- ⚠ **Safety caution in this manual**

Followings are the cautions and contents described in this manual.

Items of indicating ⚠ Caution :

Items of indicating Caution :

⚠ To use this product safely (Continued)

- **Environmental circumstance**

Although this product partially scatters electro-magnetic field into the air, it has been inspected and was installed under Electro-magnetic regulations of resident areas, such as EMC standard EN55022 (corresponding to FCC part 15 Class B, etc.). However, anything other than this product, such as an interface cable, is excluded. Therefore, the following cases require a system side improvement for the electro-magnetic field regulations.
1) Disturbance of operations of other products or equipment in resident area
2) Disturbance caused by other product, such as cabling, to operations of other products or equipment.

Only Hitachi trained persons should change this product Hitachi assumes no responsibility for products which have been changed by anyone else.

- **Safety regulations**

This product meets the following safety regulations, but the system side should consider the safety of the system with this product.

Regulations:
- UL1950 Third Edition dated July 28, 1995
- CSA C22.2 N0.950-M95
- IEC60950 A4: 1996
- EN60950 A11: 1992

Warranty and Limited Liability

This product is sold with a limited warranty and specific remedies are available to the original purchaser in the event the product fails to conform to the limited warranty. Hitachi's liability may be further limited in accordance with its sales contact.

In general, Hitachi shall not be responsible for product damages caused by natural disasters, fire, static discharge, misuse, abuse, neglect, improper handling or installation, unauthorized repair, alteration or accident. In no event will Hitachi be liable for loss of data stored on product.

HITACHI SHALL NOT BE LIABLE FOR ANY SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES, EVEN IF INFORMED OF THE POSSIBILITY THEREOF IN ADVANCE.

Please see your sales contract for a complete statement of warranty rights, remedies and limitation of liability.

Safety Instructions

⚠ Caution

1. The product is not authorized for use in life support devices or systems or other applications that pose a significant risk of personal injury.
2. Since the drive uses glass media for the disk platter, opening of Metal Head Disk Assembly (HDA) may cause bodily injury. Warranty void in case of opened HDA or any broken HDA seals. Don't open the HDA or break any HDA seals.
3. Dropping of the HDD may cause bodily injury. Handle with care.
4. Do not hit the interface connector pins against other objects. Do not make contact with the interface connector pins. Contact causes pin dent, electrical discharge distraction or contact failure. Also, pins or HDA corners may cause bodily injury. Handle with care.

Caution

5. Observe Clause 3.3 "Drive Usage Condition Specifications". Since reliability and product life depends on usage conditions, please consult our sales or application engineers.
6. Keep usage conditions within specifications (Power Supply, Environment, etc.). If the conditions are not kept within the specifications, failures may occur.
7. Hot swapping (Power-on swapping) can damage the drive. The drive shall be swapped during Power Off only.
8. Electro Static Discharge (ESD) can damage the drive. Protect the drive from ESD during handling.
9. Voltage rise time 5 - 100 ms at power on is required for power supply. The power supply voltage must not be under –0.3V at power off.
10. This product is required over current protection for possible combustion due to circuit or component failure. Secondary over current protection shall be prepared by the system. The requirement of the current limitation is max. 10 A for the protection.
11. Improper insertion of connector or wrong jumper setting may cause catastrophic failures. Referring to this manual prior to the connector insertion or jumper setting can help to insure correct insertion.
12. If a foreign conductive substance (metallic powder, fluid, etc.) adheres to active metal of the drive (Printed pattern, component lead, etc. on PCBA), it may cause catastrophic failures. Customer should protect the drive from the above condition.
13. The PCBA side of the drive should be covered with insulation sheet if the active metal of host system may contact to the PCBA of the drive. If the insulation sheet is not provided for the possible contact of the live metal, failures may occur.
14. Shock can result in permanent damage to the drive and/or loss of data. Prevent shocks, which is often incurred by dropping, knocking over, or hitting the drive.
15. To fix the drive, use the size of screws and the torque recommended in this manual. If non-recommended size screws and torque are used, it may cause catastrophic failures.
16. Do not press top cover. It may cause catastrophic failures. In case of steel plate installation on HDD cover side, the spacing between HDD cover and steel plate should be kept more than 2 mm. If this spacing is not kept for the steel plate, it may affect Load/Unload mechanism.
17. Do not push the bottom PCBA of the drive. It may cause catastrophic failures.

Caution

18. Prevent humidity when the drive is packed in a box.
19. Use original packages during drive transportation to protect from any damage.
    (Keep some extra packages for the drive transportation)
20. Recorded data on the disk may be lost due to accidents such as disasters, shock damage during handling or drive failure. To prepare for accidents, back up data. Hitachi does not perform data recovery.
21. Data may be lost due to unexpected or accidental power loss during write operation.

NOTE TO USERS

While every effort has been made to ensure that the information provided herein is correct please feel free to notify us in the event of an error or inconsistency.

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Further Hitachi reserves the right to revise this publication and to make changes from time to time in the content hereof without obligation to notify any person of such revisions or changes.

1.0 General

1.1. Introduction

The Travelstar C4K60-60/40/30/20 disk drives reach high capacities in a 1.8 type form factor by applying the latest high-density recording technology.

Product name	Model name	Capacity (Formatted)	Height	Interface
Travelstar C4K60-60	HTC426060G9AT00	60.011 GB	9.5 mm	ATA-6(IDE)
Travelstar C4K60-40	HTC426040G9AT00	40.007 GB	9.5 mm	ATA-6(IDE)
Travelstar C4K60-30	HTC426030G7AT00	30.005 GB	7.0 mm	ATA-6(IDE)
Travelstar C4K60-20	HTC426020G7AT00	20.003 GB	7.0 mm	ATA-6(IDE)

[Features]

- GMR Head
- ID-less Format
- ME^{2}PRML Read Channel
- Data Transfer Rate
  (Host-Device)
  -16.6 MB/sec: PIO mode-4/Multiword DMA mode-2
  - 100 MB/sec: Ultra DMA mode-5
  (Device-Buffer)
  - 18.4 to 34.0 MB/s(60/30GB), 15.9 to 29.7 MB/sec(40/20GB)
- CDR (Constant Density Recording)
- On-the-fly ECC Correction
- Buffer: 2MB
- Read-ahead Cache/Write Cache
- Auto Read Reassign/Auto Write Reassign
- SMART
- Average Access Time 15 ms
- Embedded Sector Servo
- FDB(Fluid Dynamics Bearing) Motor
- Rotary Actuator
- Load/Unload Mechanism
- 62grams(60/40GB), 47 grams(30/20GB)
- Low Power Consumption: 0.25W at Idle mode, 0.08W at Standby mode (3.3V operation)
- Advanced Power Management(APM)
- Non-operating Shock: 11,760m/S^2(1200G, 1ms, half-sine wave)
- Operating Shock: 4,900m/S^2(500G, 2ms, half-sine wave)

[Identify Device Information for Setup]

Table 1.1 Identify Device information (Addressing)

Product name	Word 1 Number of CYL.	Word 3 Number of HD	Word 6 Number of SPT	Word 60 – 61 ***1** Word 100 - 103 Total LBA
HTC426060G9AT00	16383 ***2**	16	63	117,210,240
HTC426040G9AT00	16383 ***2**	16	63	78,140,160
HTC426030G7AT00	16383 ***2**	16	63	58,605,120
HTC426020G7AT00	16383 ***2**	16	63	39,070,080

***1 :** Words 60-61 reflect the total number of user addressable sectors in LBA mode.
***2 :** Maximum capacity in CHS mode is 8,455MB.

1.2. General Caution

Caution Adhere to the following cautions.

(a) Warranty void if Metal Head Disk Assembly (HDA) is opened, or any HDA seal/label is broken.
(b) Hot swapping (Power on) damages the drive. The drive should be swapped during Power Off only.
(c) Shock can result in permanent damage to the drive and/or loss of data.

Prevent shocks often incurred by dropping, knocking over, or hitting the drive.

Caution **PREVENT SHOCKS**

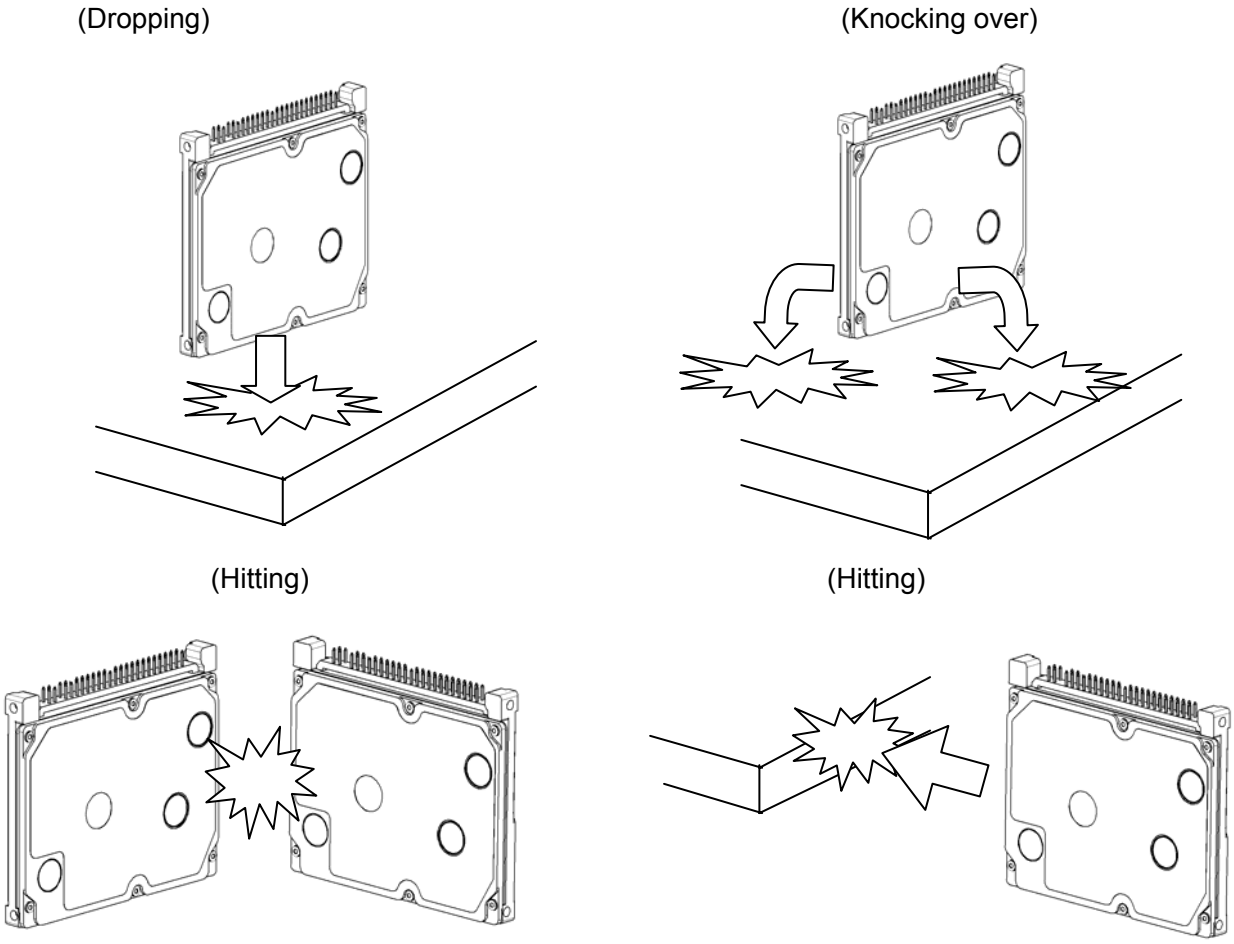


Figure 1.1

2.0 Components

Travelstar C4K60-60/4030/20 Disk Drive

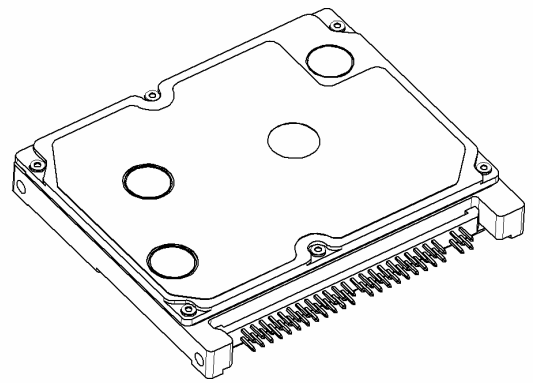


Figure 2.1 Overview of Travelstar C4K60-60/4030/20 (7.0mm height)

3.0 Specification Summary

3.1. Principal Specifications

Table 3.1 Principal Specifications

No.	Item		Specifications				Units
			Travelstar C4K60-60	**Travelstar C4K60-40**	**Travelstar C4K60-30**	**Travelstar C4K60-20**	
	Model name		HTC426060G9AT00	HTC426040G9AT00	HTC426030G7AT00	HTC426020G7AT00	
1	Capacity per drive (Formatted)		60.011	40.007	30.005	20.003	GB
	Capacity per sector		512				Bytes
	Disks		2		1		
	Heads		4	4	2	2	
2	Seek time (Nominal value)	Average	15 ***1**				ms
		Full stroke	26 ***1**				ms
		Track to track	3				ms
3	Average latency		7.1				ms
	Disk rotational speed		4,200				RPM
4	Recording density (Max.)		32.8 (832)	28.1 (713)	32.8 (832)	28.1 (713)	Mbpm(kBPI)
	Track density		4.65 (118.0)	4.13 (105.0)	4.65 (118.0)	4.13 (105.0)	Mtpm(kTPI)
	Recording method		ME^2PRML, ID-Less format				
5	Interface		ATA-6(IDE)				
	Data transfer rate (Disk-Buffer)		18.4 - 34.0	15.9 – 29.7	18.4 - 34.0	15.9 – 29.7	MB/sec
	Data transfer rate (Host-Buffer)		Max. 16.6 (PIO mode 4/ Multiword DMA mode 2)				MB/sec
			Max. 100 (Ultra DMA mode 5)				MB/sec
	Buffer size		2,048				kB
6	Power on - Ready ***2**		5 (Typical) ***3**				sec
	Sleep/Standby - Ready ***2**		3 (Typical) ***3**				sec
7	Dimensions (W×H×D)		70×9.5×60		70×7.0×60		mm
	Weight (Approximate value)		62		47		grams
8	DC Power Requirements ***4**		5.0V±5% or 3.3V±5%, Ripple noise 100mvp-p				W
	Supply Voltage		5.0V / 3.3V				
	- Start up (Max.) ***5**		2.1 / 1.4				
	- Idle (Ave.) ***6**		0.38 / 0.25				
	- Active Idle (Ave.) ***7**		0.68 / 0.45				
	- Seek (Ave.) ***8**		1.7 / 1.1				
	- Read (Ave.) ***9**		1.5 / 1.0				
	- Write (Ave.) ***9**		1.7 / 1.1				
	- Standby (Ave.)		0.12 / 0.08				
	- Sleep (Ave.)		0.11 / 0.07				

***1** :Average time of seek is calculated under the following condition. (Read/Write ratio: Read only)
Average of 10,000 random seeks, Voltage 5.0V or 3.3V, Temperature 25°C.
Full stroke time of seek is calculated under the following condition.
Average of 1,000 full stroke seeks, Voltage 5.0V or 3.3V, Temperature 25°C.
This maximum time is not included the seek time by seek retry.

***2** :Periodically, during start up, the drive may perform a spin up retry operation. When this operation occurs, the start up sound will change slightly and the ready timing will also be altered from typical time.

***3** :Power on to Ready time could take up to 10 seconds in case of spin up retries under certain conditions of the voltage specifications(Table 3.1) and environmental specifications(Table 3.2).

***4** :For DC power input, the average current is measured at the connector of the PCBA of this drive and in the nominal condition in which the power voltage and the temperature are 5.0V or 3.3V and 25°C, respectively. The DC power input has to be burst free (common mode). The average current may have some tolerance after power-on. The current measurement is recommended at 5 minutes later after power-on.

Caution Voltage rise time 5 - 100 ms at power on is required for power supply. The power supply voltage must not be under -0.3V at power off.

Caution This product is required over current protection for possible combustion due to circuit or component failure. Secondary over current protection shall be prepared by the system. The requirement of the current limitation is max. 10 A for the protection.

***5** :10ms averaged peak. For more information, refer to Section 6.1.

***6** :This value is at Low Power Idle mode. The heads are unloaded.

***7** :Power mode automatically enters to Active Idle mode after Read/Write operation.

***8** : Measured during random seek at the rate of three seeks per 100 msec.

***9** :Measured while reading or writing 16 sectors of data located on the same track.

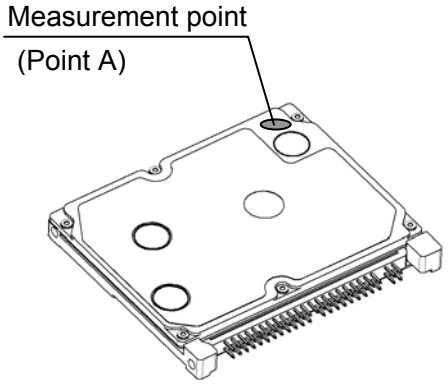
3.2. Environmental Specifications and Reliability

Table 3.2 Environmental Specification and Reliability

No.	Item		Specification			
			Travelstar C4K60-60	**Travelstar C4K60-40**	**Travelstar C4K60-30**	**Travelstar C4K60-20**
	Model name		HTC426060G9AT00	HTC426040G9AT00	HTC426030G7AT00	HTC426020G7AT00
1	Ambient ***1** temperature	Operational	5 to 60°C			
		Non-operational	-40 to 70°C			
	Temperature gradient		Max. 20°C /hour			
2	Relative humidity	Operational	5 to 90 %			
		Non-operational	5 to 95 %			
	Maximum wet bulb	Operational	29°C (without condensation)			
		Non-operational	40°C (without condensation) ***2**			
3	Vibration	Operational	1.0mm p-p or less (5 - 22Hz) 9.8 m/s^2 (1.0G) or less m/s^2 (22 – 500Hz)			
		Non-operational	5mm p-p or less (5 – 22Hz) 49m/s^2(5G) or less (22 – 500Hz)			
4	Shock ***5**	Operational	4,900m/s^2 (500G) or less (2 ms, half sine wave)			
		Non-operational	11,760m/s^2 (1200G) or less (1 ms, half sine wave)			
5	Atmospheric condition		Without corrosive vapors, salt or organic-metal compound. (ex. organic silicon, organic tin)			
6	Acoustic-noise ***3**	Idle(Typ.)	1.8Bels		1.6 Bels	
		seek(Typ.)	2.4 Bels		2.2 Bels	
7	Height (Altitude)	Operational	3,000m or less			
		Non-operational	12,000m or less			
	Height gradient		Max. 300m/min.(3.1kpa/min.)			
8	Data reliability (with retries and ECC)		Less than 1 non-recoverable error in 10 E 13 bits read ***4**			
9	External magnetic field		1,500 micro Tesla (DC) or less			

***1**: Ambient temperature should be measured at point 10 mm away from the nameplate of the drive. If the maximum operational ambient temperature cannot be measured at a point 10 mm away from the nameplate, a substitution method is stipulated in the table below.

Ambient temperature	Temperature at cover (Point A)
60°C	65°C
5°C	5°C



***2**: In case of the maximum wet bulb 40°C , the drive should be packed in HDD package box with ESD bag and desiccant. Please see specification 5.1 Packing for reference. If the drive is not packed in the HDD package box with ESD bag and desiccant, maximum wet bulb 29°C is applied.

***3** : 3.0 Bels are the maximum sound power levels with A-weighted. This value is specified at product

shipment, except during power on, load, unload or power down. Clicking noise of magnet latch operation occurs at loading and unloading operation of the magnetic heads. Also, the clicking noise of the magnet latch occurs at emergency unloading operations. Measurements are to be taken in accordance with ISO 7779. At seek mode, randomly select a cylinder and seek operation of the actuator with a delay time at each cylinder. Seek rate for the drive can be calculated as shown below.
Seek rate = 0.4/(average access time + average latency) = 0.4/(average access time + 60/RPM/2)

***4** :

Caution Data reliability is not to be used to compromise the host system data backup.

***5** :These shock specifications are defined for each axis. For non-operating rotational shock, the specification is 50K radian/sec^2 or less (2 ms, half sine wave).

3.3. Drive Usage Condition Specifications

The drive is designed for usage under the following conditions. Since reliability and product life depends on usage conditions, please consult our sales representatives or application engineers if the drive may be operated outside these conditions.

-Power on hours (POH) : Less than 333 hours/month
POH includes Sleep and Standby modes. The heads are unloaded during Power off, Standby, Sleep or Low Power Idle modes. The spindle motor is stopped during Standby and Sleep modes. This drive is not designed or intended to be used for 24/7 applications. Continuous motor spinning should be limited to 48 hours period. In case of continuous POH condition, the transition to Standby mode or Sleep mode must occur at least once every 48 hours period.

-Operating (Seek/Write Read operations) : Less than 20% of POH

-Motor Start/Stop Count : Max. 300,000 times. This number includes Standby, Sleep and power-on/off count.

-Environment : Within environmental specifications given in Table 3.2

-Power Requirement : Within DC power requirement specifications given in Table 3.1 “Principal Specifications”

-Drive Grounding : Drive frame should be grounded to system ground with four screws electrically. Grounding noise should be less than 500mVp-p. The grounding noise should be measured between electrical ground and system frame ground without the drive. Grounding AC current (measuring between two of side mounting holes) should be less than 50 mAp-p (Frequency Range: less than 12MHz). The grounding current should be measured through 50 ohm resistor.

-External Magnetic Field : Within specifications given in Table 3.2

-Mounting : Mount with recommended screws and regular torque.

-Physical/Electrical Interface: ATA-6

-Handling : Do not add Electrical Static Discharge, and Vibration and Shock to the drive. Do not press top cover and bottom PCBA surface of the drive.

3.4. Load/Unload Specifications

Load /Unload is a mechanism to load/unload the heads on the disk surfaces.

3.4.1. Normal Load/Unload

Normal load/unload operations are limited to maximum 600,000 times during HDD life. The normal unload operation is performed by the following commands.

- Standby
- Standby Immediate
- Sleep

Also, the normal unload is automatically performed by control software, during Idle mode. The above normal unload time does not include an emergency unload as explained in Sec. 3.4.2.

3.4.2. Emergency Unload

The emergency unload is occurred by unexpected power down, and is limited to maximum 20,000 times during HDD life. Since normal unload can not be performed by the software control after power off, the heads are unloaded by a hardware control. The maximum number of emergency unload is defined separately.

3.4.3. Required Power Off Sequence

To operate the load/unload normally, the following BIOS sequence is required by Host system before power off.

[Sequence #1]: Execute one of following commands.

- Standby
- Standby Immediate
- Sleep

Note: Such as Soft Reset, Flush Cache command or Check Power Mode command does not unload the heads.

[Sequence #2]: Check the Status Register, and wait the command complete.

Note: The head is unload by the sequence #1 command, and the command completion normally takes about 1sec. Considering the error retries, BIOS timer should be set to over 30 sec by the Host side.

[Sequence #3]: Power off the drive

Above sequence is required for the Host system at Power off, Suspend and Hibernation operations.

4.0 Installation

4.1. Installation Direction

The Travelstar C4K60-60/4030/20 can be installed in the 6 directions as shown below.

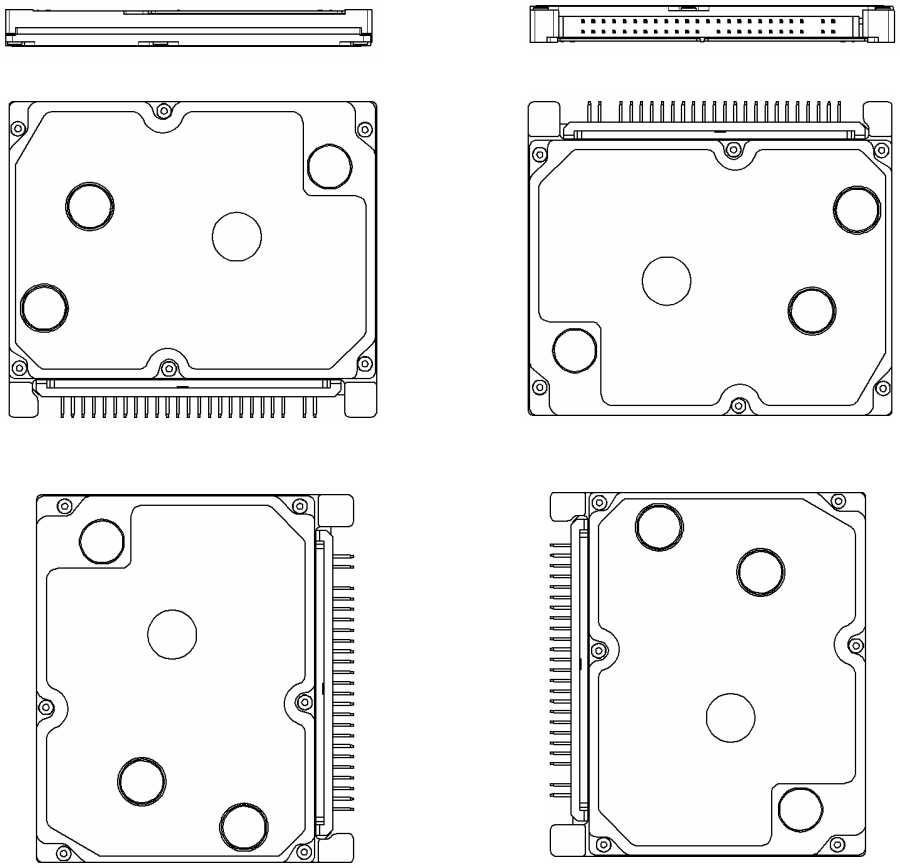


Figure 4.1 Installation

4.2. Mounting HDD

4.2.1. Mounting HDD with screws

Caution Mount the HDD with the screws according to the following instruction to optimize the performance.

(a) Mount the HDD with M2.5 screws. Take care not to add any distorting force to the HDD when mounting. Using 4 screws holes, secure the HDD.

(b) Use screws with the following specifications when the HDD is mounted.

i) M2.5 (screw engagement of 2.8mm max. However, do not use both bottom and side screw hole at the same position simultaneously.)

ii) The torque for fixing the screws is 2.5±0.5kgcm(2.2±0.4 lb. inch)

(c) Consider an appropriate cooling to keep the temperature of center of HDD top cover less than 65°C.

(d) The inertia of the chassis around the Z-axis of the gravity center of the device must be more than 3×10^{-4} kg m^2.

Note) In case of general Sub-Notebook PC(Weight: 1.7kg), the inertia of the chassis around the Z-axis of the gravity center of the device is greater than 100×10^{-4} kg m^2. Therefore, the required inertia level has no problem with the general electronic equipment.

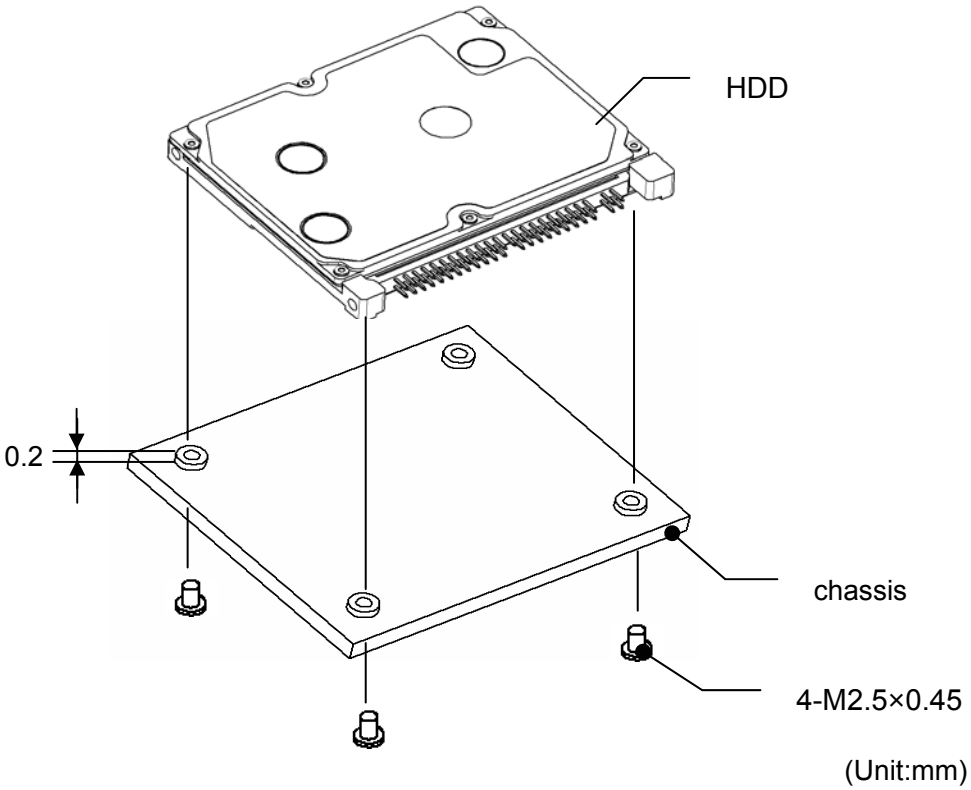


Figure 4-2 Mounting the HDD

4.2.2. Single HDD Test Condition

To optimize the performance, keep the following instructions.

1) For the Single HDD test, HDD should be placed on an ABS-sheet. HDD should be place with no movement by external force min. 0.25N for X axis and Y-axis directions.
2) Don't place HDD on a soft sponge sheet or hard surface at HDD test. If the HDD is placed on the soft sponge sheet or slippery hard desk surface, the HDD has unstable conditions such as HDD self-vibration at seek operations or spindle motor rotation. It may cause performance reduction or some errors. Also, HDD floating by tension of I/F cabling may cause the similar symptom. The HDD should be placed without any floating. Don't test the HDD under these unstable conditions.
3) If the HDD cannot be fixed by the required holding torque above item 1), put a body weight on the HDD as shown in Figure 4-3. The body weight is provided for preventing the HDD movement or HDD floating by tension of I/F cabling.

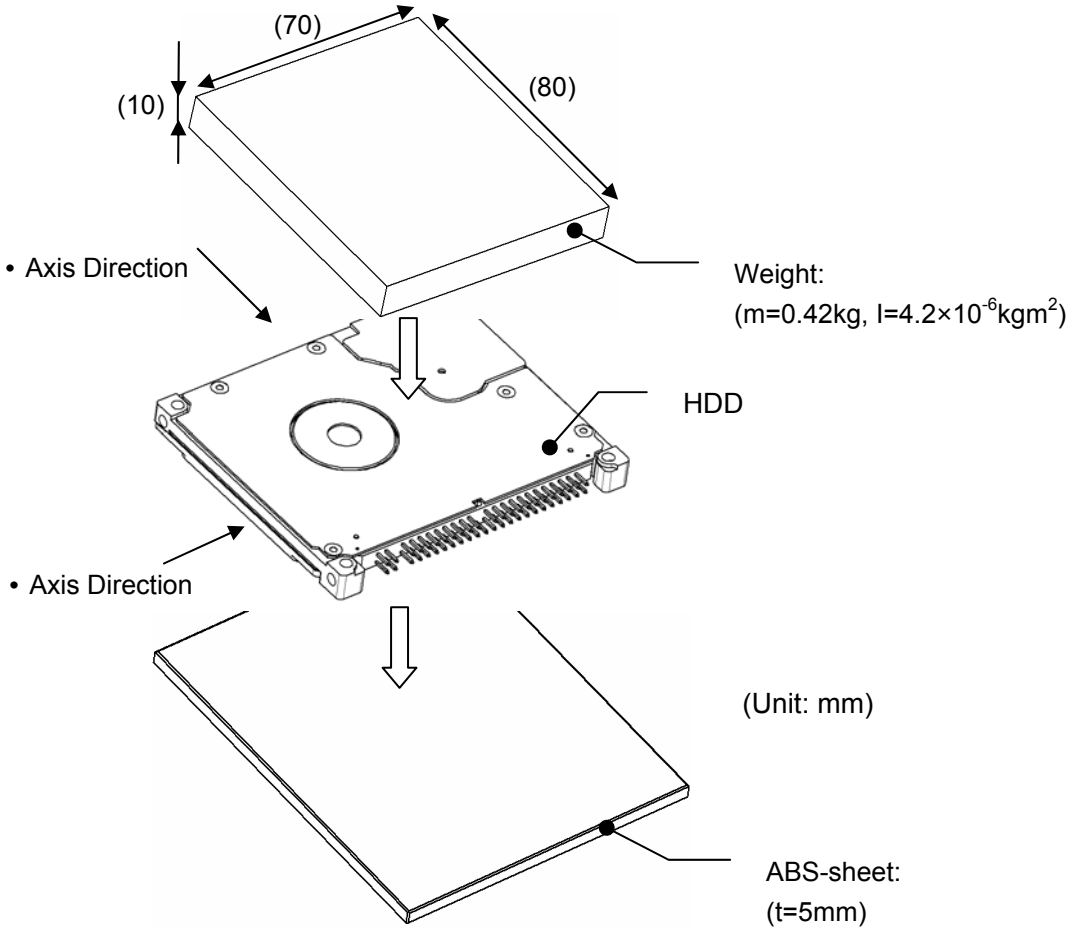


Figure 4.3 Single HDD Test Condition

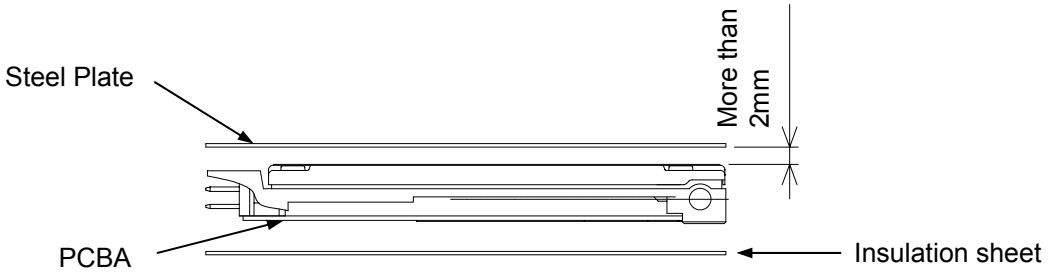
4.2.3. Attention for HDD Installation

Caution

(1) In case of steel plate installation on HDD cover side, the spacing between HDD cover and steel plate should be kept more than 2 mm. If this spacing is not kept for the steel plate, it may affect Load/Unload mechanism.

(2) The PCBA side of the drive should be covered with insulation sheet if the active metal of host system may contact to the PCBA of the drive. If the insulation sheet is not provided for the possible contact of the live metal, failures may occur.

(3) Do not push the bottom PCBA. It may cause catastrophic failures.

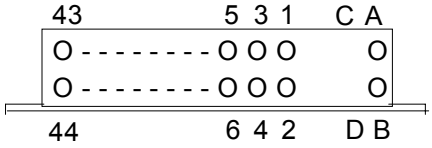


4.3. Device Address Setting (DRIVE 0/DRIVE 1)

When the device is connected to the host bus, Device address setting is necessary to configure a device as DRIVE 0 or DRIVE 1. The device address setting is established between drives on the interface connector by using jumper 0-2 (pin # A, B, D)

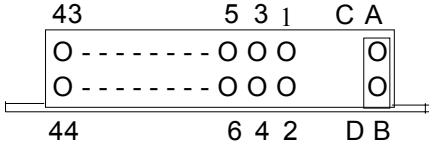
The DRIVE 0 is assigned to device address 0, and the DRIVE 1 is assigned to device address 1.

1) DRIVE 0 (or single)



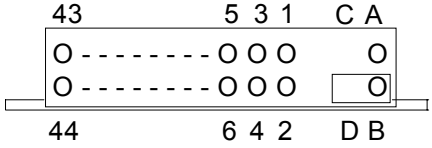
If all of pins A,B, D are open, the drive is DRIVE 0(or single).

2) DRIVE 1



If jumper Position A-B is used, the drive is DRIVE 1.

3) CSEL Selection



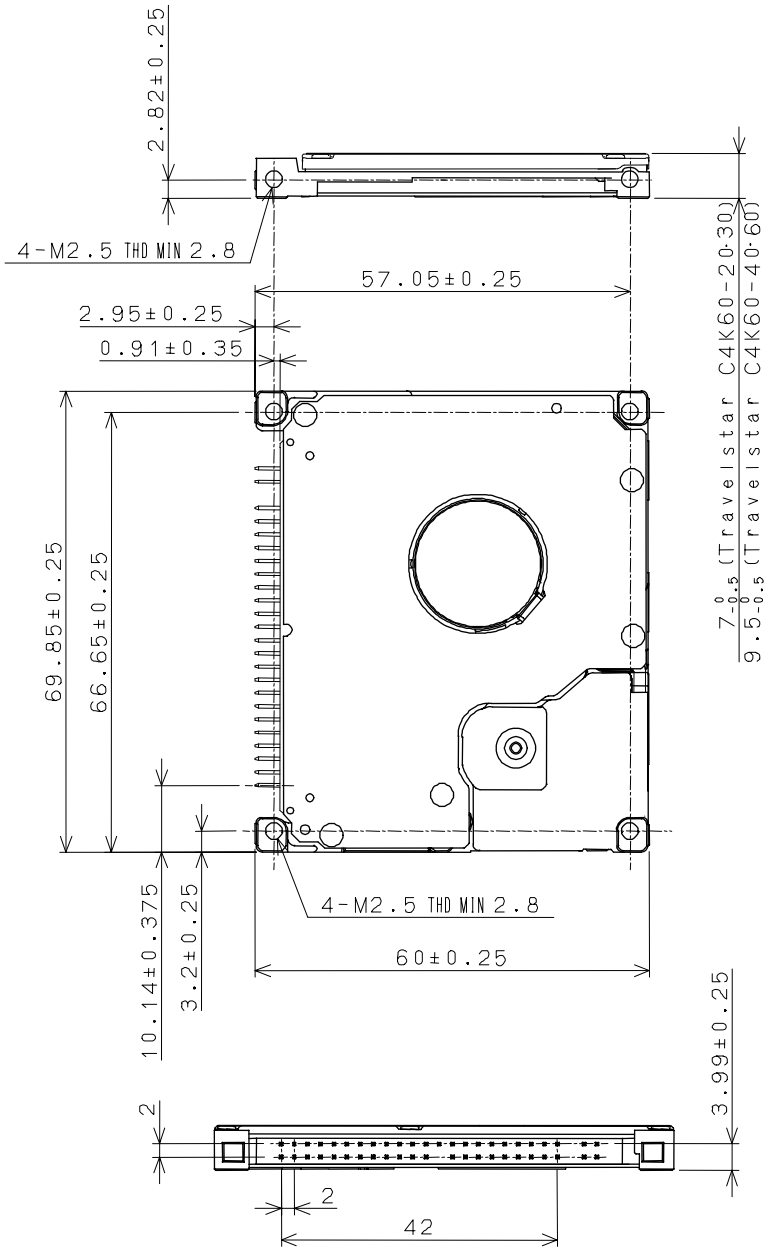
If jumper Position B-D is used, DRIVE 0 or DRIVE 1 setting is determined by the condition of CSEL signal (pin# 28).

(Recommended type of jumper socket)

Vender: IRISO ELECTRONICS CO., LTD.

Vender Part Number: 9721HJ-GF

4.4. Dimensions



(Unit : mm)

Figure 4.4 Dimensions

5.0 Packing and Handling

5.1. Packing

Caution When you package the device, clean it and execute the following procedures to prevent humidity and handling damage and contamination.

(1) Pack the device in an ESD protective bag with desiccant.
(2) Use the original Hitachi cardboard box and the cushioning materials or equivalent cushioning structures to surround the above bag.
(3) Never stack or package drives next to each other with at the proper cushion material separating them.
(4) Indicate which side is upside or downside on the exterior of the package box and attach notes requesting careful treatment and preventing the box from being turned upside down.
(5) Prevent excessive pressure from being applied on the top and bottom of the drive(top cover and PCBA side) when packing, unpacking, and transporting.
(6) Remember, mishandling of a drive can void the drive's warranty.
(7) Packing materials, i.e. ESD protective bag, cardboard box, cushion, etc., should not contain corrosive vapors, salt or organic-metal compound. (ex. organic silicon, organic tin)

Caution Prevent humidity when the drive is packed in a box.

5.2. Handling

Caution Mount the HDD with the screws according to the following instructions to optimize the performance.

It is necessary to prevent vibration, shock, and static electricity to the drive because it will damage the precision parts. In particular, prevent vibration or shock generated by dropping, knocking over, or hitting the drive. Also, avoid touching the electrical components directly, which can discharge electrostatic energy and damage the drive.

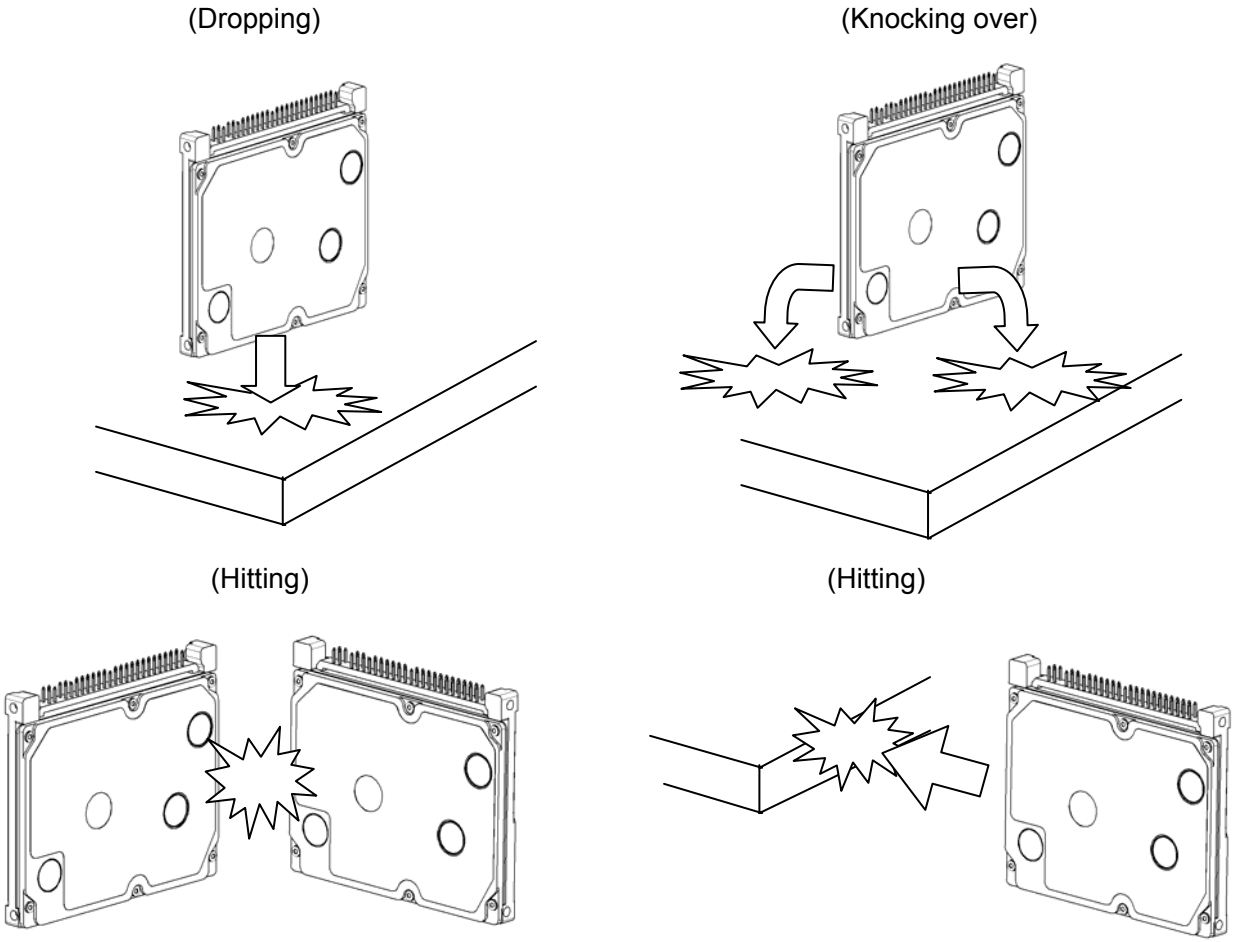
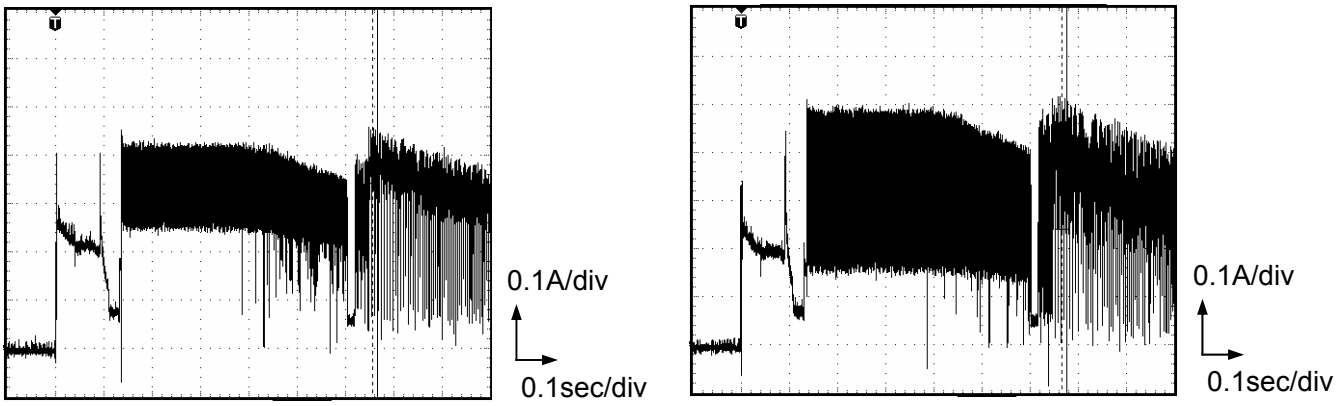


Figure 5.1

6.0 Physical Interface

6.1. Power Interface

Figures 6.1 shows typical power current transitions after turning on the power.



Supply voltage : 3.3V

Supply Voltage : 5.0V

Figure 6.1 Power Current Transition

6.2. Physical Interface

6.2.1. Connector

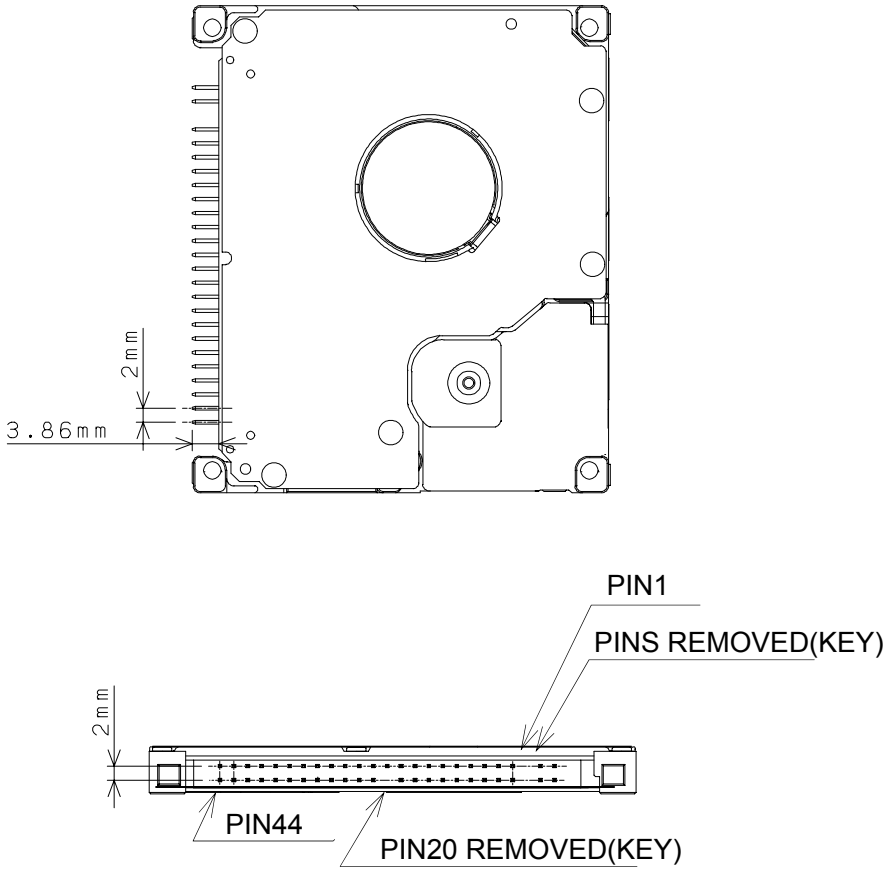
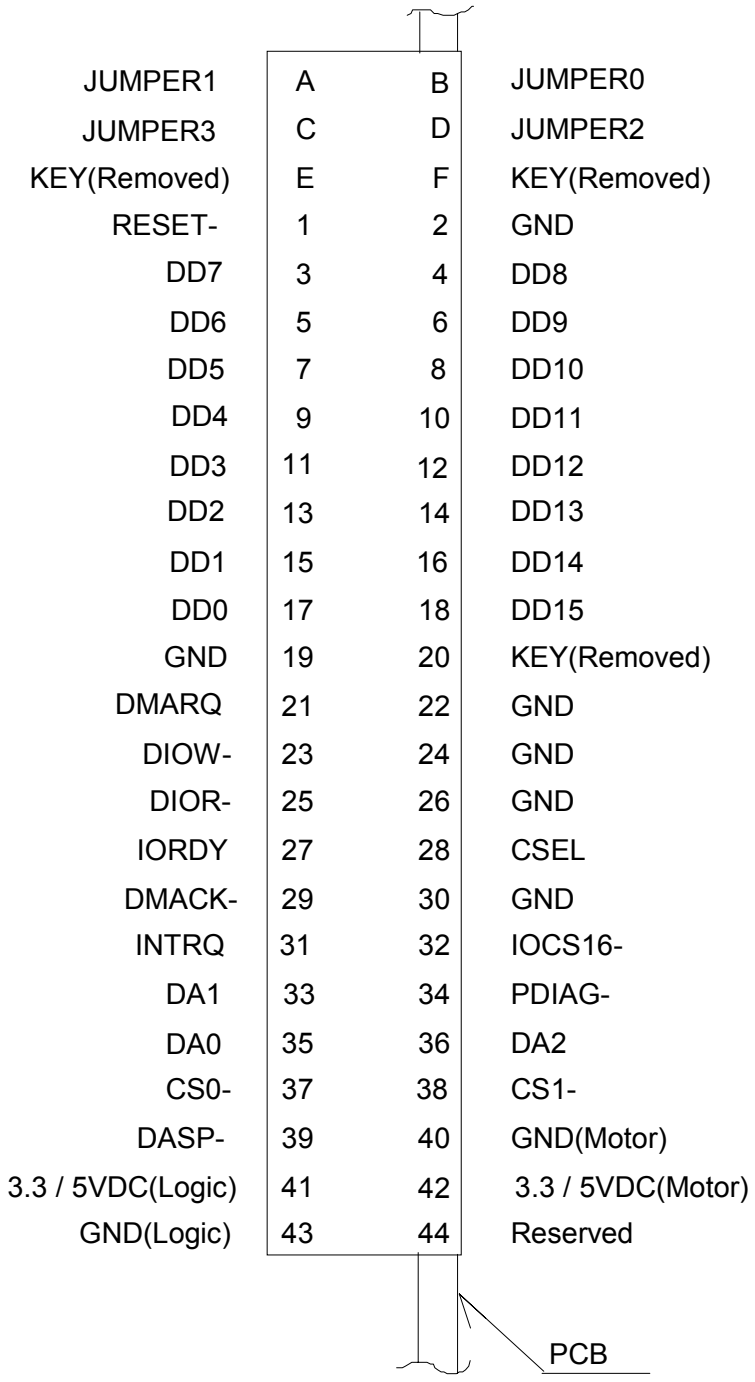


Figure 6.2 Connector Location

Table 6.1 Recommended socket connector

Drive interface connector	Recommended socket connector
DDK : KKS-PD50A-R23-FG or equivalent	DDK : KKS-RTS44-342N or equivalent

6.2.2. Connector Pin Assignment



6.2.3. Description of the Interface Signals

The interface is an ATA(IDE) interface. Reserved pins should be left unconnected. The signal names and the pin numbers are shown in Table 6.2. Table 6.2 shows signal definitions.
"I" of I/O type represents an input signal from the device and "O" represents an output signal from the device.

Table 6.2 Signal List(1/3)

Signal name	Pin	I/O type	Description
RESET-	1	I	This is a reset signal output from the host system and to be used for interface logic circuit.
DD0-DD15	3-18	I/O	This is a 16-bit bi-directional data bus. The lower 8 bits are used for register access other than data register.
DIOW-	23	I	The rising edge of this Write Strobe signal clocks data from the host data bus into a register on the device.
STOP ***1**			Assertion of this signal by the host during an Ultra DMA burst signals the termination of the Ultra DMA burst.
DIOR-	25	I	Activating this Read Strobe signal enables data from a register on the device to be clocked onto the host data bus. The rising edge of this signal latches data at the host.
HDMARDY- ***1**			This signal is a flow control signal for Ultra DMA Read. Host asserts this signal, and indicates that the host is ready to receive Ultra DMA Read data .
HSTROBE ***1**			This signal is Write data strobe signal from the host for an Ultra DMA Write. Both the rising and falling edge latch the data from DD(15:0) into the device.
IORDY	27	O	This signal is used to temporarily stop the host register access (read or write) when the device is not ready to respond to a data transfer request.
DDMARDY- ***1**			This signal is a flow control signal for Ultra DMA Write. Device asserts this signal, and indicates that the device is ready to receive Ultra DMA Write data .
DSTROBE ***1**			This signal is the data in strobe signal from the device for an Ultra DMA Read. Both the rising and falling edge latch the data from DD(15:0) into the host.

***1**: Signal name in Ultra DMA mode

Table 6.2 Signal List(2/3)

Signal name	Pin	I/O type	Description
CSEL	28	I	This signal is used to configure a device as either DRIVE 0 or DRIVE1 when CSEL mode is selected. This signal is pulled up inside the drive.
INTRQ	31	O	This is an interrupt signal for the host system. This signal is asserted by a selected device when the nIEN bit in the Device Control Register is "0". In other cases, this signal should be a high impedance state.
IOCS16-	32	O	This signal indicates to the host that the 16-bit data port has been addressed and a 16-bit word can be read or written to the device.
DA0-2	33,35,36	I	This is a register address signal from the host system.
PDIAG-:CBLID- ***2**	34	I/O	The PDIAG- signal is asserted by Device 1 to indicate to Device 0 that it has completed diagnostics. This signal is pulled up inside the device. The host may sample CBLID- after a power-on or hardware reset in order to detect the presence or absence of an 80-conductor cable assembly by performing the following steps: a) The host shall wait until the power on or hardware reset sequence is complete for all devices on the cable; b) If Device 1 is present, the host should issue IDENTIFY DEVICE or IDENTIFY PACKET DEVICE and use the returned data to determine that Device 1 is compliant with ATA-3 or subsequent standards. Any device compliant with ATA-3 or subsequent standards releases PDIAG- no later than after the first command following a power on or hardware reset sequence. If the host detects that CBLID- is connected to ground, an 80-conductor cable assembly is installed in the system. If the host detects that this signal is not connected to ground, an 80-conductor cable assembly is not installed in the system.
CS0-	37	I	This device chip selection signal is used to select the Command Block Registers from the host system.
CS1-	38	I	This device chip selection signal is used to select the Control Block Registers from the host system.

***2**: PDIAG-:CBLID- (Passed diagnostics: Cable assembly type identifier

Table 6.2 Signal List(3/3)

Signal name	Pin	I/O type	Description
DASP-	39	I/O	This signal indicates that a device is active or that Drive 1 is present when the power is turned on. Upon receipt of a command from the host, the device asserts this signal. At command completion, the device de-asserts this signal.
DMARQ	21	O	The device shall assert this signal, used for DMA data transfers between host and device, when it is ready to transfer data.
DMACK-	29	I	The host in response to DMARQ to either acknowledge that data has been accepted, or that data is available shall use this signal.
JUMPER0,1,2	PIN-A,B,D	-	See Sec. 4.3 " Drive Address Setting (Drive 0/Drive 1)" for the detail.

The I/O signal levels are as follows.

(1) Input signal High level +2.0V to Vcc+0.5V
Low level −0.5V to +0.8V

(2) Output signal High level +2.4V to +5.25V or an open circuit
Low level +0.4V or less (IOL=2mA), +0.5V or less (IOL=12mA)

Note) The I/F cable should be no longer than 50cm(20 inches) including the circuit pattern length in the host system. If the cable length is not within this specification, it may cause factional degradations or some errors.

7.0 Logical Interface

7.1. I/O Registers

Communication between the host system and the device is done through I/O registers. The Command Block Registers are used for sending commands to the device or posting device status. The Control Block Registers are used for controlling the device or posting device status.

Table 7.1 Register List

Addresses					Functions	
CS0-	CS1-	DA2	DA1	DA0	READ(DIOR-)	WRITE(DIOW-)
Command Block Registers						
0	1	0	0	0	Data	Data
0	1	0	0	1	Error	Features
0	1	0	1	0	Sector Count	Sector Count
0	1	0	1	1	LBA Low (Sector Number)	LBA Low (Sector Number)
0	1	1	0	0	LBA Mid (Cylinder Low)	LBA Mid (Cylinder Low)
0	1	1	0	1	LBA High (Cylinder High)	LBA High (Cylinder High)
0	1	1	1	0	Device/Head	Device/Head
0	1	1	1	1	Status	Command
Control Block Registers						
1	0	1	1	0	Alt. Status	Device Control
Invalid or Not Used						
0	0	×	×	×	Invalid address	
0	1	×	×	×	Data bus high impedance (not used)	
1	0	0	×	×	Data bus high impedance (not used)	
1	0	1	0	×	Data bus high impedance (not used)	

'0' is low signal level. '1' is high signal level.

7.1.1. Data register

A 16-bit register to be used for transferring data blocks between the HDD's data buffer and the host.

7.1.2. Error register

This register stores device status when the last command has been completed or diagnostic codes when a self-diagnostic process has been completed. The contents of this register are valid when the error bit (ERR) is set in the Status Register. The contents of this register are diagnostic codes when the device has just completed a self-diagnostic process requested when turning on the power or resetting.

Bit	7	6	5	4	3	2	1	0
Name	ICRC	UNC	0	IDNF	0	ABRT	0	AMNF

- AMNF(Address Mark Not Found):
  This bit indicates that the device is unable to execute SMART command due to a invalid data structure.
- ABRT(Aborted Command):
  This bit indicates that execution of a command is interrupted due to a device error(e.g. Not Ready and Write fault) or an invalid command code.
- IDNF (ID Not Found):
  This bit indicates that an ID field of the requested sector is not found.
- UNC(Uncorrectable Data Error):
  This bit indicates that an uncorrectable error or an data address mark not found has occurred.
- ICRC(Interface CRC Error): This bit indicates that an interface CRC error was occurred. This bit is not applied for Multiword DMA transfers.

7.1.3. Features Register

By combining with the Set Features command, this register is used for enabling or disabling each feature.

7.1.4. Sector Count Register

The register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the device. If value in the register is set to 0, a count of 256 sectors in 28-bit addressing or 65,536 sectors in 48-bit addressing is specified.

When a command has been completed and the value of this register is "0", it represents that the command has been executed successfully. If the command has not been executed successfully, this register indicates the number of the sectors yet to be processed. This definition cannot be applied to all commands. For more information on commands, refer to the corresponding sections.

7.1.5. LBA Low Register (Sector Number Register)

This register in CHS mode contains the starting sector number for any disk data access. This number may be from 1 to the maximum number of sectors per track. In LBA mode and 28-bit addressing, the register contains bits 7-0 of the LBA address. When 48-bit addressing commands are used, the most recently written content contains "LBA bits 7-0", and the previous content contains LBA bits 31-24. The contents of the register are defined otherwise on some commands. These definitions are given in the command descriptions.

7.1.6. LBA Mid Register (Cylinder Low Register)

This register in CHS mode contains the lower 8 bits of the starting cylinder address for any disk access. In LBA mode and 28-bit addressing, the register contains bits 15-8 of the LBA address. When 48-bit addressing commands are used, the most recently written content contains "LBA bits 15-8", and the previous content contains LBA bits 39-32. The contents of the register are defined otherwise on some commands. These definitions are given in the command descriptions.

7.1.7. LBA High Register (Cylinder High Register)

This register in CHS mode contains the higher 8 bits of the starting cylinder address for any disk access. In LBA mode and 28-bit addressing, the register contains bits 23-16 of the LBA address. When 48-bit addressing commands are used, the most recently written content contains "LBA bits 23-16", and the previous content contains LBA bits 47-40. The contents of the register are defined otherwise on some commands. These definitions are given in the command descriptions.

7.1.8. Device/Head Register

This register has the binary coded address of device and head selected. The head numbers begins with "0".

Bit	7	6	5	4	3	2	1	0
Name	-	L	-	DRV	HS3	HS2	HS1	HS0

- Bits HS3 to HS0 are head addresses to be selected. HS3 is the highest bit. The address of the currently selected head is displayed in this register when a command is completed. In case of LBA mode and 28-bit addressing mode, these bits HS3 to HS0 are applied to LBA bits 27 - 24.
- DRV is a device selection bit. 0=DEVICE 0, 1=DEVICE 1
- L is the sector address mode select:
  0=CHS mode, 1= LBA mode (28-bit addressing or 48-bit addressing)

7.1.9. Status Register

The current device status is reflected in this register. The contents are updated at the completion of each command. If BSY=1, no other bits in this register are valid. When BSY is cleared, the other bits in this register is valid within 400 ns. If the host reads this register when an interrupt is pending, it is considered to be the interrupt acknowledge, and the pending interrupt is then cleared.

Bit	7	6	5	4	3	2	1	0
Name	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

- ERR (Error):
  This bit indicates that an error occurs during the execution of a command.
  For more information, refer to the description of the Error register.
- IDX (Index):
  This bit is set once per disk revolution.
- CORR (Corrected Data):
  This bit reports always "1"
- DRQ (Data Request):
  This bit indicates that the device is ready to transfer data between the host and the device.
- DSC (Device Seek Complete):
  This bit indicates that the device head is located on the specified track.
  If an error has occurred, the value of this bit is not changed until the host reads the Status register.
- DFW (Device Write Fault):
  This bit indicates that an error has occurred during a Write operation.
  If an error has occurred, the value of this bit is not changed until the host reads the Status register.
- DRDY (Device Ready):
  This bit indicates that the device is ready to respond any command. If an error has occurred, the value of this bit is not changed until the host reads the Status register. This bit is cleared when the power is turned on and then kept cleared until the device gets ready to accept any command.
- BSY (Busy):
  This bit is specified when the device accesses the Command Block Registers. When BSY is 1,the host cannot access the Command Block Registers. If the Command Block Registers are read when BSY is "1", all contents of the Status Register are returned.

7.1.10. Command Register

The command code is sent to this register. After it is written, execution begins.

7.1.11. Alternate Status Register

The information in this register is a duplicate of that in the Status Register.
Reading this register will not clear the interrupt.

7.1.12. Device Control Register

Bit	7	6	5	4	3	2	1	0
Name	HOB	-	-	-	-	SRST	nIEN	'0'

- HOB (High Order Byte):
  This bit is defined by 48-bit addressing feature:
  HOB = 1: The host can read the previous content of the Features, Sector Count, LBA Low, LBA Mid, and LBA High Registers.
  HOB = 0: The host can read the most recently written content of the above registers.
  The device clears HOB bit to zero by a write to any command block register.
- nIEN(Interrupt Enable):
  If the device is selected when nIEN is 0, the INTRQ signal is enabled. When nIEN is 1 or when the device is not selected, the INTRQ signal is in a high impedance state.
- SRST (Software Reset):
  When this bit is set, the device is reset. When this bit is cleared, the device exits from the reset state. When two devices are connected through one line in the daisy chain mode, they are reset simultaneously.

7.2. General Operations

7.2.1. 48-bit Addressing Feature Set

The 48-bit Addressing Feature set allows device with capacities up to 281,474,976,710.655 sectors (144,115,188,075,855,360 bytes). In addition, the number of sectors that may be transferred by a single command are increased by increasing the allowable sector count to 16-bits. Commands unique to the 48-bit Address feature set are:

- FLUSH CACHE EXT
- READ SECTORS EXT, READ MULTIPLE EXT, READ VERIFY SECTORS EXT, READ DMA EXT
- READ NATIVE MAX ADDRESS EXT
- SET MAX ADDRESS EXT
- WRITE DMA FUA EXT, WRITE MULTIPLE FUA EXT
- WRITE SECTOR EXT, WRITE MULTIPLE EXT, WRITE DMA EXT
- READ LOG EXT, WRITE LOG EXT

The 48-bit Address feature operates in LBA only. Device also implements commands set using 28-bit addressing. 28-bit and 48-bit commands may be intermixed.

In the device, the Features Register, the Sector Count Register, the LBA Low Register, the LBA Mid Register, and the LBA High Register are each a two byte deep FIFO. Each time one of these registers is written, the new content written is placed into the “most recently written” location and the previous content of the register is moved to “previous content” location.

The host may read the “previous content” of the Sector Count, LBA Low, LBA Mid, and LBA High Registers by first setting the High Order Bit (HOB, bit 7) of the Device Control register to one and then reading the desired register. If HOB (bit 7) in the Device Control register is cleared to zero the host reads the “most recently written” content when the register is read. A write to any Command Block register causes the device to clear the HOB bit to zero in the Device Control register. The “most recently written” content always gets written by a register write regardless of the state of HOB (bit 7) in the Device Control register.

Support of the 48-bit Address feature set is indicated in the IDENTIFY DEVICE command response bit 10 word 83. In addition, the maximum user LBA address accessible by 48-bit addressable commands is contained in Identify Device response words 100 through 103.

When the 48-bit Address feature set is implemented, the native maximum address is the value returned by a READ NATIVE MAX ADDRESS EXT command. If the native maximum address is equal to or less than 268,435,455, a READ NATIVE MAX ADDRESS command returns the native maximum address. If the native maximum address is greater than 268,435,455, a READ NATIVE MAX ADDRESS command returns a value of 268,435,455.

7.2.2. Power Management

Supported commands and functions:

- IDLE command, IDLE IMMEDIATA command
- SLEEP command
- STANDBY command, STANDBY IMMEDIATE command
- Advanced Power Management (APM)
- Standby Timer

7.2.2.1. Low power consumption modes

The drive supports the following low power consumption modes:

- Active mode:
  The spindle motor is rotated. Seek and Read/Write operations are activated.
- Active Idle mode:
  Heads are loaded, and kept on outer cylinder.
- Low Power Idle mode:
  Heads are unloaded outside of the disk platters and the spindle motor is rotating. This mode is lower power mode than Active Idle mode.
- Standby mode:
  State of ready to receive commands. State of ready to receive commands, but the spindle motor is stopped. If the device receive a command with seek operation, the spindle motor is rotated and the command is executed.
- Sleep mode:
  This mode is the lowest power mode. The spindle motor is stopped. The device can not receive the command except Hardware Reset and Software Reset.

Standby, Standby Immediate and Sleep commands are executed with the following process:

- Wait Write command completion
- Unload heads
- Clear BSY bit and enable INTRQ signal
- Stop the spindle motor
- Move to a low power mode

7.2.2.2. Standby Timer

Standby timer is provided for automatic power saving control. The device automatically moves to the Standby mode if the host does not issue a command within the timer period. The Standby timer is disabled at power-on. The Standby timer value is changeable using Idle and Standby commands. The timer can be set up to 30 minutes.

7.2.2.3. Advanced Power Management

The host can select the power saving control pattern by Advanced Power management (APM). The device performs an intelligent power saving control based on the selected pattern by host.

Using Set Feature command and Sector Count Register can set the APM operation mode. The Sector count value is related to the performance level and the power consumption level. If the Sector Counter value is set to 01h, the power consumption is getting better, but the performance is getting worse. If the large Sector Count Register is set to FEh, the performance is getting better sacrificing the power consumption. The device has five levels of APM operation mode (APM mode 0,1,2,3 and 4) depending on the Sector Counter values from 01h to FEh.

Using the following command, the APM control can be set the mode and reset the mode.

- Set Feature command, Enable Advanced Power Management sub-command.
  (Command Code = EFh, Features = 05h)
- Set Feature command, Disable Advanced Power Management sub-command.
  (Command Code = EFh, Features = 85h)

The Enable Advanced Power Management sub-command enables the APM operation set by the Sector Count Register. The Disable Advanced Power Management sub-command disables the APM operation. If the APM operation is disabled, the device performs APM mode 0.

Table 7.2 Low Power Consumption Mode Transition Time

Operation Mode	APM Value ***1**	Operation
APM Mode 0	C0h - FEh	Move to Low Power Idle mode
APM Mode 1	A0h – BFh	Move to Low Power Idle mode
APM Mode 2	80h – 9Fh	Move to Low Power Idle mode (Power on Default)
APM Mode 3	20h – 7Fh	Move to Standby mode ***2**
APM Mode 4	01h – 1Fh	

***1**: This value is set by Sector Count register of Enable Advanced power management sub-command. If non-defined values 00h and FFh are set, the device returns Aborted command.

***2**: APM function does not affect on the Standby timer value. The Standby timer and the Standby mode transition control of APM function is operated independently.

7.2.3. SMART Feature

The intent of self-monitoring, analysis, and reporting technology (SMART) is to protect user data and minimize the likelihood of unscheduled system downtime that may be caused by predictable degradation and/or fault of the device. By monitoring and storing critical performance and calibration parameters, SMART devices attempt to predict the likelihood of near-term degradation or fault condition. Providing the host system the knowledge of a negative reliability condition, allows the host system to warn the user of the impending risk of a data loss and advise the user of appropriate action. Support of this feature set is indicated in bit 0 of word 82 of the Identify Device response.

The SMART commands use a single command code and are differentiated by the value placed in the Features register. The commands supported by this feature set are:

- SMART ENABLE OPERATIONS command, SMART DISABLE OPERATIONS command
- SMART RETURN STATUS command
- SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE command
- SMART SAVE ATTRIBUTE VALUES command
- SMART ENABLE/DISABLE AUTOMATIC OFFLINE command
- SMART EXECUTE OFFLINE IMMEDIATE command
- SMART READ LOG SECTOR command, SMART WRITE LOG SECTOR command

7.2.3.1. Attribute Parameters

Attributes are the specific performance or calibration parameters that are used in analyzing the status of the device. Attributes are selected by the device manufacturer based on that attribute's ability to contribute to the prediction of degrading or fault conditions for that particular device. The specific set of attributes being used and the identity of these attributes is vendor specific and proprietary.

Attribute values are used to represent the relative reliability of individual performance or calibration attributes. Higher attribute values indicate that the analysis algorithms being used by the device are predicting a lower probability of a degrading or fault condition existing. Accordingly, lower attribute values indicate that the analysis algorithms being used by the device are predicting a higher probability of a degrading or fault condition existing.

Each attribute value has a corresponding attribute threshold limit that is used for direct comparison to the attribute value to indicate the existence of a degrading or fault condition. The device manufacturer through design and reliability testing and analysis determine the numerical values of the attribute thresholds. Each attribute threshold represents the lowest limit to which its corresponding attribute value can be equal while still retaining a positive reliability status. Attribute thresholds are set at the device manufacturer's factory and cannot be changed in the field. If one or more attribute values are less than or equal to their corresponding attribute thresholds, then the device reliability status indicates an impending degrading or fault condition.

7.2.3.2. SMART Device Error Log Reporting

The intent of SMART Device Error Log Reporting feature is to augment the SMART feature set to provide additional diagnostic information on device that have generated error conditions. The device retains a specified amount of previously executed commands, and write this data along with the time of a triggered error condition to the existing SMART Read Logging Sectors.

The errors that device reported are gathered at all times the device is powered on except that logging of errors when in reduced power modes “standby mode and sleep mode”. The last five errors that device reported are gathered in summary SMART error log, and The last 255 errors that device reported are gathered in comprehensive SMART error log. The summary SMART error log duplicates the five error entries in the comprehensive SMART error log. A host can deliver the error information using the SMART READ LOG SECTOR command. If SMART is disabled by the host, the device does not disable SMART device error log. Disabling SMART will only disable the delivering of error log information via the SMART READ LOG SECTOR command.

If a device receives a firmware modification, all error log data will be discarded and the device error count for the life of the device will be reset to zero by client software “Download Utility”.

7.2.3.3. SMART Operation with Power Management Modes

When used in a system that is utilizing the power management feature set, a SMART enabled device automatically saves its attribute values upon receipt of an IDLE IMMEDIATE, STANDBY IMMEDIATE, or SLEEP command. If the device has been set to utilize the standby timer, The device automatically perform a SMART SAVE ATTRIBUTE VALUES function prior to going from an Idle state to the Standby state.

7.2.3.4. SMART Function Default Setting

The device is shipped from the device manufacturer's factory with SMART feature disabled.
The system manufacturer or the applications shall enable SMART.

7.2.4. Security Mode Feature

The Security Mode feature set is a password system that restricts access to user data stored on a device. The system has two passwords, User and Master and two security levels, High and Maximum. The security system is enabled by sending a user password to the device with the SECURITY SET PASSWORD command. When the security system is enabled, access to user data on the device is denied after a power cycle until the User password is sent to the device with the SECURITY UNLOCK command.

A Master password may be set in a addition to the User password. The purpose of the Master password is to allow an administrator to establish a password that is kept secret from the user, and which may be used to unlock the device if the User password is lost. Setting the Master password does not enable the password system.

The security level is set to High or Maximum with the SECURITY SET PASSWORD command. The security level determines device behavior when the Master password is used to unlock the device. When the security level is set to High the device requires the SECURITY UNLOCK command and the Master password to unlock. When the security level is set to Maximum the device requires a SECURITY ERASE PREPARE command and a SECURITY ERASE UNIT command with the master password to unlock.

The SECURITY FREEZE LOCK command prevents changes to passwords until a following power cycle. The purpose of the SECURITY FREEZE LOCK command is to prevent password setting attacks on the security system.

The security mode features allow a host to implement a security password system to prevent unauthorized access to the internal disk device.

The commands supported by this feature set are:

- SECURITY SET PASSWORD command
- SECURITY UNLOCK command
- SECURITY ERASE PREPARE command
- SECURITY ERASE UNIT command
- SECURITY FREEZE LOCK command
- SECURITY DISABLE PASSWORD command

Support of the security mode feature set is indicated in Identify Device response Word 128.

7.2.4.1. Security Mode Default Setting

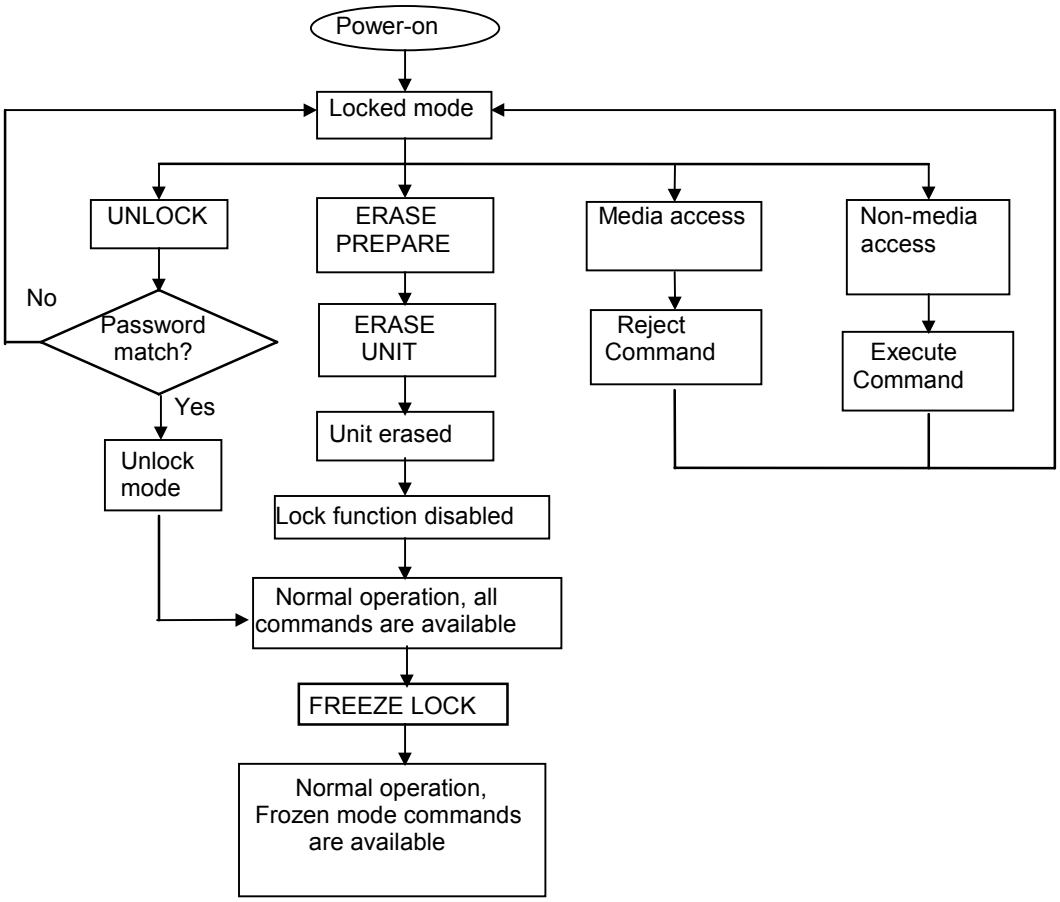
The device is shipped with the master password set to 20h value (ASCII space) and the lock function disabled. The system manufacturer/dealer may set a new master password using the SECURITY SET PASSWORD command, without enabling or disabling the lock function.

7.2.4.2. Initial Setting of the User Password

When a user password is set, the device automatically enters lock mode the next time the device is powered-on or hardware reset.

7.2.4.3. Security Mode Operation from Power-on or Hardware Reset

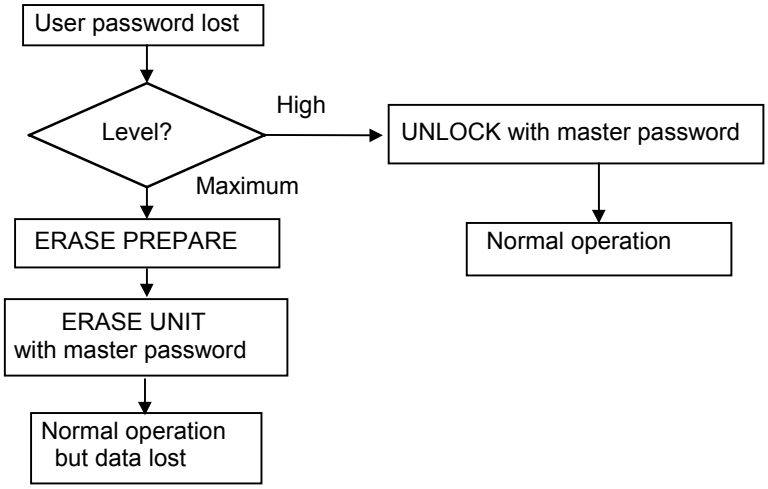
When lock is enabled, the device reject media access commands until a SECURITY UNLOCK command is successfully completed.



7.2.4.4. User Password Lost

If the user password is lost and High level security is set, the device does not allow the user to access data. The device is unlocked using the master password.

If the user password is lost and Maximum security level is set, data access is impossible. However, the device is unlocked using the SECURITY ERASE UNIT command with the master password to unlock the device and erase all user data.



7.2.4.5. Security Mode Command Action

The following table defines executable commands in each lock mode state.

Table 7.3 Command Table for Device Lock Operation

Command	Locked mode	Unlocked mode	Frozen mode
READ MAX ADDRESS, READ MAX ADDRESS EXT	Executable	Executable	Executable
SET MAX ADDRESS, SET MAX ADDRESS EXT	Aborted	Executable	Executable
SECURITY DISABLE PASSWORD SECURITY SET PASSWORD	Aborted	Executable	Aborted
SECURITY UNLOCK SECURITY ERASE PREPARE SECURITY ERASE UNIT	Executable	Executable	Aborted
SECURITY FREEZE LOCK	Aborted	Executable	Executable
SMART AUTOMATIC ENABLE/DISABLE OFFLINE SMART EXECUTE OFFLINE IMMEDIATE SMART DISABLE OPERATIONS SMART ENABLE/DISABLE AUTOSAVE SMART ENABLE OPERATIONS SMART RETURN STATUS SMART SAVE ATTRIBUTE VALUES SMART READ LOG SECTOR, SMART WRITE LOG SECTOR	Executable	Executable	Executable
RECALIBRATE, SEEK			
READ BUFFER, WRITE BUFFER			
INITIAL DEVICE PARAMETERS, IDENTIFY DEVICE EXECUTE DEVICE DIAGNOSTICS SET MULTIPLE MODE SET FEATURE			
IDLE, IDLE IMMEDIATE STANDBY, STANDBY IMMEDIATE SLEEP			
READ DMA, READ LONG, READ MULTIPLE READ SECTOR, READ VERIFY	Aborted	Executable	Executable
READ DMA EXT, READ MULTIPLE EXT, READ SECTOR EXT READ VERIFY SECTORS EXT READ LOG EXT			
WRITE DMA, WRITE LONG, FORMAT TRACK WRITE MULTIPLE, WRITE SECTOR, FLUSH CACHE			
WRITE DMA EXT, WRITE SECTORS EXT WRITE MULTIPLE EXT, FLUSH CACHE EXT WRITE DMA FUA EXT, WRITE MULTIPLE FUA EXT WRITE LOG EXT			
DEVICE CONFIGURATION FREEZE LOCK DEVICE CONFIGURATION IDENTIFY DEVICE CONFIGURATION SET DEVICE CONFIGURATION RESTORE			

7.2.5. Protected Area Feature

A reserved area for data storage outside the normal operating system is required for several specialized applications. Systems may wish to store configuration data or save memory to disk data in a location that operation system can not change. Following commands are defined in this feature.

- READ MAX ADDRESS command and SET MAX ADDRESS command for 28-bit addressing
- READ MAX ADDRESS EXT command and SET MAX ADDRESS EXT command for 48-bit addressing
- SET MAX SET PASSWORD command
- SET MAX LOCK command
- SET MAX FREEZE LOCK command
- SET MAX UNLOCK command

The READ NATIVE MAX ADDRESS or READ NATIVE MAX ADDRESS EXT command allows the host to determine the maximum native address space of the device even when a protected area has been allocated.

The SET MAX ADDRESS or SET MAX ADDRESS EXT command allows the host to redefine the maximum address of the user accessible address space. That is, when the SET MAX ADDRESS or SET MAX ADDRESS EXT command is issued with a maximum address less than the native maximum address, the device reduces the user accessible address space to the maximum specified by the command, providing a protected area above that maximum address. The SET MAX ADDRESS or SET MAX ADDRESS EXT command is immediately preceded by a READ NATIVE MAX ADDRESS or READ NATIVE MAX ADDRESS EXT command. After the SET MAX ADDRESS or SET MAX ADDRESS EXT command has been issued, the device reports only the reduced user address space in response to an IDENTIFY DEVICE command in words 60, 61, 100, 101, 102, and 103. Any read or write command to an address above the maximum address specified by the SET MAX ADDRESS or SET MAX ADDRESS EXT command causes command completion with the IDNF bit set to one and ERR set to one, or command aborted.

A volatility bit in the Sector Count register allows the host to specify if the maximum address set is preserved across power-on or hardware reset cycles. On power-on or hardware reset the device maximum address returns to the last non-volatile address setting regardless of subsequent volatile SET MAX ADDRESS or SET MAX ADDRESS EXT commands. If the SET MAX ADDRESS or SET MAX ADDRESS EXT command is issued with a value that exceeds the native maximum address command aborted is returned.

When the 48-bit Address feature set is implemented, the native maximum address is the value returned by a READ NATIVE MAX ADDRESS EXT command. If the native maximum address is equal to or less than 268,435,455, a READ NATIVE MAX ADDRESS command returns the native maximum address. If the native maximum address is greater than 268,435,455, a READ NATIVE MAX ADDRESS command returns a value of 268,435,455.

If a Protected Area has been created using the SET MAX ADDRESS command, all SET MAX ADDRESS EXT commands result in command aborted until the Protected Area is eliminated by use of the SET MAX ADDRESS command with the address value returned by the READ NATIVE MAX ADDRESS command.

If a Protected Area has been created using the SET MAX ADDRESS EXT command, all SET MAX ADDRESS commands result in command aborted until the Protected Area is eliminated by use of the SET MAX ADDRESS EXT command with the address value returned by the READ NATIVE MAX ADDRESS EXT command.

The SET MAX SET PASSWORD command allows the host to define the password to be used during the current power-on cycle. The password does not persist over a power cycle but does persist over a hardware or software reset. This password is not related to the password used for the Security Mode Feature set. When the password is set the device is in the Set Max Unlocked mode. The SET MAX LOCK command allows the host to disable the SET MAX commands (except SET MAX UNLOCK) until the next power cycle or the issuance and acceptance of the SET MAX UNLOCK command. When this command is accepted the device is in the Set max locked mode. The SET MAX UNLOCK command changes the device from the Set Max Locked mode to the Set Max Unlocked mode. The SET MAX FREEZE LOCK command allows the host to disable the SET MAX commands (including Set Max Unlock) until the next power cycle. When this command is accepted the device is in the Set Max Frozen mode.

7.2.6. Address Offset Feature (Vendor Specific)

Computer systems perform initial code booting by reading from a predefined address on a disk drive. To allow an alternate bootable operating system to exist in a reserved area on disk drive, Address Offset Feature provides a Set Feature function to temporarily offset the drive address space. The offset address space wraps around so that the entire disk drive address space remains addressable in offset mode. The Set Max pointer is set to the end of the reserved area to protect the data in the user area when operating in offset mode. This protection can be removed by a SET MAX ADDRESS / SET MAX ADDRESS EXT command to move the Set Max pointer to the end of the drive.

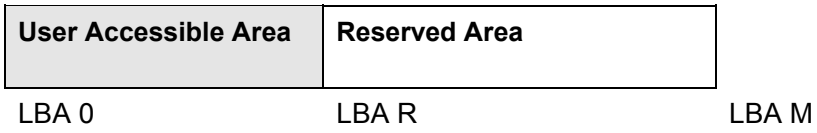
Set Feature Command Subcommand code 09h “ENABLE ADDRESS OFSET MODE sub command” offsets address LBA 0(Cylinder 0, Head 0, Sector 1) to the start of a non-volatile reserved area established using the SET MAX ADDRESS / SET MAX ADDRESS EXT command. The offset condition is cleared by SET FEATURE command Subcommand 89h “DISABLE ADDRESS OFFSET MODE”, Software Reset, Hardware Reset or Power on Reset. Upon entering offset mode the capacity of the drive returned in the IDENTIFY DEVICE data is the size of the former reserved area. A subsequent SET MAX ADDRESS / SET MAX ADDRESS EXT command using the address returned by READ MAX ADDRESS / READMAX ADDRESS EXT command allows access to the entire drive. Addresses wrap so the entire drive remains addressable.

If a non-volatile reserved area has not been established before the device receives a SET FEATURES ENABLE ADDRESS OFFSET MODE sub command, the command fails with Abort error status.

Disable Address Offset Mode removes the address offset and sets the size of the drive reported by the IDENTIFY DEVICE command back to the size specified in the last non-volatile SET MAX ADDRESS / SET MAX ADDRESS EXT command. IDENTIFY DEVICE Word 83 bit 7.indicates the device supports the Set Features Address Offset Mode. IDENTIFY DEVICE Word 86 bit 7 indicates the device is in address offset mode.

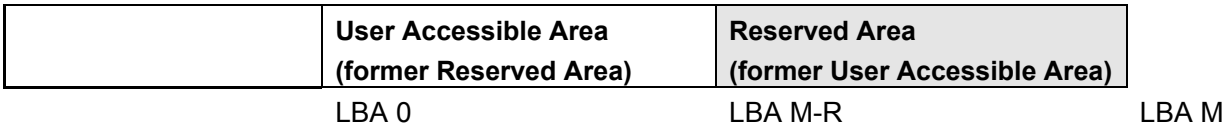
Before Enable Address Offset Mode

A reserved area has been created using a non-volatile SET MAX ADDRESS command or SET MAX ADDRESS EXT command.

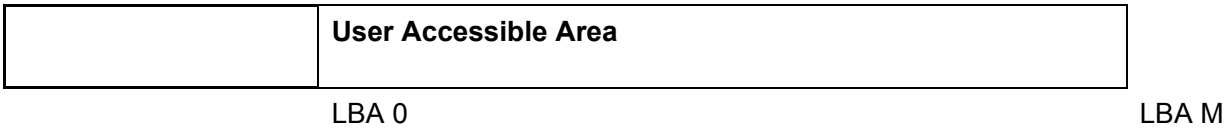


After Enable Address Offset Mode

The former reserved area is now the user accessible area. The former user accessible area is now the reserved area.



After SET MAX ADDRESS/SET MAX ADDRESS EXT command using the Value Returned by READ MAX ADDRESS Command/READ MAX ADDRESS EXT command



Set Feature Disable Address Offset Mode, hardware or Power on Reset returns the device to Address Offset Mode Disabled. Software reset returns the device to Address Offset Mode Disable if Set Features Disable Reverting to Power On Defaults has not been set.

7.2.7. Device Configuration Overlay Feature

The Device Configuration Overlay feature set allows a utility program to modify some of the commands, modes, and features sets that a device reports as supported in the IDENTIFY DEVICE command response as well as the capacity reported. Commands unique to the Device Configuration Overlay feature set use a single command code and are differentiated from one another by the value placed in the Features register. These commands are:

- DEVICE CONFIGURATION FREEZE LOCK command
- DEVICE CONFIGURATION IDENTIFY command
- DEVICE CONFIGURATION RESTORE command
- DEVICE CONFIGURATION SET command

The Device Configuration Overlay feature set affects the IDENTIFY DEVICE command responses. Certain bits in these words that indicate that a command, mode, capacity, or feature set is supported and enabled can be cleared by a DEVICE CONFIGURATION SET command. Since a host protected area may be lost if the capacity of the device is reduced, an attempt to modify the maximum capacity when a host protected area is set will cause the DEVICE CONFIGURATION SET command to return command aborted. If a DEVICE CONFIGURATION FREEZE LOCK command has been issued since the device powered-up, the DEVICE CONFIGURATION RESTORE SET command returns command aborted. The settings made by a DEVICE CONFIGURATION SET command are maintained over power-down and power-up.

A DEVICE CONFIGURATION IDENTIFY command indicates the selectable commands, modes, capacity and feature sets that the device is capable of supporting. After the execution of DEVICE CONFIGURATION SET command this information is no longer available from an IDENTIFY DEVICE command.

A DEVICE CONFIGURATION RESTORE command disables an overlay that has been set by a DEVICE CONFIGURATION SET command and returns the IDENTIFY DEVICE command response to that indicated by the DEVICE CONFIGURATION IDENTIFY command. Since a host protected area may be lost if the capacity of the device is reduced, an attempt to modify the maximum capacity when a host protected area is set will cause the DEVICE CONFIGURATION RESTORE command to return command aborted. If a DEVICE CONFIGURATION FREEZE LOCK command has been issued since the device powered-up, the DEVICE CONFIGURATION RESTORE command returns command aborted.

A DEVICE CONFIGURATION FREEZE LOCK command prevents accidental modification of the state of the Device Configuration Overlay feature set. A device always powers-up with configuration freeze lock not set. After a successful DEVICE CONFIGURATION FREEZE LOCK command is executed, all DEVICE CONFIGURATION SET, DEVICE CONFIGURATION IDENTIFY, and DEVICE CONFIGURATION RESTORE commands are aborted by the device until the device is powered-down and powered-up again. The freeze locked state is not affected by hardware or software reset.

7.2.8. Write Cache and Auto Reallocation

7.2.8.1. Loss of data in write cache

Write cache is a performance enhancement whereby the device reports as completion the write commands to the host as soon as the device has received all of the data into its cache buffer memory. This means that there is a possibility that power off even after write command completion might cause the loss of the data that the device has not written onto the media.

Therefore it is recommended that some other command except write command shall be executed before powering the device off.

7.2.8.2. Error Report and Auto Write Reallocation

In case of write cache mode, the device reports the write command completion after receiving all data from host immediately. After this command completion, the device automatically reallocates the error sector when the device cannot recover the error in write operation. By this auto reallocation, the unrecoverable error sector is reassigned to a spare sector, and the data of the error sector are written on the spare sector. If the device cannot recover the data by this auto write reallocation, the device reports the error as follows:

a) The error occurred when the command execution is on going, the error is reported for the current command.
b) The error occurred when the command execution is not on going, the error is reported for by the next command.

In case of non-write cache mode, the device reports the write command completion after the completion of write operation on the media. If an error occurred during write operation on the media, the device automatically reallocates the error sector when the device cannot recover the error in write operation and reports the command completion.

The Auto Write Reallocation cannot be disabled.

7.2.8.3. Read Auto Reallocation

Non recovered read errors:

When a read operation fails after error recovery is fully carried out, an error is reported to the host. This error location is registered internally as a candidate for the read reallocation. When the error location is specified as a termite of subsequent write operation, the error location is reallocated automatically.

Recovered read errors:

When a read error operation for a sector failed once and recovered at the certain retry step, the recovered sector of the data is reallocated automatically.

7.3. Command Protocol

7.3.1. PIO Data In Command

Execution includes the transfer of one or more 512 byte sectors of data from the device to the host.

1) The host writes any required parameters to the Features, Sector Count, LBA Low (Sector Number), LBA Mid (Cylinder Low), LBA High (Cylinder High), and Device/Head registers.
2) The host writes the command code to the Command Register.
3) The device sets BSY and prepares for data transfer.
4) When a sector(block) of data is available, the device sets DRQ and clears BSY prior to asserting INTRQ.
5) After detecting INTRQ, the host reads the Status Register, then reads one sector (block) of data via the Data Register. In response to the Status Register being read, the device negates INTRQ.
6) The device clears DRQ. If transfer of another sector (block) is required, the device also sets BSY and the above sequence is repeated from 4).

7.3.2. PIO Data Out Command

Execution includes the transfer of one or more 512-byte sectors of data from the host to the device.

1) The host writes any required parameters to the Features, Sector Count, LBA Low (Sector Number), LBA Mid (Cylinder Low), LBA High (Cylinder High), and Device/Head Registers.
2) The host writes the command code to the Command Register.
3) The device sets the DRQ when it gets ready to accept the first sector(block) of data.
4) The host writes one sector block of data to the Data Register.
5) The device clears DRQ and sets BSY.
6) When the device has processed the sector(block), it clears BSY and set the INTRQ signal to "ON". The device sets DRQ again if another sector is required to transfer.
7) After detecting INTRQ, the host reads the Status Register.
8) The device clears the interrupt.
9) If another sector (block) is required to be transferred, the above steps 3) to 8) are repeated.

7.3.3. DMA Data In/Out Command

The Read DMA and Write DMA commands execute data transfer using the slave-DMA channel.
The host is required to enable the slave-DMA feature, if using these commands.

1) The host initializes the slave-DMA feature, if using these commands.
2) The host write any required parameters to the Features, Sector Count, LBA Low (Sector Number), LBA Mid (Cylinder low), LBA High (Cylinder High), and Device/Head registers.
3) The host writes the command code to the Command Register.
4) The device sets the DMARQ when it gets ready to transfer.
5) The slave-DMA channel shall respond by negating CS0- and CS1-, asserting DMACK- signal. And it shall begin data transfer using DMA transfer protocol. CS0- and CS1- shall remain negated as long as DMACK- is asserted, and DMARQ and DMACK- signal shall remain asserted until at least one word of data has been transferred. The register contents are not valid during a DMA Data Phase.
6) The device generates the interrupt to the host, when the data transfer has completed.
7) The host resets the slave-DMA channel.
8) The host reads the Status Register. In response to the Status Register being read, the device negates INTRQ.

7.3.4. Non-Data Command

Execution of these commands does not involve any data transfer:

1) The host writes any required parameters to the registers.
2) The host writes the command code to the Command Registers.
3) The device sets BSY.
4) When the device has completed processing, it clears BSY and asserts INTRQ.
5) The host reads the Status Register.
6) The device negates INTRQ.

7.3.5. Command BSY Timing

The manner in which a command is accepted varies by the three classes of command acceptance all predicated on the fact that to receive a command, BSY=0. The following describes by the conditions under which busy is set after receipt of a command.

Class 1 - The device sets busy within 400 ns.
Class 2 - The device will set BSY within 400 ns, then sets up the sector buffer for a write operation, then sets DRQ, and clears BSY within 400 ns of setting DRQ.

Note: DRQ may be set so quickly on classes 2 that the BSY transition is too short for BSY=1 to be recognized.

7.4. Command Summary

Commands are issued to the device first loading the Command Block Registers with any information needed for the command. Then a command code is written to the Command Register, which starts the execution of the command.

Table 7.4 Command Codes

Command Description	Protocol	Class	48-bit LBA	Code	Parameter Setup					
					FR	SC	LBA Low	LBA Mid	LBA Hi	DH
Read Commands										
Read Buffer	PI	1		E4h						D
Read Sectors	PI	1		20h, 21h		V	V	V	V	V
Read Long	PI	1		22h, 23h		V	V	V	V	V
Read Multiple	PI	1		C4h		V	V	V	V	V
Read DMA	DM	1		C8h, C9h		V	V	V	V	V
Read Verify	ND	1		40h, 41h		V	V	V	V	V
Read Sectors EXT	PI	1	V	24h		V	V	V	V	LD
Read Multiple EXT	PI	1	V	29h		V	V	V	V	LD
Read DMA EXT	DM	1	V	25h		V	V	V	V	LD
Read Verify Sectors EXT	ND	1	V	42h		V	V	V	V	LD
Write Commands										
Write Buffer	PO	2		E8h						D
Write Sectors	PO	2		30h, 31h		V	V	V	V	V
Write Long	PO	2		32h, 33h		V	V	V	V	V
Write Multiple	PO	2		C5h		V	V	V	V	V
Write DMA	DM	2		CAh,CBh		V	V	V	V	V
Format Track	PO	2		50h		V		V	V	V
Flush Cache	ND	1		E7h						D
Write Sector EXT	PO	2	V	34h		V	V	V	V	LD
Write Multiple EXT	PO	2	V	39h		V	V	V	V	LD
Write DMA EXT	DM	2	V	35h		V	V	V	V	LD
Write Multiple FUA EXT	PO	2	V	CEh		V	V	V	V	LD
Write DMA FUA EXT	DM	2	V	3Dh		V	V	V	V	LD
Flush Cache EXT	ND	1	V	EAh						D
Seek Commands										
Recalibrate	ND	1		1Xh						D
Seek	ND	1		7Xh			V	V		V

Table 7.4 Command Codes(Continued)

Command Description	Protocol	Class	48-bit LBA	Code	Parameter Setup					
					FR	SC	LBA Low	LBA Mid	LBA Hi	DH
Mode Set/Check, Diagnostic										
Execute Device Diagnostic	ND	1		90h						D
Initialize Device Parameters	ND	1		91h		V				V
Identify Device	PI	1		ECh						D
Set Features	ND	1		EFh	V					D
Set Multiple Mode	ND	1		C6h		V				D
Power Control										
Check Power Mode	ND	1		98h, E5h		V				D
Idle	ND	1		97h, E3h		V				D
Idle Immediate	ND	1		95h, E1h						D
Sleep	ND	1		99h, E6h						D
Standby	ND	1		96h, E2h		V				D
Standby Immediate	ND	1		94h, E0h						D
Unload Immediate	ND	1		E1h	44h	00h	4Ch	4Eh	55h	D
SMART Commands										
SMART Enable/Disable Auto Save	ND	1		B0h	D2h	V		V		D
SMART Save Attribute Values	ND	1		B0h	D3h			V		D
SMART Enable Operations	ND	1		B0h	D8h			V		D
SMART Disable Operations	ND	1		B0h	D9h			V		D
SMART Return Status	ND	1		B0h	DAh			V		D
SMART Enable/Disable Automatic Off-line	ND	1		B0h	DBh	V		V		D
SMART Execute Off-line Immediate	ND	1		B0h	D4h			V		D
SMART Read Log Sector	PI	1		B0h	D5h	V	V	V		D
SMART Write Log Sector	PO	2		B0h	D6h	V	V	V		D
General Purpose Logging										
Read Log EXT	PI	1	V	2Fh		V	V	V		D
Write Log EXT	PO	2	V	3Fh		V	V	V		D

Table 7.4 Command Codes(Continued)

Command Description	Protocol	Class	48-bit LBA	Code	Parameter Setup					
					FR	SC	LBA Low	LBA Mid	LBA Hi	DH
Security Commands										
Security Disable Password	PO	2		F6h						D
Security Erase Prepare	ND	1		F3h						D
Security Erase Unit	PO	2		F4h						D
Security Freeze Lock	ND	1		F5h						D
Security Set Password	PO	2		F1h						D
Security Unlock	PO	2		F2h						D
Protected Area Commands										
Read Max Address	ND	1		F8h						D
Read Native Max Address EXT	ND	1	V	27h						LD
Set Max Address	ND	1		F9h	00h	V	V	V	V	D
Set Max Address EXT	ND	1	V	37h		V	V	V	V	LD
Set Max Set Password	PO	2		F9h	01h					D
Set Max Lock	ND	1		F9h	02h					D
Set Max Unlock	PO	2		F9h	03h					D
Set Max Freeze Lock	ND	1		F9h	04h					D
Device Configuration Overlay										
Device Configuration Restore	ND	1		B1h	C0h					D
Device Configuration Freeze Lock	ND	1		B1h	C1h					D
Device Configuration Identify	PI	1		B1h	C2h					D
Device Configuration Set	PO	2		B1h	C3h					D

PI: PIO Data In
PO: PIO Data Out
ND: Non-Data
DM: DMA Data In/Out

48-bit LBA: 48-bit Addressing Feature

SC: Sector Count Register
LBA Low: LBA Low Register (Sector Number Register)
LBA Mid: LBA Mid Register (Cylinder Low Register)
LBA Hi: LBA High Register (Cylinder High Register)

DH: Device/Head Register
FR: Features Register
V : Valid parameter register for this command
D : Bit 4 DRV of the Device/head Register is valid.
LD: Bit 4 DRV and bit 6 L of the Device/Head Register are valid.

7.5. Command Descriptions

7.5.1. Check Power Mode [98h, E5h]

Task File Register	7	6	5	4	3	2	1	0
Command	98h or E5h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	XX							

This command posts the power mode of the device. If the device is in, going into, or recovering from the Standby Mode, the device sets BSY bit and set the Sector Count Register to 00h. The device then clears BSY and generates an interrupt. If the device is in the Idle Mode, the device sets BSY, set the Sector Count Register to FFh, clear BSY, and generate an interrupt. If the device is in the Active Mode, the device sets BSY, set the Sector Count Register to FFh, clear BSY, and generate an interrupt.

7.5.2. Device Configuration Identify [B1h, Sub 02h]

Task File Register	7	6	5	4	3	2	1	0
Command	B1h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	02h							

The DEVICE CONFIGURATION IDENTIFY command returns a 512 byte data structure via PIO data-in transfer. The content of this data structure indicates the selectable commands, modes, and feature sets that the device is capable of supporting. If a DEVICE CONFIGURATION SET command has been issued reducing the capabilities, the response to an IDENTIFY DEVICE command will reflect the reduced set of capabilities, while the DEVICE CONFIGURATION IDENTIFY command will reflect the entire set of selectable capabilities. The format of the Device Configuration Overlay data structure is shown in Table 7.5.

If the device has executed a previous DEVICE CONFIGURATION FREEZE LOCK command since power-up, this device returns command aborted.

Table 7.5 DEVICE CONFIGURATION IDENTIFY Data Structure

Word	Description	Value (HEX.)
0	Data Structure Revision	0002h
1	Multiword DMA modes supported bit 15 - 3 0 = Reserved bit 2 1 = Multiword DMA mode 2 and below are supported bit 1 1 = Multiword DMA mode 1 and below are supported bit 0 1 = Multiword DMA mode 0 is supported	0007h
2	Ultra DMA modes supported bit 15 - 6 0 = Reserved bit 5 1 = Ultra DMA mode 5 and below are supported bit 4 1 = Ultra DMA mode 4 and below are supported bit 3 1 = Ultra DMA mode 3 and below are supported bit 2 1 = Ultra DMA mode 2 and below are supported bit 1 1 = Ultra DMA mode 1 and below are supported bit 0 1 = Ultra DMA mode 0 is supported	003Fh
3 - 6	Maximum LBA Address This is the highest address accepted by the device in the factory default condition. If no DEVICE CONFIGURATION SET command has been executed modifying the factory default condition	60GB: 06FC 7C7Fh 40GB: 04A8 52FFh 30GB: 037E 3E3Fh 20GB: 0254 297Fh
7	Command Set / Feature Set Supported bit 15 - 9 0 = Reserved bit 14 0 = Reserved bit 13 0 = Reserved bit 12 1 = SMART selective self-test supported bit 11 1 = Forced Unit Access feature set supported bit 10 0 = Reserved bit 9 0 = Reserved bit 8 1 = 48-bit Addressing feature set supported bit 7 1 = Host Protected Area feature set supported bit 6 0 = Reserved bit 5 0 = Reserved bit 4 0 = Reserved bit 3 1 = Security feature set supported bit 2 1 = SMART error log supported bit 1 1 = SMART self-test supported bit 0 1 = SMART feature set supported	198Fh
8 - 254	Reserved	0000h
255	Integrity word bit 15 - 8 Checksum The checksum is the two's complement of the sum of all byte in words 0 through 254 and the byte consisting of bits 7:0 of word 255. Each byte is added with unsigned arithmetic, and overflow is ignored. bit 7 - 0 Signature Code "A5h"	xxA5h

7.5.3. Device Configuration Freeze Lock [B1h, Sub 01h]

Task File Register	7	6	5	4	3	2	1	0
Command	B1h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	01h							

The DEVICE CONFIGURATION FREEZE LOCK command prevents accidental modification of the Device Configuration Overlay settings. After successful execution of a DEVICE CONFIGURATION FREEZE LOCK command, all DEVICE CONFIGURATION SET, DEVICE CONFIGURATION FREEZE LOCK, DEVICE CONFIGURATION IDENTIFY, and DEVICE CONFIGURATION RESTORE commands are aborted by the device. The DEVICE CONFIGURATION FREEZE LOCK condition is cleared by a power-down. The DEVICE CONFIGURATION FREEZE LOCK condition is not cleared by hardware or software reset.

If the device has executed a previous DEVICE CONFIGURATION FREEZE LOCK command since power-up, the device returns command aborted.

7.5.4. Device Configuration Restore [B1h, Sub 00h]

Task File Register	7	6	5	4	3	2	1	0
Command	B1h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	00h							

The DEVICE CONFIGURATION RESTORE command disables any setting previously made by a DEVICE CONFIGURATION SET command and returns the content of the IDENTIFY DEVICE command response to the original settings as indicated by the data returned from the execution of a DEVICE CONFIGURATION IDENTIFY command.

If DEVICE CONFIGURATION FREEZE LOCK is set or if a host protected area has been set by a SET MAX ADDRESS command or a SET MAX ADDRESS EXT command, the device returns command aborted.

7.5.5. Device Configuration Set [B1h, Sub 03h]

Task File Registers	7	6	5	4	3	2	1	0
Command	B1h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	03h							

The DEVICE CONFIGURATION SET command allows a device manufacturer or a personal computer system manufacturer to reduce the set of optional commands, modes, or feature sets supported by a device as indicated by a DEVICE CONFIGURATION IDENTIFY command. The DEVICE CONFIGURATION SET command transfers an overlay that modifies some of the bits set in the IDENTIFY DEVICE command response. When the bits in these words are cleared, the device no longer support the indicated command, mode, or feature set. If a bit is set in the overlay transmitted by the device that is not set in the overlay received from a DEVICE CONFIGURATION IDENTIFY command, no action is taken for that bit.

The format of the overlay transmitted by the device is described in following table.

Table 7.6 DEVICE CONFIGURATION SET command Data Structure

Word	Description
0	Data Structure Revision Word 0 contains the value 0002h.
1	Multiword DMA modes supported bit 15 - 3 0 = Reserved bit 2 1 = Multiword DMA mode 2 and below are supported Bit 2 is cleared to select no support for Multiword DMA mode 2. This bit shall not be cleared if Multiword DMA mode 2 is currently selected. bit 1 1 = Multiword DMA mode 1 and below are supported Bit 1 is cleared to select no support for Multiword DMA mode 1. This bit shall not be cleared if Multiword DMA mode 2 is supported or Multiword DMA mode 1 or 2 is selected. bit 0 1 = Multiword DMA mode 0 is supported Bit 0 shall not be cleared.

Table 7.6 DEVICE CONFIGURATION SET command Data Structure(Continued)

Word	Description
2	Ultra DMA modes supported bit 15 - 6 0 = Reserved bit 5 1 = Ultra DMA mode 5 and below are supported Bit 5 is cleared to select no support for Ultra DMA mode 5. This bit shall not be cleared if Ultra DMA mode 5 is currently selected. bit 4 1 = Ultra DMA mode 4 and below are supported Bit 4 is cleared to select no support for Ultra DMA mode 4. This bit shall not be cleared if Ultra DMA mode 5 is supported or if Ultra DMA mode 5 or 4 is selected. bit 3 1 = Ultra DMA mode 3 and below are supported Bit 3 is cleared to select no support for Ultra DMA mode 3. This bit shall not be cleared if Ultra DMA mode 5 or 4 is supported or if Ultra DMA mode 5, 4, or 3 is selected. bit 2 1 = Ultra DMA mode 2 and below are supported Bit 2 is cleared to select no support for Ultra DMA mode 2. This bit shall not be cleared if Ultra DMA mode 5, 4, or 3 is supported or if Ultra DMA mode 5, 4, 3, or 2 is selected. bit 1 1 = Ultra DMA mode 1 and below are supported Bit 1 is cleared to select no support for Ultra DMA mode 1. This bit shall not be cleared if Ultra DMA mode 5, 4, 3, or 2 is supported or if Ultra DMA mode 5, 4, 3, 2, or 1 is selected. bit 0 1 = Ultra DMA mode 0 is supported Bit 0 is cleared to select no support for Ultra DMA mode 0. This bit shall not be cleared if Ultra DMA mode 5, 4, 3, 2, or 1 is supported or if Ultra DMA mode 5, 4, 3, 2, 1, or 0 is selected.
3 – 6	Maximum LBA Address Words 3 - 6 define the maximum LBA address. This shall be the highest address accepted by the device after execution of the command. When this value is changed, the content of IDENTIFY DEVICE command are changed to reflect the maximum address set with this command. This value does not be changed and command aborted is returned if a Host Protected Area has been established by the execution of a SET MAX ADDRESS command or a SET MAX ADDRESS EXT command.

Table 7.6 DEVICE CONFIGURATION SET command Data Structure(Continued)

Word	Description
7	Command Set / Feature Set Supported bit 15 - 13 0 = Reserved bit 12 1= SMART selective self-test supported Bit 12 is cleared to select no support for SMART selective self-test feature set bit 11 1 = Forced unit access feature set supported Bit 11 is cleared to select no support for Forced unit access feature set bit 10 - 9 0 = Reserved bit 8 1= 48-bit Addressing feature set supported Bit 8 is cleared to select no support for 48-bit Addressing feature set bit 7 1 = Host Protected Area feature set supported Bit 7 is cleared to select no support for the Host Protected Area feature set. If a host protected area has been established by use of a SET MAX ADDRESS command or a SET MAX ADDRESS EXT command, the device returns command aborted. bit 6 - 4 0 = Reserved bit 3 1 = Security feature set supported Bit 3 is cleared to select no support for the Security feature set This These bits shall not be cleared if the Security feature set has been enabled. bit 2 1 = SMART error log supported Bit 2 is cleared to select no support for the SMART error logging bit 1 1 = SMART self-test supported Bit 1 is cleared to select no support for the SMART self-test bit 0 1 = SMART feature set supported Bit 0 is cleared to select no support for the SMART feature set If bits 1, 2 and 12 of word 7 are not cleared to zero or if the SMART feature set has been enabled by use of the SMART ENABLE OPERATIONS command, these bits shall not be cleared and the device returns command aborted.
8 – 254	Reserved
255	Integrity word bit 15 - 8 Checksum The checksum shall be the two's complement of the sum of all byte in words 0 through 254 and the byte consisting of bits 7:0 of word 255. Each byte shall be added with unsigned arithmetic, and overflow shall be ignored. bit 7 - 0 Signature Code Bits 7:0 of this word shall contain the value A5h.

Error Outputs:

If DEVICE CONFIGURATION FREEZE LOCK is set or If any of the bit modification restrictions described are violated, the device returns command aborted.

Registers	7	6	5	4	3	2	1	0
LBA High	Word Location Number							
LBA Mid	Bit Location Number bit15 - 8							
LBA Low	Bit Location Number bit 7 - 0							
Sector Count	XX (Vendor Unique)							

Sector Count Register:

This register contains vendor unique value by the device.

LBA Mid Register (Cylinder Low Register), LBA Low Register (Sector Number Register):

If the command was aborted because an attempt was made to modify a mode or feature that cannot be modified with the device in its current state, these registers contain bits (15:0) set in the bit positions that correspond to the bits in the device configuration overlay data structure words 1, 2, or 7 for each mode or feature that cannot be changed. If not, the value is 00h.

LBA High Register (Cylinder High Register):

If the command was aborted because an attempt was made to modify a bit that cannot be modified with the device in its current state, this register contains the offset of the word that cannot be changed. If not, the value is 00h.

7.5.6. Execute Device Diagnostic [90h]

Task File Registers	7	6	5	4	3	2	1	0
Command	90h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	XXh							

This command allows the device to perform a self-diagnostics. When Device 0 and Device 1 are connected in the daisy chain mode, this command is executed for both of the devices. When the device receives this command, it sets BSY=1 and executes the self-diagnostic operation. Then the device registers the diagnostic result in the Error Register, clears BSY, and generates an interrupt.

Table 7.7 Diagnostic Codes

Code	Contents
01	No Error
02	Controller error
03	Sector buffer error
05	CPU error
8X	DRV1 error

7.5.7. Flush Cache [E7h]

Task File Registers	7	6	5	4	3	2	1	0
Command	E7h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	L	X	DRV	X	X	X	X
Sector Count	XX							
Features	XX							

The FLUSH CACHE command is to check the device if write cache data were written on the disk or not. BSY is set until all write cache data are written on the disk or a write error is occurred. Maximum time to write the cache data on the disk is 30 seconds. In case of Write Fault, the command is aborted and Status Register bit 5 DWF (Device Write Fault) is set to one. For Device/Head Register bit 6 L=0 (CHS mode), a logical CHS address, which had the first error during write cache, is reported on Task File Register. For Device/Head Register bit 6 L=1 (LBA mode), a LBA address, which had the first error during write cache, is reported on Task File Register.

7.5.8. Flush Cache EXT [EAh]

Task File Register		7	6	5	4	3	2	1	0
Command		EAh							
Feature	Previous setting	XX							
	Current setting	XX							
LBA High	Previous setting	XX							
	Current setting	XX							
LBA Mid	Previous setting	XX							
	Current setting	XX							
LBA Low	Previous setting	XX							
	Current setting	XX							
Sector Count	Previous setting	XX							
	Current setting	XX							
Device		X	X	X	DEV	X	X	X	X

The FLUSH CACHE EXT command to used by the host to request the device to flush the write cache. If there is data in the write cache, that data is written to the media. The BSY bit remains set to one until all data has been successfully written or an error occurs. Maximum time to write the cache data on the disk is 30 seconds. An unrecoverable error encountered while writing data results in the termination of the command and the Command Block registers contain the 48-bit address of the sector where the first unrecoverable error occurred.

7.5.9. Format Track [50h] (Vendor Specific)

Task File Registers	7	6	5	4	3	2	1	0
Command	50h							
LBA High	Logical cylinder number bit 15 - 8							
LBA Mid	Logical cylinder Number bit 7 - 0							
LBA Low	XX							
Device/Head	X	0	X	DRV	Logical head Number			
Sector Count	XXh							
Features	XXh							

The FORMAT TRACK command formats a single track on the device. Each good sector of data on the track will be initialized to zero with the write operation. The logical track address and head address are specified in the LBA High (Cylinder High), LBA Low (Cylinder Low) and Device/Head Registers. When the command is accepted, the device sets the DRQ bit and waits for the host fill the sector buffer. When the sector buffer is filled with 512 bytes of data, the device clears DRQ, sets BSY, and begins the command execution (Transferred single sector data is ignored). This command is used only in the physical mode, but the physical mode is not released. If the device is not in the physical mode, the device executes a vendor specific operation.

7.5.10. Identify Device [ECh]

Task File Registers	7	6	5	4	3	2	1	0
Command	ECh							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XXh							
Features	XXh							

The IDENTIFY DEVICE command enables the host to receive parameter information from the device. When the command is issued, the device sets BSY, stores the required parameter information in the sector buffer, sets DRQ, and generates an interrupt. The host then reads the information from the sector buffer through the Data Register. The parameter words are defined in Table 7.8 and Table 7.9 All reserved bits or words is zero.

Table 7.8 IDENTIFY DEVICE information

Word	Description	Value (HEX.)
0	General configuration bit 15 1 = ATAPI Device, 0 = ATA Device bit 14 - 8 0 = Retired bit 7 1 = Removable Media, 0 = Fixed Media Device bit 6 1 = Fixed Device bit 5 - 3 0 = Retired bit 2 1 = IDENTIFY DEVICE data incomplete bit 1 0 = Retired bit 0 0 = Reserved	0040h
1	Number of logical cylinders	See Table 7.9
2	Specific configuration	C837h
3	Number of logical heads	See Table 7.9
4 – 5	Retired	0000h
6	Number of logical sectors per logical track	See Table 7.9
7-9	Vendor Specific	
10-19	Serial Number (20 ASCII characters)	
20	Retired	0000h
21	Retired	0000h
22	Number of ECC bytes passed on READ/WRITE LONG commands	0004h
23-26	Firmware Revision (8 ASCII Characters)	
27-46	Model number(40 ASCII Characters)	
47	Number of sectors on multiple commands bit 15 - 8 80h (Fixed) bit 7 - 0 Number of sectors on multiple command	8010h
48	Reserved	0000h
49	Capabilities bit 15 – 14 0 = Reserved bit 13 1 = Standby timer values as specified in ATA SPEC supported bit 12 0 = Reserved bit 11 1 = IORDY supported bit 10 1 = IORDY can be disabled bit 9 1 = LBA supported bit 8 1 = DMA supported bit 7 – 0 0 = Retired	0B00h

Table 7.8 IDENTIFY DEVICE information(Continued)

Word	Description	Value (HEX.)
50	Capabilities bit 15 0 (fixed) bit 14 1 (fixed) bit 13 - 1 0 = Reserved bit 0 1 = minimum value of standby timer is device specific	4000h
51	Bit 15 - 8 PIO data transfer cycle timing mode Bit 7 - 0 Vendor Specific	0200h
52	Obsolete	0000h
53	Field validity bit 15 - 3 0 = Reserved bit 2 1 = The field reported in word 88 is valid bit 1 1 = The fields reported words 64-70 are valid bit 0 1 = The fields reported words 54-58 are valid	0007h
54	Number of current cylinders	
55	Number of current heads	
56	Number of current sectors per track	
57-58	Current capacity in sectors	
59	Multiple sector setting bit 15-9 0 = Reserved bit 8 1 = Multiple sector setting is valid bit 7 - 0 Current setting for number of sectors that can be transferred per interrupt on R/W MULTIPLE command	
60-61	Total addressable LBA	See Table 7.9
62	Obsolete	0000h
63	Multi-word DMA transfer bit 15 - 8 Multi-word DMA transfer mode active bit 7 - 0 Multi-word DMA transfer mode supported	
64	Flow control PIO transfer Modes supported bit 15 - 2 0 = Reserved bit 1 1 = PIO Mode 4 supported bit 0 1 = PIO Mode 3 supported	0003h
65	Minimum Multi-word DMA Transfer Cycle Time Per Word(ns)	0078h
66	Manufacturer's Recommended Multi-word DMA Cycle Time(ns)	0078h
67	Minimum PIO Transfer Cycle Time without Flow Control(ns)	00F0h
68	Minimum PIO Transfer Cycle Time with IORDY(ns)	0078h
69-74	Reserved	0000h
75	Queue Depth bit 15 - 5 0 = Reserved bit 4 - 0 Maximum queue depth	0000h
76-79	Reserved	0000h

Table 7.8 IDENTIFY DEVICE information(Continued)

Word	Description	Value (HEX.)
80	ATA Interface Major Version Number Bit 15 - 8 0 = Reserved bit 7 1 = Supports ATA-7 bit 6 1 = Supports ATA-6 bit 5 1 = Supports ATA-5 bit 4 1 = Supports ATA-4 bit 3 1 = Supports ATA-3 bit 2 0 = Obsolete bit 1 0 = Obsolete bit 0 0 = Reserved	0078h
81	ATA Interface Minor Version Number	0019h
82	Command Set Supported bit 15 0 = Reserved bit 14 1 = NOP command supported bit 13 1 = READ BUFFER command supported bit 12 1 = WRITE BUFFER command supported bit 11 0 = Reserved bit 10 1 = Host Protected Area feature set supported bit 9 1 = DEVICE RESET command supported bit 8 1 = SERVICE interrupt supported bit 7 1 = Release interrupt supported bit 6 1 = Look-ahead supported bit 5 1 = Write cache supported bit 4 1 = PACKET command feature set supported bit 3 1 = Power management feature set supported bit 2 1 = Removable feature set supported bit 1 1 = Security feature set supported bit 0 1 = SMART feature set supported	746Bh
83	Command set supported bit 15 0 (Fixed) bit 14 1 (Fixed) bit 13 1 = Flush cache EXT command supported bit 12 1 = Flush cache command supported bit 11 1 = Device configuration overlay feature set supported bit 10 1 = 48-bit Address feature set supported bit 9 1 = Automatic Acoustic Management bit 8 1 = SET MAX security extension supported bit 7 1 = Address offset mode feature supported bit 6 1 = SET FEATURES subcommand required to spin-up bit 5 1 = Power-up in standby feature set supported bit 4 1 = Removable Media Status Notification feature set supported bit 3 1 = Advanced Power Management feature set supported bit 2 1 = CFA feature set supported bit 1 1 = READ/WRITE DMA QUEUED supported bit 0 1 = DOWNLOAD MICROCODE command supported	7D88h

Table 7.8 IDENTIFY DEVICE information(Continued)

Word	Description	Value (HEX.)
84	Command set/feature supported extension bit 15 0 (fixed) bit 14 1 (fixed) bit 13 1 = UNLOAD IMMEDIATE command supported bit 12 0 = Reserved bit 11 0 = Reserved bit 10 1 = WRITE STREAM URG bit supported bit 9 1 = READ STREAM URG bit supported bit 8 1 = 64-bit World Wide Name supported bit 7 1 = WRITE DMA QUEUED FUA EXT command supported bit 6 1 = WRITE DMA/MULTIPLE FUA EXT command supported bit 5 1 = General Purpose Logging Feature set supported bit 4 0 = Streaming Feature set supported bit 3 1 = Media Card Path Though Command feature set supported bit 2 1 = Media Serial Number supported bit 1 1 = SMART self-test supported bit 0 1 = SMART error logging supported	60E3h
85	Command set/feature enabled bit 15 0 = Reserved bit 14 1 = NOP command supported bit 13 1 = READ BUFFER command supported bit 12 1 = WRITE BUFFER command supported bit 11 0 = Reserved bit 10 1 = Host Protected Area feature set supported bit 9 1 = DEVICE RESET command supported bit 8 1 = SERVICE interrupt enabled bit 7 1 = Release interrupt enabled bit 6 1 = Read Look-ahead enabled bit 5 1 = Write cache enabled bit 4 1 = Supports PACKET command feature set bit 3 1 = Supports power management feature set bit 2 1 = Supports removable feature set bit 1 1 = Supports Security Mode feature enabled bit 0 1 = Supports SMART feature enabled	7468h (at shipment)

Table 7.8 IDENTIFY DEVICE information(Continued)

Word	Description	Value (HEX.)
86	Command set/feature enabled bit 15 –14 0 = Reserved bit 13 1 = Flush cache EXT command supported bit 12 1 = Flush Cache command supported bit 11 1 = Device Configuration Overlay supported bit 10 1 = 48-bit Address features set supported bit 9 1 = Automatic Acoustic Management feature set enabled bit 8 1 = SET MAX security extension enabled by SET MAX PASSWORD bit 7 1 = Address offset mode feature enabled bit 6 1 = SET FEATURES subcommand required to spin-up bit 5 1 = Power-up in standby feature set enabled bit 4 1 = Removable Media Status Notification feature set enabled bit 3 1 = Advanced Power Management feature set enabled bit 2 1 = CFA feature set supported bit 1 1 = READ/WRITE DMA QUEUED supported bit 0 1 = DOWNLOAD MICROCODE command supported	3C08h
87	Command set/feature default bit 15 0 (Fixed) bit 14 1 (Fixed) bit 13 1 = IDLE IMMEDIATE with UNLOAD FEATURE supported bit 12 - 11 0 = Reserved bit 10 1 = WRITE STREM URG bit supported bit 9 1 = READ STREAM URG bit supported bit 8 1 = 64 bit World wide name supported bit 7 1 = WRITE DMA QUEUED FUA EXT command supported bit 6 1 = WRITE DMA/MULTIPLE FUA EXT commands supported bit 5 1 = General Purpose Logging feature set supported bit 4 1 = Valid CONFIGURE STREAM command has been executed bit 3 1 = Media Card Pass Through Command feature set enabled bit 2 1 = Media serial number is valid bit 1 1 = SMART self-test supported bit 0 1 = SMART error logging supported	6063h
88	Ultra DMA transfer bit 15 – 14 0 = Reserved bit 13 0 = Ultra DMA mode 5 is selected bit 12 0 = Ultra DMA mode 4 is selected bit 11 0 = Ultra DMA mode 3 is selected bit 10 0 = Ultra DMA mode 2 is selected bit 9 0 = Ultra DMA mode 1 is selected bit 8 0 = Ultra DMA mode 0 is selected bit 7 – 6 0 = Reserved bit 5 1 = Ultra DMA mode 5 and below are supported bit 4 1 = Ultra DMA mode 4 and below are supported bit 3 1 = Ultra DMA mode 3 and below are supported bit 2 1 = Ultra DMA mode 2 and below are supported bit 1 1 = Ultra DMA mode 1 and below are supported bit 0 1 = Ultra DMA mode 0 and below are supported	XX3Fh

Table 7.8 IDENTIFY DEVICE information(Continued)

Word	Description	Value (HEX.)
89	Time required for security erase unit completion Word 89 specifies the time required for the SECURITY ERASE UNIT command to completion. If word 90 is 0000h, the time is not specified. SECURITY ERASE UNIT completion time = value x 2[minutes]	00XXh
90	Time required for enhanced security erase unit completion Word 90 specifies the time required for the ENHANCED SECURITY ERASE UNIT command to completion. ENHANCED SECURITY ERASE UNIT completion time = value x 2[minutes]. If Word 90 is 0000h, the time is not specified.	00XXh
91	Current advanced power management level value Word 91 contains the current Advanced Power Management level settings.	40XXh
92	Master password revision code Word 92 contains the value of the Master password revision code set when the Master Password was last changed.	XXXXh
93	Hardware reset result bit 15 0 (fixed) bit 14 1 (fixed) bit 13 1 = Device detected CBLID- above V_{iH} 0 = Device detected CBLID- below V_{iL} bit 12 - 8 Device 1 hardware reset result. Device 1 clears these bits to zero. Device 1 sets these bits as follows: bit 12 0 = Reserved bit 11 1 = Device 1 asserted PDIAG- bit 10 - 9 These bits indicate how Device 1 determined the device number: 00, 11 = Reserved 01 = A jumper was used 10 = the CSEL signal was used bit 8 1 (Fixed) bit 7 - 0 Device 0 hardware reset result. Device 1 clears these bits to zero. Device 0 sets these bits as follows: bit 7 0 = Reserved bit 6 1 = Device 0 responds when Device 1 is selected bit 5 1 = Device 0 detected the assertion of DASP- bit 4 1 = Device 0 detected the assertion of PDIAG0 bit 3 1 = Device 0 passed diagnostic bit 2 - 1 These bits indicate how Device 0 determined the device number: 00, 11 = Reserved 01 = A jumper was used 10 = the CSEL signal was used bit 0 1 (Fixed)	XXXXh

Table 7.8 IDENTIFY DEVICE information(Continued)

Word	Description	Value (HEX.)
94 - 99	Reserved	0000h
100 - 103	Maximum user LBA for 48-bit addressing feature set	See Table 7.9
104 - 126	Reserved	0000h
127	Removable Media Status Notification feature set support bit 15 – 2 0 = Reserved bit 1 – 0 00 = Removable Media Status Notification feature not supported 01 = Removable Media Status Notification feature supported 10, 11 = Reserved	0000h
128	Security Status bit 15 – 9 0 = Reserved bit 8 Security level 0 = High, 1 = Maximum bit 7 – 6 0 = Reserved bit 5 1 = Enhanced security erase supported bit 4 1 = Security count expired bit 3 1 = Security frozen bit 2 1 = Security locked bit 1 1 = Security enabled bit 0 1 = Security supported	0XXXh
129-159	Vendor Specific	
160-254	Reserved	0000h
255	Integrity Word Bit 15 - 8 Checksum. The checksum is the two's complement of the sum of all bytes in word 0 through 254 and the byte consisting of bit 7:0 in word 255. Each byte is added with unsigned arithmetic, and overflow is ignored. Bit 7 - 0 Signature Code "A5h"	XXA5h

Table 7.9 IDENTIFY DEVICE information (Addressing)

Product name (Model name)	Word 1 Number of CYL.	Word 2 Number of HD	Word 3 Number of SPT	Word 60 - 61 ***1** Word 100 - 103 Total LBA
HTC426060G9AT00	16383 ***2** (3FFFh)	16 (0010h)	63 (3Fh)	117,210,240 (6FC 7C80h)
HTC426040G9AT00	16383 ***2** (3FFFh)	16 (0010h)	63 (3Fh)	78,140,160 (4A8 5300h)
HTC426030G7AT00	16383 ***2** (3FFFh)	16 (0010h)	63 (3Fh)	58,605,120 (37E 3E40h)
HTC426020G7AT00	16383 ***2** (3FFFh)	16 (0010h)	63 (3Fh)	39,070,080 (254 2980h)

***1:** Words 60-61 reflect the total number of user addressable sectors in LBA mode.

***2:** Maximum capacity in CHS mode is 8,455MB.

7.5.11. Idle [97h, E3h]

Task File Registers	7	6	5	4	3	2	1	0
Command	97h or E3h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	Standby Timer Value							
Features	XX							

The IDLE command causes the device to enter to the Active Idle Mode. The Sector Count Register sets the standby timer value. By the power on default, the Standby timer is disabled.

Table 7.10 Standby Timer

Sector Count Value	Standby Timer Value
SC = 0	Disabled (Power on default)
0<SC≤240	SC X 5 sec (5 sec to 20 minutes)
241<SC≤251, 253	30 minutes
252	21 minutes
254, 255	21 minutes 15 sec
Default (Power on)	Disabled

7.5.12. Idle Immediate [95h,E1h] / Unload Immediate [E1h]

Default Function:

Task File Registers	7	6	5	4	3	2	1	0
Command	95h or E1h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	XX							

Unload Feature (Unload Immediate Command):

Task File Registers	7	6	5	4	3	2	1	0
Command	E1h							
LBA High	55h							
LBA Mid	4Eh							
LBA Low	4Ch							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	00h							
Features	44h							

Default function:

The IDLE IMMEDIATE command allows the host to immediately place the device in the Active Idle mode. The device clears BSY and generates an interrupt after transition to active idle mode.

Unload Feature (Unload Immediate Command):

The device retracts the heads onto the ramp position as soon as receiving the UNLOAD FEATURE of the IDLE IMMEDIATE command. INTRQ is asserted and BSY is cleared after the heads are completely retracted onto the ramp position and latched. The time to complete the unload operation is typically within 500 milliseconds of receiving the command. The unload controlling method by the Unload Feature of the Idle Immediate command is the same as that by power mode transition, and does not effect the specification of normal load/unload times per device life.

The device stops read look-ahead operation if it is in process. If the device is performing a write operation, the device suspends writing cached data onto the media as soon as possible. And the device keeps unwritten sectors stored in the cache buffer until receiving a Software Reset, a Hardware Reset, or a any new command except IDLE IMMEDIATE with Unload Feature (Unload Immediate Command).

After completion of this command, the device stays at Low Power Idle mode, does not go into Standby mode and does not load the heads onto the media until receiving a new command. If a device receives this command while the heads are currently on ramp, no physical action is needed. Power consumption of the device is higher than normal low power idle mode moved by Power Management Feature.

7.5.13. Initialize Device Parameters [91h]

Task File Registers	7	6	5	4	3	2	1	0
Command	91h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	0	X	DRV	number of heads minus 1 per cylinder			
Sector Count	Number of sectors per track							
Features	XX							

These parameters allow the host to set the number of sectors per track and the number of heads per cylinder. Upon receipt of the command, the device sets BSY, saves the specified parameters, clears BSY, and generates an interrupt. The only two register values that this command uses are the Sector Count Register that specifies the number of sectors per track, and the Device/Head Register that specifies the number of heads minus 1. The sector count and head values are not checked for validity by this command. If they are invalid, no error will be posted until an illegal access is made by some other command.

7.5.14. Read Buffer [E4h]

Task File Registers	7	6	5	4	3	2	1	0
Command	E4h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	XX							

The READ BUFFER command enables the host to read the current contents of the device's sector buffer. When this command is issued, the device sets BSY, sets up the sector buffer for a read operation, sets DRQ, clears BSY, and generates an interrupt. The host then reads up to 512 bytes of data from the sector buffer.

7.5.15. Read DMA [C8h, C9h]

Task File Registers	7	6	5	4	3	2	1	0
Command	C8h or C9h							
LBA High	L = 0: Cylinder number bit 15 - 8 L = 1: 28-bit LBA address bit 23 - 16							
LBA Mid	L = 0: Cylinder number bit 7 - 0 L = 1: 28-bit LBA address bit 15 - 8							
LBA Low	L = 0: Sector number L = 1: 28-bit LBA address bit 7 - 0							
Device/Head	X	L	X	DRV	L = 0: Head Number L = 1: 28-bit LBA address bit 27-24			
Sector Count	Sector count							
Features	XX							

This command executes in a similar manner to the READ SECTORS command except for the following:

- The host initializes a slave-DMA channel prior to issuing the command.
- Data transfers are qualified by DMARQ and are performed by the slave-DMA channel.
- The device issues only one interrupt per command indicating that data transfer has terminated and status is valid.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector numbers or 28-bit LBA address where the error occurred.

7.5.16. Read DMA EXT [25h]

Task File Register		7	6	5	4	3	2	1	0
Command		25h							
Feature	Previous setting	XX							
	Current setting	XX							
LBA High	Previous setting	LBA bit 47 - 40							
	Current setting	LBA bit 23 - 16							
LBA Mid	Previous setting	LBA bit 39 - 32							
	Current setting	LBA bit 15 - 8							
LBA Low	Previous setting	LBA bit 31 - 24							
	Current setting	LBA bit 7 - 0							
Sector Count	Previous setting	Sector Count bit 15 - 8							
	Current setting	Sector Count bit 7 - 0							
Device		X	1	X	DEV	X	X	X	X

This command executes in a similar manner to the READ SECTORS EXT command except for the following:

- The host initializes a slave-DMA channel prior to issuing the command.
- Data transfers are qualified by DMARQ and are performed by the slave-DMA channel.
- The device issues only one interrupt per command indicating that data transfer has terminated and status is valid.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain 48-bit LBA address where the error occurred.

7.5.17. Read Log EXT [2Fh]

Task File Register		7	6	5	4	3	2	1	0
Command		2Fh							
Feature	Previous setting	XX							
	Current setting	XX							
LBA High	Previous setting	Reserved							
	Current setting	Reserved							
LBA Mid	Previous setting	Sector Offset bit 15 - 8							
	Current setting	Sector Offset bit 7 - 0							
LBA Low	Previous setting	Reserved							
	Current setting	Log Sector Address							
Sector Count	Previous setting	Sector Count bit 15 - 8							
	Current setting	Sector Count bit 7 - 0							
Device		X	X	X	DRV	X	X	X	X

The READ LOG EXT command returns the specified log to the host. If the feature set associated with the log specified in the LBA Low register is not supported or enabled, or if the values in the Features, Sector Count, LBA Mid, or LBA High registers are invalid, the device returns command aborted.

- Sector Count Register:
  Specifies the number of sectors to be read from the specified log. The log transferred by the device starts at the sector in the specified log at the specified offset, regardless of the sector count requested.

- LBA Low Register:
  Specifies the log to be returned as described in Table 7.11.

- LBA Mid Register:
  Specifies the first sector of the log to be read.

Table 7.11 Log Sector Address Definition

Log Sector Address	Content	Sector Size	SMART READ LOG SECTOR command SMART WRITE LOG SECTOR command	READ LOG EXT command WRITE LOG EXT command
00h	SMART Log Directory General Purpose Log Directory	1	Read Only	Read Only
01h	Summary SMART Error Log	1	Read Only	X
02h	Comprehensive SMART Error Log	51	Read Only	X
03h	Extended Comprehensive SMART Error Log	64	X	Read Only
06h	SMART Self-test Log	1	Read Only	X
07h	Extended SMART Self-test Log	1	X	Read Only
09h	SMART Selective Self-test Log	1	Read/Write	
23h	Delayed LBA Log	96	X	Read Only
80h - 9Fh	Host vendor specific	16	Read/Write	
A0h	Device vendor specific	1	Read Only, Host shall not use	
A1h - A2h	Device vendor specific	96	Read Only, Host shall not use	
A3h – BFh	Device vendor specific	1	Read/Write, Host shall not use	

X: The device reports command abort to the host

7.5.17.1. General Purpose Log Directory [Log Sector Address = 00h]

The General Purpose Log Directory is reported size of each log sector address. The following table defines 512 bytes that make up the General Purpose Log Directory.

Table 7.12 General Purpose Log Directory

Byte	Description
0 - 1	SMART Logging Version '0001h'
2 - 3	Number of sectors in the log at log sector address 01h
4 - 5	Number of sectors in the log at log sector address 02h
:	:
510 - 511	Number of sectors in the log at log sector address FFh

7.5.17.2. Extended Comprehensive SMART Error Log [Log Sector Address = 03h]

The errors that device reported are gathered in Extended comprehensive SMART error log. Only 28-bit error entries contain in the Comprehensive SMART log, Both 28-bit error entries and 48-bit error entries contain in the Extended Comprehensive SMART error log. Table 7.13 defines the format of each of the sectors that comprise the Extended Comprehensive SMART error log. This error log data structures include UNC errors, IDNF errors for which the address requested was valid, servo errors, write fault errors, etc. Error log data structures do not include errors attributed to the receipt of faulty commands such as command codes not implemented by the device or requests with invalid parameters or invalid addresses.

Table 7.13 Extended Comprehensive SMART Error Log

Sector	Byte	Description
First Sector	0	SMART error log version '01h'.
	1	Reserved
	2 - 3	Error log index Indicates the error log data structure representing the most recent error
	4 - 127	1st Extended error log data structure
	128 - 251	2nd Extended error log data structure
	252 - 375	3rd Extended error log data structure
	376 - 499	4th Extended error log data structure
	500 - 501	Device error count Contains the total number of errors attributable to the device that have been reported by the device during the life of the device. If the maximum value for this field is reached, the count remains at the maximum value when additional errors are encountered and logged.
	502 - 510	Reserved
	511	Data structure checksum Two's complement of the sum of the first 511 bytes in the first sector.
Subsequent Sector N 1 < N < 63	0 - 3	Reserved
	4 - 127	(4n + 1) Extended Error log data structure
	128 - 251	(4n + 2) Extended Error log data structure
	252 - 375	(4n + 3) Extended Error log data structure
	376 - 499	(4n + 4) Extended Error log data structure
	500 - 510	Reserved
	511	Data structure checksum Two's complement of the sum of the first 511 bytes in the subsequent sector.

(1) Extended Error log data structure

The error log is viewed as a circular buffer. The error log index indicates the most recent error log data structure. Unused error log data structures are filled with zeros. The content of the error log data structure entries is defined in Table 7.14.

Table 7.14 Extended Error Log Data Structure

Byte	Descriptions
n ~ n+17	1st Command Data Structure
n+18 ~ n+35	2nd Command Data Structure
n+36 ~ n+53	3rd Command Data Structure
n+54 ~ n+71	4th Command Data Structure
n+72 ~ n+89	5th Command Data Structure
n+90 ~ n+123	Error Data Structure

(2) Command Data Structure

The fifth command data structure contains the command or reset for which the error is being reported. The fourth command data structure contains the command or reset that preceded the command or reset for which the error is being reported, the third command data structure contains the command or reset preceding the one in the fourth command data structure, etc. If fewer than four commands and resets preceded the command or reset for which the error is being reported, the unused command data structures are filled zero. If the command data structure represents a command or software reset, the content of the command data structure is as shown in Table 7.15 If the command data structure represents a hardware reset, the content of byte n is FFh, the content of bytes n+1 through n+13 are not valid and the content of bytes n+14 through n+17 contain the timestamp.

Table 7.15 Command Data Structure

Byte	Descriptions
n	Content of the Device Control register when the Command register was written.
n+1 ~ n+2	Content of the Features register when the Command register was written.
n+3 ~ n+4	Content of the Sector Count Register when the Command register was written.
n+5 ~ n+6	Content of the LBA Low Register when the Command register was written.
n+7 ~ n+8	Content of the LBA Mid Register when the Command register was written.
n+9 ~ n+10	Content of the LBA High Register when the Command register was written.
n+11	Content of the Device/Head register when the Command register was written.
n+12	Content of the Command Register when Command Register was written.
n+13	Reserved
n+14 ~ n+17	Timestamp (Time since power-on in milliseconds when command acceptance occurred)

(3) Error data structure

The error data structure contains the error description of the command for which an error was reported as described in Table 7.16.

Table 7.16 Error Data Structure

Byte	Description
n	Reserved
n+1	Content of the Error register after command completion occurred.
n+2 ~ n+3	Content of the Sector Count Register after command completion occurred.
n+4 ~ n+5	Content of the LBA Low (Sector Number) Register after command completion occurred.
n+6 ~ n+7	Content of the LBA Mid (Cylinder Low) Register after command completion occurred.
n+8 ~ n+9	Content of the LBA High (Cylinder High) Register after command completion occurred.
n+10	Content of the Device/Head register after command completion occurred.
n+11	Content written to the Status register after command completion occurred.
n+12 ~ n+30	Extended error information (Vendor Specific)
n+31	This contains a value indicating the state of the device when command was written to the Command register or the reset occurred as described below. 01h: Sleep 02h: Standby 03h: Active/Idle with BSY cleared to zero 04h: Executing SMART off-line or self-test
n+32 ~ n+33	Life timestamp Power-on lifetime of the device in hours when command completion occurred.

7.5.17.3. Extended SMART Self-test Log [Log Sector Address = 07h]

The results of SMART short self-test routine, extended self-test routine and SMART selective self-test routine are gathered in Extended SMART self-test log. This log is viewed as a circular buffer. All unused self-test descriptors are filled with zeros. Only 28-bit error entries contain in the SMART self-test log, Both 28-bit error entries and 48-bit error entries contain in the Extended SMART self-test log. Table 7.17 defines the format of each of the sectors that comprise the Extended SMART Self-test log.

Table 7.17 Extended SMART Self-test Log

Byte	Description
0	Self-test log data structure revision number "01h"
1	Reserved
2 - 3	Self-test descriptor index The index points to the most recent entry. When the log is empty, the index is set to zero.
4 - 29	1st descriptor entry
30 - 55	2nd descriptor entry
:	:
446 - 471	18th descriptor entry
472 - 499	Vendor Specific
500 -510	Reserved
511	Data structure checksum

(1) Extended Self-test log descriptor entry

Table 7.18 Self-test log descriptor entry

Byte	Description
n	Content of the LBA Low (Sector Number) Register This contains the content of the LBA Low (Sector Number) Register when the Nth self-test subcommand was issued.
n+1	Content of the self-test execution status byte This contains the result of self-test routine when the Nth self-test was completed.
n+2 ~ n+3	Life timestamp This contains the Power-on lifetime of the device in hours when the Nth self-test subcommand was completed.
n+4	Content of the self-test failure checkpoint byte This contains additional information about the self-test routine that failed.
n+5 ~ n+10	Falling LBA The failing LBA is the LBA of the uncorrectable sector that caused the test to fail. If the device encountered more than one uncorrectable sector during the test, this field indicates the LBA of the first uncorrectable sector encountered. If the test passed or the test failed for some reason other than an uncorrectable sector, the value of this field is undefined.
n+11 ~ n+29	Vendor Specific

7.5.17.4. SMART Selective Self-test Log [Log Sector Address = 09h]

See 7.5.49.5 SMART Selective self-test Log [Log Sector Address = 09h]

7.5.17.5. Delayed LBA Log [Log Sector Address = 23h]

The Delayed LBA Log contains all sector addresses which have been moved from their normal physical location using auto-reallocation feature set. Table 7.19 defines the format of each of the sectors that comprise the Delayed LBA Log. If the maximum size of the Delayed LBA Log is reached and an additional Delayed LBA is detected by the device, the most recent Delayed LBA is added to the log. The log is returned to the host ordered by timestamp, the most recently added entry is last. The Delayed LBA Log is non-volatile, it is preserved across power cycles and hardware reset.

Table 7.19 Delayed LBA Log

Sector	Byte	Decription	
First Sector	0	Delayed LBA Log Version "01h"	
	1	Reserved	
	2 - 3	Number of Delayed LBA entries Contain the total count of Delayed LBA entries	
	4 - 9	1st Entry	LBA address of 1st re-assigned sector
	10 - 11		Power-on lifetime of the device, in hours, when the 1st sector was reallocated.
	:	:	:
	500 - 505	63rd Entry	LBA address of 63rd re-assigned sector
	500 - 507		Power-on lifetime of the device, in hours, when the 63rd sector was reallocated.
	508 - 510	Reserved	
	511	Data Structure Checksum Two's complement of the sum of the first 511 bytes in the subsequent sector.	
Subsequent Sector N 0 < N < 95	0 - 3	Reserved	
	4 - 11	(63n+1) entry	(63n + 1) Reassigned Sector Entry
	12 - 19	(63n+2) entry	(63n + 2) Reassigned Sector Entry
	:	:	:
	500 - 507	(63n+63) entry	(63n + 63) Reassigned Sector Entry
	508 - 510	Reserved	
	511	Data Structure Checksum Two's complement of the sum of the first 511 bytes in the subsequent sector.	

7.5.18. Read Long [22h, 23h]

Task File Registers	7	6	5	4	3	2	1	0
Command	22h or 23h							
LBA High	L = 0: Cylinder number bit 15 - 8 L = 1: 28-bit LBA address bit 23 - 16							
LBA Mid	L = 0: Cylinder number bit 7 - 0 L = 1: 28-bit LBA address bit 15 - 8							
LBA Low	L = 0: Sector number L = 1: 28-bit LBA address bit 7 - 0							
Device/Head	X	L	X	DRV	L = 0: Head Number L = 1: 28-bit LBA address bit 27-24			
Sector Count	01h							
Features	XX							

The READ LONG command performs similarly to the READ SECTORS command except that it returns the data and the ECC bytes contained in the data field of the desired sector. During a READ LONG command, the device does not check the ECC bytes to determine if there has been a data error. Only single sector read long operations are supported. The number of ECC bytes transferred will be 4 Bytes (Default). If the ECC transfer length is changed by Feature register 44h, 68 bytes of ECC will be transferred.

7.5.19. Read Multiple [C4h]

Task File Registers	7	6	5	4	3	2	1	0
Command	C4h							
LBA High	L = 0: Cylinder number bit 15 - 8 L = 1: 28-bit LBA address bit 23 - 16							
LBA Mid	L = 0: Cylinder number bit 7 - 0 L = 1: 28-bit LBA address bit 15 - 8							
LBA Low	L = 0: Sector number L = 1: 28-bit LBA address bit 7 - 0							
Device/Head	X	L	X	DRV	L = 0: Head Number L = 1: 28-bit LBA address bit 27-24			
Sector Count	Sector Count							
Features	XX							

The READ MULTIPLE command is similar to the READ SECTORS command, except interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a SET MULTIPLE MODE command. The number of sectors defined by a SET MULTIPLE MODE command is transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The SET MULTIPLE MODE command, which must be executed prior to the READ MULTIPLE command, sets the block count of sectors to be transferred.

When the READ MULTIPLE command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer for n sectors, where n = residue of {Sector Count / Sector Count per Block}.

Disk errors encountered during READ MULTIPLE commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer should be executed as it normally would, including transfer of corrupted data, if any. Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block that contained the error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

7.5.20. Read Multiple EXT [29h]

Task File Register		7	6	5	4	3	2	1	0
Command		29h							
Feature	Previous setting	XX							
	Current setting	XX							
LBA High	Previous setting	LBA bit 47 - 40							
	Current setting	LBA bit 23 - 16							
LBA Mid	Previous setting	LBA bit 39 - 32							
	Current setting	LBA bit 15 - 8							
LBA Low	Previous setting	LBA bit 31 - 24							
	Current setting	LBA bit 7 - 0							
Sector Count	Previous setting	Sector Count bit 15 - 8							
	Current setting	Sector Count bit 7 - 0							
Device		X	1	X	DEV	X	X	X	X

The READ MULTIPLE EXT command is similar to the READ SECTORS EXT command, except interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a SET MULTIPLE MODE command. The number of sectors defined by a SET MULTIPLE MODE command is transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The SET MULTIPLE MODE command, which must be executed prior to the READ MULTIPLE EXT command, sets the block count of sectors to be transferred.

When the READ MULTIPLE EXT command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer for n sectors, where n = residue of {Sector Count / Sector Count per Block}.

Disk errors encountered during READ MULTIPLE EXT commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer should be executed as it normally would, including transfer of corrupted data, if any. Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block that contained the error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

7.5.21. Read Max Address Command [F8h]

Task File Registers	7	6	5	4	3	2	1	0
Command	F8h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	L	X	DRV	X	X	X	X
Sector Count	XX							
Features	XX							

The READ NATIVE MAX command returns the native maximum 28-bit LBA or cylinders of the device which is not affect by SET MAX ADDRESS command or SET MAX ADDRESS EXT command. The data returned in the command block registers is the maximum device size as shown in the following tables.

Task File Registers	7	6	5	4	3	2	1	0
LBA High	L = 0: Native Maximum Cylinder bit 15 - 8 L = 1: Native Maximum LBA bit 23 - 16							
LBA Mid	L = 0: Native Maximum Cylinder bit 7 - 0 L = 1: Native Maximum LBA bit 15 - 8							
LBA Low	L = 0: Native Maximum Sector Number L = 1: Native Maximum LBA bit 7 - 0							
Device/Head	-	L	-	DRV	L = 0: Native Max Head L = 1: Native Max LBA bit 27 - 24			
Sector Count	XX							

If the 48-bit Address feature set is supported and the 48-bit native max address is greater than 268,435,455, the READ NATIVE MAX ADDRESS command returns a maximum 28-bit LBA value of 268,435,454.

7.5.22. Read Max Address EXT Command [27h]

Task File Register		7	6	5	4	3	2	1	0
Command		27h							
Feature	Previous setting	XX							
	Current setting	XX							
LBA High	Previous setting	XX							
	Current setting	XX							
LBA Mid	Previous setting	XX							
	Current setting	XX							
LBA Low	Previous setting	XX							
	Current setting	XX							
Sector Count	Previous setting	XX							
	Current setting	XX							
Device		X	1	X	DEV	X	X	X	X

The READ NATIVE MAX EXT command returns the native maximum 48-bit LBA of the device which is not affect by SET MAX ADDRESS EXT command or SET MAX ADDRESS EXT command. The data returned in the command block registers is the maximum device size as shown in the following tables.

Task File Register		7	6	5	4	3	2	1	0
LBA High	HOB = 1	Maximum LBA bit 47 - 40							
	HOB = 0	Maximum LBA bit 23 - 16							
LBA Mid	HOB = 1	Maximum LBA bit 39 - 32							
	HOB = 0	Maximum LBA bit 15 - 8							
LBA Low	HOB = 1	Maximum LBA bit 31 - 24							
	HOB = 0	Maximum LBA bit 7 - 0							

7.5.23. Read Sectors [20h, 21h]

Task File Registers	7	6	5	4	3	2	1	0
Command	20h or 21h							
LBA High	L = 0: Cylinder number bit 15 - 8 L = 1: 28-bit LBA address bit 23 - 16							
LBA Mid	L = 0: Cylinder number bit 7 - 0 L = 1: 28-bit LBA address bit 15 - 8							
LBA Low	L = 0: Sector number L = 1: 28-bit LBA address bit 7 - 0							
Device/Head	X	L	X	DRV	L = 0: Head Number L = 1:28-bit LBA address bit 27-24			
Sector Count	Sector Count							
Features	XX							

This command reads sectors as specified in the Sector Count Register. The read operation begins at the sector specified in the LBA High, LBA Mid and LBA Low Registers. DRQ is set prior to data transfer regardless of the presence or absence of an error condition. At command completion, the Command Block Registers contain the 28-bit LBA address or cylinder/head/sector numbers of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the 28-bit LBA address or the cylinder/head/sector numbers where the error occurred.

7.5.24. Read Sectors EXT [24h]

Task File Register		7	6	5	4	3	2	1	0
Command		24h							
Feature	Previous setting	XX							
	Current setting	XX							
LBA High	Previous setting	LBA bit 47 - 40							
	Current setting	LBA bit 23 - 16							
LBA Mid	Previous setting	LBA bit 39 - 32							
	Current setting	LBA bit 15 - 8							
LBA Low	Previous setting	LBA bit 31 - 24							
	Current setting	LBA bit 7 - 0							
Sector Count	Previous setting	Sector Count bit 15 - 8							
	Current setting	Sector Count bit 7 - 0							
Device		X	1	X	DEV	X	X	X	X

The READ SECTORS EXT command reads sectors as specified in the Sector Count Register. The read operation begins at the sector specified in the LBA High, LBA Mid and LBA Low Registers. DRQ is set prior to data transfer regardless of the presence or absence of an error condition. At command completion, the Command Block Registers contain the 48-bit LBA address of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the 48-bit LBA address where the error occurred.

7.5.25. Read Verify [40h, 41h]

Task File Registers	7	6	5	4	3	2	1	0
Command	40h or 41h							
LBA High	L = 0: Cylinder number bit 15 - 8 L = 1: 28-bit LBA address bit 23 - 16							
LBA Mid	L = 0: Cylinder number bit 7 - 0 L = 1: 28-bit LBA address bit 15 - 8							
LBA Low	L = 0: Sector number L = 1: 28-bit LBA address bit 7 - 0							
Device/Head	X	L	X	DRV	L = 0: Head Number L = 1: 28-bit LBA address bit 27-24			
Sector Count	Sector Count							
Features	XX							

The READ VERIFY command is same as the READ SECTORS command, except that DRQ is never set and no data is transferred to the host. When the requested sectors have been verified, the device clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the 28-bit LBA address or cylinder/head/sector numbers of the last sector verified. If an error occurs, the verify terminates at the sector where the error occurs. The Command Block Registers contain the 28-bit LBA address or cylinder/head/sector numbers of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

7.5.26. Read Verify Sectors EXT [42h]

Task File Register		7	6	5	4	3	2	1	0
Command		42h							
Feature	Previous setting	XX							
	Current setting	XX							
LBA High	Previous setting	LBA bit 47 - 40							
	Current setting	LBA bit 23 - 16							
LBA Mid	Previous setting	LBA bit 39 - 32							
	Current setting	LBA bit 15 - 8							
LBA Low	Previous setting	LBA bit 31 - 24							
	Current setting	LBA bit 7 - 0							
Sector Count	Previous setting	Sector Count bit 15 - 8							
	Current setting	Sector Count bit 7 - 0							
Device		X	1	X	DEV	X	X	X	X

The READ VERIFY SECTORS EXT command is same as the READ SECTORS EXT command, except that DRQ is never set and no data is transferred to the host. When the requested sectors have been verified, the device clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the 48-bit LBA address of the last sector verified. If an error occurs, the verify terminates at the sector where the error occurs. The Command Block Registers contain the 48-bit LBA address of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

7.5.27. Recalibrate [1Xh]

Task File Registers	7	6	5	4	3	2	1	0
Command	1Xh							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	XX							

The RECALIBRATE command performs no operation.
Upon receipt of the command, the device clears BSY and generates an interrupt.

7.5.28. Security Disable Password [F6h]

Task File Registers	7	6	5	4	3	2	1	0
Command	F6h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	XX							

The SECURITY DISABLE PASSWORD command requests a transfer of a single sector of data from the host. The following table defines the content of this sector of information. Then the device checks the transferred password. If the User password or the Master password match, the device disables the lock function. This command does not change the Master password that may be reactivated later by setting a User password.

Table 7.20 Password Data Format

Word	Contents
0	Control Word bit 15-1 Reserved bit 0 Identifier 0 = Compare user password, 1 = Compare master password
1-16	Password (32bytes)
17-255	Reserved

Device returns aborted command error if the device is in Locked mode, or the device is in Frozen mode.

7.5.29. Security Erase Prepare [F3h]

Task File Registers	7	6	5	4	3	2	1	0
Command	F6h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	XX							

The SECURITY ERASE PREPARE command shall be issued immediately before the SECURITY ERASE UNIT command to enable device erasing and unlocking. This command is to prevent accidental erasure of the device.

Device returns Aborted command error if the device is in Frozen mode.

7.5.30. Security Erase Unit [F4h]

Task File Registers	7	6	5	4	3	2	1	0
Command	F4h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	XX							

The SECURITY ERASE UNIT command requests a transfer of a single sector of data from the host. The following table defines the content of this sector of information. If the password does not match, then the device rejects the command with an Aborted error.

Table 7.21 Password Data Format

Word	Contents
0	Control Word bit 15-1 Reserved bit 0 Identifier 0 = Compare user password, 1 = Compare master password
1-16	Password(32bytes)
17-255	Reserved

The SECURITY ERASE UNIT command erases all user data. The SECURITY ERASE PREPARE command shall be completed immediately prior to the SECURITY ERASE UNIT command. If the device receives a SECURITY ERASE UNIT command without an immediately prior SECURITY ERASE PREPARE command, the device aborts the SECURITY ERASE UNIT command

This command disables the device lock function, however, the master password is still stored internally within the device and may be reactivated later when a new user password is set. The device returns Aborted command error if the device is in Frozen mode.

The execution time of this command is shown below.

- HTC426060G9AT00 54 minutes
- HTC426040G9AT00 40 minutes
- HTC426030G7AT00 27 minutes
- HTC426020G7AT00 20 minutes

7.5.31. Security Freeze Lock [F5h]

Task File Registers	7	6	5	4	3	2	1	0
Command	F5h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	XX							

The SECURITY FREEZE LOCK command sets the device to frozen mode. After this command is completed any other commands which update the device lock functions are rejected. Frozen mode is quit by power-off or hardware reset. If Security Freeze Lock is issued when the device is in frozen mode, the command executes and the device remains in frozen mode. The device returns Aborted command if the device is in Locked Mode.

Commands disabled by Security Freeze Lock are:

- SECURITY SET PASSWORD command
- SECUIRTY UNLOCK command
- SECURITY DISABLE PASSWORD command
- SECURITY ERASE UNIT command

7.5.32. Security Set Password [F1h]

Task File Registers	7	6	5	4	3	2	1	0
Command	F1h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	XX							

The SECURITY SET PASSWORD command requests a transfer of a single sector of data from the host. The following table defines the content of this sector of information. The data transferred controls the function of this command. The revision code field is returned in the IDENTIFY DEVICE Word 92. The valid revision codes are 0000h to FFFDh. The initial factory shipped value of Master Password Revision code is FFFEh. Value FFFFh is revised.

Table 7.22 Password Data Format

Word	Contents
0	Control Word bit 15-9 Reserved bit 8 Security Level 0 = High, 1 = Maximum bit 7 Reserved bit 0 Identifier 0 = Set user password, 1 = Set master password
1-16	Password(32bytes)
17	Mater Password Revision Code (Valid if word 0 bit 0 = 1)
18 - 255	Reserved

The following table defines the interaction of the identifier and security level bits.

Table 7.23 Security Level and Identifier

Identifier	Security Level	Command Result
User	High	The password supplied with the command is saved as the new user password. The lock function will be enabled from the next power-on or hardware reset. The device will then be unlocked by either the user password or the previously set master password.
User	Maximum	The password supplied with the command is saved as the new user password. The lock function will be enabled from the next power-on or hardware reset. The device will then be unlocked by only the user password. The master password previously set is still stored in the device but shall not be used to unlock the device.
Master	High or Maximum	This combination set a mater password, but will not enable the security mode feature. The security level is not changed. Master password revision code set to the value in Master Password Revision Code field.

The device returns aborted command error if the device is in Locked mode or Frozen mode.

7.5.33. Security Unlock [F2h]

Task File Registers	7	6	5	4	3	2	1	0
Command	F2h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	XX							

The SECURITY UNLOCK command requests a transfer of a single sector of data from the host. The following table defines the content of this sector of information.

Table 7.24 Password Data Format

Word	Contents
0	Control Word bit 15-1 Reserved bit 0 Identifier 0 = Compare user password, 1 = Compare master password
1-16	Password(32bytes)
17-255	Reserved

If the Identifier bit is set to master and the device is in high security level, then the password supplied is compared with the stored master password. If the device is in maximum security level, then the SECURITY UNLOCK command is rejected. If the Identifier bit is set to user, then the device compares the supplied password with the stored user password.

If the password compare fails then the device returns an abort error to the host and decrements the unlock counter. This counter is initially set to five and is decrement for each password mismatch when SECURITY UNLOCK command is issued and the device is locked. When this counter reaches zero then SECURITY UNLOCK and SECURITY ERASE UNIT commands are aborted until a power-on reset or a hard reset. SECURITY UNLOCK command issued when the device is unlocked have no effect on the unlock counter.

The device returns aborted command error if the device is in Frozen mode.

7.5.34. Seek [7Xh]

Task File Registers	7	6	5	4	3	2	1	0
Command	7Xh							
LBA High	L = 0: Cylinder number bit 15 - 8 L = 1: 28-bit LBA address bit 23 - 16							
LBA Mid	L = 0: Cylinder number bit 7 - 0 L = 1: 28-bit LBA address bit 15 - 8							
LBA Low	L = 0: Sector number L = 1: 28-bit LBA address bit 7 - 0							
Device/Head	X	L	X	DRV	L = 0: Head Number L = 1: 28-bit LBA address bit 27-24			
Sector Count	XX							
Features	XX							

The SEEK command initiates a seek operation to the track specified in the Command Block Registers. The device returns the interrupt before completion of a seek operation. If another command is issued to the device while a seek operation is being executed, the device sets BSY, waits for the seek to complete, and then begins execution of the command.

7.5.35. Set Features [EFh]

Task File Registers	7	6	5	4	3	2	1	0
Command	EFh							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	Refer to Table 7.25							
Features	Refer to Table 7.25							

This command is used to specify the parameters shown in Table 7.25 and Table 7.26.

Table 7.25 Set feature Register Definition

Features Code ***1***	Description	Default
03h	Set transfer mode based on value in Sector Count register See Table 7.26.	
05h	Enable Advanced Power management ***2***	√
09h	Enable Address Offset Mode ***3***	
33h	Disable retries	
44h	Enable Vendor Unique ECC Byte Length(24 bytes) transfer	
55h	Disable read look-ahead feature	
66h	Disable reverting to power on defaults	√
77h	Disable ECC	
85h	Disable Advanced Power management ***2***	
88h	Enable ECC	√
89h	Disable Address Offset Mode ***3***	
99h	Enable retries	√
AAh	Enable read look-ahead feature	√
BBh	Enable 4 bytes ECC transfer	√
CCh	Enable reverting to power on defaults	
02h	Enable write cache	√
82h	Disable write cache	

1: If the code is not supported, the device returns Aborted Command Error.

2: See Sec. 7.2.2.3 Advanced Power Management for the details.

3: See Sec. 7.2.6 Address Offset Feature (Vendor Specific)for the details.

Table 7.26 Transfer Mode Code Definition

Sector Count Register	Transfer Mode
2Xh	Multi-Word DMA Mode (X: 0, 1, 2): 0: Mode 0(4.1 MB/s), 1: Mode 1(13.3 MB/s), 2: Mode 2(16.6 MB/s)
4Xh	Ultra DMA Mode (X: 0, 1, 2, 3, 4, 5): 0: Mode 0(16.6 MB/s), 1: Mode 1(25.0 MB/s), 2: Mode 2(33.3 MB/s) 3: Mode 3(44.4 MB/s), 4: Mode 4(66.6 MB/s), 5: Mode 5(100.0 MB/s)

7.5.36. Set Max Address Command [F9h, Sub 00h]

Task File Registers	7	6	5	4	3	2	1	0
Command	F9h							
LBA High	L = 0: Maximum Cylinder bit 15 - 8 L = 1: Maximum LBA bit 23 - 16							
LBA Mid	L = 0: Maximum Cylinder bit 7 - 0 L = 1: Maximum LBA bit 15 - 8							
LBA Low	L = 0: Unused L = 1: Maximum LBA bit 7 - 0							
Device/Head	X	L	X	DRV	L = 0: Unused L = 1: Maximum LBA bit 27-24			
Sector Count	XX							B
Features	00h							

The SET MAX ADDRESS command overwrites the maximum 28-bit LBA address or cylinder of the device in a range of actual device capacity (Head number and Sector Number are ignored, the default value is used for that). Once the device receives this command, all accesses beyond that LBA or cylinder are rejected. IDENTIFY DEVICE command returns the LBA or Cylinder, which is set via this command as default.

Bit 0 "B" of Sector Count Register is option bit for selection whether nonvolatile. When B = 1, Maximum LBA or maximum Cylinder which is set by SET MAX ADDRESS command is preserved over power-on, hardware reset, software reset. When B = 0, Maximum LBA or maximum cylinder which is set by SET MAX ADDRESS command will be lost by power-on or hardware reset. B set to one is not valid when the device is in Address Offset Mode. ABRT is set if B set to one when the device is in Address Offset mode.

READ NAX ADDRESS command should be issued and completed immediately prior to issuing SET MAX ADDRESS command. If the device receives SET MAX ADDRESS command without a prior READ MAX ADDRESS command, the device aborts the SET MAX ADDRESS command. After successful completion of this command, all accesses beyond that LBA or Cylinder will be rejected with setting ID not found error. If the device receives a second nonvolatile SET MAX ADDRESS command (B=1) after a power on or hardware reset, the device reports an ID Not Found error.

If the maximum value to be set exceeds the capacity of the device, or the device is in the Set Max Locked or Set Max Frozen state, then the device returns command aborted. If a protected area has been established by a SET MAX ADDRESS EXT command, the device returns command aborted.

After a successful command completion, IDENTIFY DEVICE response Word 60-61 and Word 100-103 reflect the maximum address set with this command. The address returned in the command block registers is the maximum device size as shown in the following tables:

Output Parameters to the device:

Task File Registers	7	6	5	4	3	2	1	0
LBA High	L = 0: Maximum Cylinder bit 15 - 8 L = 1: Maximum LBA bit 23 - 16							
LBA Mid	L = 0: Maximum Cylinder bit 7 - 0 L = 1: Maximum LBA bit 15 - 8							
LBA Low	L = 0: Maximum Sector Number (*1) L = 1: Maximum LBA bit 7 - 0							
Device/Head	X	L	X	DRV	L = 0: Maximum head number (*1) L = 1: Maximum LBA bit 27-24			

*1: Maximum sector number and maximum head number are fixed values, and the values are 16 and 63.

7.5.37. Set Max Address EXT Command [37h]

Task File Register		7	6	5	4	3	2	1	0
Command		37h							
Feature	Previous setting	XX							
	Current setting	XX							
LBA High	Previous setting	Maximum LBA bit 47 - 40							
	Current setting	Maximum LBA bit 23 - 16							
LBA Mid	Previous setting	Maximum LBA bit 39 - 32							
	Current setting	Maximum LBA bit 15 - 8							
LBA Low	Previous setting	Maximum LBA bit 31 - 24							
	Current setting	Maximum LBA bit 7 - 0							
Sector Count	Previous setting	XX							
	Current setting	XX							B
Device		X	1	X	DEV	X	X	X	X

The SET MAX ADDRESS EXT command overwrites the maximum 48-bit LBA address of the device in a range of actual device capacity. Once the device receives this command, all accesses beyond that LBA or cylinder are rejected. IDENTIFY DEVICE command returns the LBA or Cylinder, which is set via this command as default.

Bit 0 "B" of Sector Count Register is option bit for selection whether nonvolatile. When B = 1, Maximum LBA which is set by SET MAX ADDRESS EXT command is preserved over power-on, hardware reset, software reset. When B = 0, Maximum LBA which is set by SET MAX ADDRESS EXT command will be lost by power-on or hardware reset. B set to one is not valid when the device is in Address Offset Mode. ABRT is set if B set to one when the device is in Address Offset mode.

READ NAX ADDRESS EXT command should be issued and completed immediately prior to issuing SET MAX ADDRESS EXT command. If the device receives SET MAX ADDRESS EXT command without a prior READ MAX ADDRESS EXT command, the device aborts the SET MAX ADDRESS EXT command. After successful completion of this command, all accesses beyond that LBA will be rejected with setting ID not found error. If the device receives a second nonvolatile SET MAX ADDRESS EXT command (B=1) after a power on or hardware reset, the device reports an ID Not Found error.

If the maximum value to be set exceeds the capacity of the device, or the device is in the Set Max Locked or Set Max Frozen state, then the device returns command aborted. If a protected area has been established by a SET MAX ADDRESS command, the device returns command aborted.

After a successful command completion, IDENTIFY DEVICE response Word 60-61 and Word 100-103 reflect the maximum address set with this command. The address returned in the command block registers is the maximum device size as shown in the following tables:

Output Parameters to the device:

Task File Register		7	6	5	4	3	2	1	0
LBA High	HOB = 1	Maximum LBA bit 47 - 40							
	HOB = 0	Maximum LBA bit 23 - 16							
LBA Mid	HOB = 1	Maximum LBA bit 39 - 32							
	HOB = 0	Maximum LBA bit 15 - 8							
LBA Low	HOB = 1	Maximum LBA bit 31 - 24							
	HOB = 0	Maximum LBA bit 7 - 0							

7.5.38. Set Max Freeze Lock Command [F9h, Sub 04h]

Task File Registers	7	6	5	4	3	2	1	0
Command	F9h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	04h							

The SET MAX FREEZE LOCK command sets the device to Set Max Frozen state. After command completion any subsequent SET MAX commands are rejected. Commands disabled by Set Max Freeze Lock are:

- SET MAX ADDRESS command
- SET MAX ADDRESS EXT command
- SET MAX SET PASSWORD command
- SET MAX LOCK command
- SET MAX UNLOCK command

A SET MAX SET PASSWORD command shall previously have been successfully completed. This command shall not be immediately preceded by a READ MAX ADDRESS command. If this command is immediately preceded by a READ MAX ADDRESS command, it is interpreted as a SET MAX ADDRESS command. If the device is in the Set Max Unlocked state, the device reports command aborted.

7.5.39. Set Max Lock Command [F9h, Sub 02h]

Task File Registers	7	6	5	4	3	2	1	0
Command	F9h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	02h							

The SET MAX LOCK command sets the device into Set Max Locked state. After this command is completed any other SET MAX commands except SET MAX UNLOCK command and SET MAX FREEZE LOCK command are rejected. The device remains in this state until a power cycle or the acceptance of a SET MAX UNLOCK or SET MAX FREEZE LOCK command.

This command shall not be immediately preceded by a READ MAX ADDRESS command. If this command is immediately preceded by a READ MAX ADDRESS command, it is interpreted as a SET MAX ADDRESS command. If the device is not in the Set Max Locked state, the device reports command aborted.

7.5.40. Set Max Set Password Command [F9h, Sub 01h]

Task File Registers	7	6	5	4	3	2	1	0
Command	F9h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	01h							

The SET MAX SET PASSWORD command requests a transfer of a single sector of data from the host. Table 7.27 defines the content of this sector of information. The password is retained by the device until the next power cycle. When the device accepts this command the device is in Set Max Unlocked state.

Table 7.27 Set Max Password Data Format

Word	Content
0	Reserved
1- 16	Password for Set Max Security Extension
17 - 255	Reserved

This command shall not be immediately preceded by a READ MAX ADDRESS command. If this command is immediately preceded by a READ MAX ADDRESS command, it is interpreted as a SET MAX ADDRESS command. If the device is in the Set Max Locked or Set Max Frozen state, the device returns command aborted.

7.5.41. Set Max Unlock Command [F9h, Sub 03h]

Task File Registers	7	6	5	4	3	2	1	0
Command	F9h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	01h							

This command requests a transfer of a single sector of data from the host. Table 7.27 defines the content of this sector of information. The password supplied in the sector of data transferred is compared with the stored Set Max password.

If the password compare fails, then the device returns command aborted and decrements the unlock counter. On the acceptance of the SET MAX LOCK command, this counter is set to a value of five and is decrement for each password mismatch when SET MAX UNLOCK command is issued and the device is locked. When this counter reaches zero, then the SET MAX UNLOCK command returns command aborted until a power cycle. If the password compare matches, then the device makes a transition to the Set Max Unlocked State and all Set Max commands are accepted.

This command shall not be immediately preceded by a READ MAX ADDRESS command. If this command is immediately preceded by a READ MAX ADDRESS command, it is interpreted as a SET MAX AADDRESS command. If the device is not in the Set Max Locked state, the device reports command aborted.

7.5.42. Set Multiple Mode [C6h]

Task File Registers	7	6	5	4	3	2	1	0
Command	C6h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	Sector per block							
Features	XX							

The SET MULTIPLE MODE command allows the device to specify the number of sectors per block to perform READ MULTIPLE and WRITE MULTIPLE command operations. The Sector Count Register is loaded with the number of sectors per block. Block sizes of 1, 2, 4, 8, and 16 sectors are supported. Upon receipt of the command, the device sets BSY=1 and checks the Sector Count Register. If the Sector Count Register contains a valid value, then the value is loaded for all subsequent Multiple commands and execution of those commands is enabled. If an invalid value is specified, an Aborted Command error is posted and execution of the Multiple commands is disabled. The Multiple commands cannot be executed in the default mode at power on or after a hardware reset.

7.5.43. Sleep [99h,E6h]

Task File Registers	7	6	5	4	3	2	1	0
Command	99h or E6h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	XX							

The SLEEP command causes the device to be spun down and enter the Sleep Mode. When the rotation stops, BSY is cleared, an interruption is generated, and the interface becomes inactive. Software reset or hardware reset allows the device to recover from the Sleep Mode.

7.5.44. SMART Disable Operations [B0h, Sub D9h]

Task File Registers	7	6	5	4	3	2	1	0
Command	B0h							
LBA High	C2h							
LBA Mid	4Fh							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	D9h							

The SMART DISABLE OPERATIONS command disables all SMART capabilities within the device including any and all timer functions related exclusively to this feature. After receipt of this command the device will disable all SMART operations. Attribute values will no longer be monitored or saved by the device. The device will preserve the state of SMART (either enabled or disabled) across power cycles.

If SMART is not enabled, or if the values in the Features, LBA Mid (Cylinder Low) or LBA High (Cylinder High) registers are invalid, an Aborted command error is posted.

Upon receipt of the SMART DISABLE OPERATIONS command from the host, the device sets BSY, disables SMART capabilities and functions, clears BSY, and asserts INTRQ.

After receipt of this command by the device, all other SMART commands, with the exception of SMART ENABLE OPERATIONS, are disabled and invalid and are aborted by the device (including SMART DISABLE OPERATIONS commands), returning the Aborted command error.

7.5.45. SMART Enable/Disable Automatic Off-line [B0h, Sub DBh]

Task File Registers	7	6	5	4	3	2	1	0
Command	B0h							
LBA High	C2h							
LBA Mid	4Fh							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	00h: Disable, F8h: Enable							
Features	DBh							

SMART ENABLE / DISABLE AUTOMATIC OFF-LINE command enables and disables the Automatic Off-line feature. if Automatic Off-line is enabled, the device automatically correct attribute data in an off-line mode periodically and save the attribute data on the disk.

- The Sector Count Register is set to 00h to disable Automatic collection of Off-line data
- The Sector Count Register is set to F8h to enable Automatic collection of Off-line data

The following tests are performed for the Automatic off-line feature:

a) Raw Read Error Rate Measurement
Partial read scanning and Raw Read Error Rate measurement is performed.
This event is occurred every 24 POH's and 2 minutes of host inactivity.

b) Automatic sector reallocation in off-line read scanning for entire LBA.
This event occurs every 168 POH's and 2 minutes of host inactivity.

Enable state is preserved until receiving a disable automatic off-line command. Upon receipt of the SMART Enable/Disable automatic Off-line command, the device sets BSY to one, enables or disables the automatic off-line data correction feature, clear BSY to zero and asserts INTRQ. During execution of its off-line data collection activities and saving the data on the disk, DRDY and BSY are set to zero. A command is issued during execution of its off-line data collection activities and saving the data on the disk, the device will respond to the host within two seconds.

7.5.46. SMART Enable/Disable Attribute AUTOSAVE [B0h, Sub D2h]

Task File Registers	7	6	5	4	3	2	1	0
Command	B0h							
LBA High	C2h							
LBA Mid	4Fh							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	00h: Disable, F1h: Enable							
Features	D2h							

The SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE command enables and disables the attribute auto save feature of the device. The state of the attribute auto save feature (either enable or disable) will be preserved by the device across power cycles.

A value of zero written by the host into the Sector Count register before issuing this command will cause this feature to be disabled. Disabling this feature does not preclude the device from saving attribute values to non-volatile memory during some other normal operation. A value of F1h written by the host into the Sector Count register before issuing this command will cause this feature to be enabled.

Upon receipt of the command from the host, the device sets BSY, enables or disables the auto save feature, clears BSY, and asserts INTRQ.

During execution of the auto save routine the device does not assert BSY nor de-assert DRDY. If the device receives a command from the host while executing its auto save routine, the device will respond to the host within two seconds.

7.5.47. SMART Enable Operations [B0h, Sub D8h]

Task File Registers	7	6	5	4	3	2	1	0
Command	B0h							
LBA High	C2h							
LBA Mid	4Fh							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	D8h							

The SMART ENABLE OPERATIONS command enables access to all SMART capabilities within the device. Prior to receipt of this command attribute values are neither monitored nor saved by the device. The device will preserve the state of SMART (either enabled or disabled) across power cycles. Once enabled, the receipt of subsequent SMART Enable Operations commands does not affect any of the attribute values.

If the values in the Features, LBA Mid (Cylinder Low), or LBA High (Cylinder High) registers are invalid, an Aborted command error is posted.

Upon receipt of this command from the host, the device sets BSY, enables SMART capabilities and functions, clears BSY, and asserts INTRQ.

7.5.48. SMART Execute Off-line Immediate [B0h, Sub D4h]

Task File Registers	7	6	5	4	3	2	1	0
Command	B0h							
LBA High	C2h							
LBA Mid	4Fh							
LBA Low	Sub command specific							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	D4h							

The SMART EXECUTE OFF-LINE IMMEDIATE command causes the device to immediately initiate the optional set of off-line data collection activities that collect attribute data in an off-line mode and then save this data to the device, or execute a self-diagnostic test routine in either captive or off-line mode.

The device reports command aborted if SMART is not enabled, if register values are invalid, or if a self-test fails while executing a sequence in captive mode. Also, The device sets F4h to LBA Mid Register and sets 2Ch to LBA High Register when the subcommand specified a captive self-test routine which has failed during execution. The device sets 4Fh to LBA Mid Register and sets C2h to LBA High Register when the subcommand specified a captive self-test routine and some error other than a self-test routine failure occurred.

Table 7.28 11 SMART EXECUTE OFF-LINE IMMEDIATE LBA Low Register Values

Value	Description of subcommand to be executed
0	Execute SMART off-line routine immediately in off-line mode
1	Execute SMART Short self-test routine immediately in off-line mode
2	Execute SMART Extended self-test routine immediately in off-line mode
3	Reserved
4	Execute SMART Selective self-test routine immediately in off-line mode
5 - 63	Reserved
64 - 125	Reserved (Vendor specific)
126	Abort off-line mode off-line routine (Vendor specific)
127	Abort off-line mode self-test routine
128	Reserved
129	Execute SMART Short self-test routine immediately in captive mode
130	Execute SMART Extended self-test routine immediately in captive mode
131	Reserved
132	Execute SMART Selective self-test routine immediately in captive mode
133- 191	Reserved
192 - 255	Reserved (Vendor Specific)

7.5.48.1. Off-line mode

The following describes the protocol for executing a SMART EXECUTE OFF-LINE IMMEDIATE sub command routine (including a self-test routine) in the off-line mode.

a) The device executes command completion before executing the subcommand routine.

b) After clearing BSY to zero and setting DRDY to one after receiving the command, the device does not set BSY nor clears DRDY during execution of the subcommand routine.

c) If the device is in the process of performing the sub command routine and is interrupted by any new command from the host except a SLEEP, SMART DISABLE OPERATIONS, SMART EXECUTE OFF-LINE IMMEDIATE or STANDBY IMMEDIATE command, the device suspends or aborts the sub command routine and services the host within two seconds after receipt of the new command. After servicing the interrupting command from the host the device immediately resumes the sub command routine without any additional commands from the host.

d) If the device is in the process of performing a off-line routine and is interrupted by a SLEEP command from the host, the device suspends the off-line routine and services the host after receipt of the command. If the device is in the process of performing any self-test routine and is interrupted by a SLEEP command from the host, the device aborts the self-test routine and services the host after receipt of the command.

e) If the device is in the process of performing the subcommand routine and is interrupted by a SMART DISABLE OPERATIONS command from the host, the device aborts the subcommand routine and services the host within two seconds after receipt of the command.

f) If the device is in the process of performing the subcommand routine and is interrupted by a SMART EXECUTE OFF-LINE IMMEDIATE command from the host, the device aborts the subcommand routine and services the host within two seconds after receipt of the command. The device then services the new SMART EXECUTE OFF-LINE IMMEDIATE subcommand.

g) If the device is in the process of performing the off-line routine and is interrupted by a STANDBY IMMEDIATE command from the host, the device suspends the subcommand routine, and services the host within two seconds after receipt of the command. After receiving a new command that causes the device to exit a power saving mode, the device resumes the off-line routine without any additional commands from the host unless these activities were aborted by the host.

h) If the device is in the process of performing the self-test routine and is interrupted by a STANDBY IMMEDIATE command from the host, the device aborts the self-test routine, and services the host within two seconds after receipt of the command.

i) While the device is performing the subcommand routine it does not automatically change power states (e.g., as a result of its Standby timer expiring). If an error occurs while a device is performing a self-test routine the device discontinues the testing and places the test results in the Self-test execution status byte.

7.5.48.2. Captive mode

When executing a self-test in captive mode, the device sets BSY to one and executes the self-test routine after receipt of the command. At the end of the routine the device places the results of this routine in the Self-test execution status byte and executes command completion. If an error occurs while a device is performing the routine the device discontinues its testing, place the results of this routine in the Self-test execution status byte, and complete the command.

7.5.48.3. SMART off-line routine

This routine only is performed in the off-line mode. The following tests are performed:

a) Raw Read Error Rate Measurement
   Partial read scanning and Raw Read Error Rate measurement is performed.
b) Automatic sector reallocation in off-line read scanning for entire LBA.

7.5.48.4. SMART Short self-test routine

Depending on the value in the LBA Low (Sector Number) register, this self-test routine is performed in either the captive or the off-line or mode. This self-test routine should take on the order of two minutes to complete. The following tests are performed for the SMART short self-test routine:

a) Read test - Partial read scanning and Raw Read Error Rate measurement is performed.
b) Write test - A part of the factory data area is used. Write and Read test is performed for each head.
c) Servo test
   - Position Error Signal is checked for certain rotations in order to analyze RRO and settling accuracy.
   - Load and Unload function is tested.
   - Servo data on the outer track of each zone for each head is verified.
d) Partial read scan test for the first 500MB and the last 300MB 0f the device.
e) Random read test - Average seek time and throughput performance are measured in this test.
f) RAM test - Diagnoses buffer RAM and SDRAM.
g) SMART parameter verify - Detects a threshold exceed condition.
h) SMART error log check - Read scanning for SMART error log sector and Verify validity.

7.5.48.5. SMART Extended self-test routine

Depending on the value in the LBA Low (Sector Number) Register, this self-test routine is performed in either the captive or the off-line mode. This self-test routine takes on the order of tens of minutes to complete. SMART Extended self-test routine performs read scanning test for entire LBA in addition to the above SMART short self-test routine (except the partial read scan test).

7.5.48.6. SMART Selective self-test routine

Depending on the value in the LBA Low (Sector Number) Register, this self-test routine is performed in either the captive mode or the off-line mode. In addition to the above SMART short self-test routine (except the partial read scan test), SMART selective self-test routine performs read scanning test for up to five areas of the media specified by user. To do this, a user shall set the test spans desired in Selective self-test log (Log sector address # 09h) using WRITE SMART LOG command. After the scan of the selected areas, the user may wish to have the rest of media read scanned as an off-line scan. In this case, the user shall set the flag of selective self-test log to enable off-line scan.

7.5.49. SMART Read Log Sector [B0h, Sub D5h]

Task File Registers	7	6	5	4	3	2	1	0
Command	B0h							
LBA High	C2h							
LBA Mid	4Fh							
LBA Low	Log Address							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	Number of sector to be read							
Features	D5h							

The SMART READ LOG SECTOR command returns the indicated log to the host.

LBA Low (Sector number) Register indicates the log to be returned as described in Table 7.11. The host vendor specific logs may be used by the host to store any data desired. If a host vendor specific log has never been written by the host, when read the content of the log is zeros. Device vendor specific logs are used by the device vendor to store any data.

7.5.49.1. SMART Log Directory [Log Sector Address = 00h]

The SMART Log Directory is reported size of each log sector address. The following table defines 512 bytes that make up the SMART Log Directory. The value of the SMART Logging Version word is 01h.

Table 7.29 SMART Log Directory

Byte	Description
0 - 1	SMART Logging Version
2	Number of sectors in the log at log sector address 01h
3	Reserved
:	:
510	Number of sectors in the log at log sector address FFh
511	Reserved

7.5.49.2. Summary SMART Error Log [Log Sector Address = 01h]

The last five 28-bit error entries that device reported are gathered in summary SMART error log. Only 28-bit error entries contain in Summary SMART error log. The following table defines the 512 bytes that make up the summary SMART error log. Error log data structure includes UNC errors, IDNF errors for which the address requested was valid, servo errors, write fault errors, etc. They do not include errors attributed to the receipt of faulty commands such as command codes not implemented by the device or requests with invalid parameters or invalid addresses.

Table 7.30 Summary SMART Error Log

Byte	Description
0	SMART error log version The value of the SMART error log version is 01h.
1	Error log index The error log index indicates the error log data structure representing the most recent error. Only values 1 through 5 are valid.
2-91	First error log data structure
92-181	Second error log data structure
182-271	Third error log data structure
272-361	Fourth error log data structure
362-451	Fifth error log data structure
452-453	Device error count This contains the total number of errors attributable to the device that have been reported by the device during the life of the device. These errors include UNC errors, IDNF errors for which the address requested was valid, servo errors, write fault errors, etc. This count is not include errors attributed to the receipt of faulty commands such as commands codes not implemented by the device or requests with invalid parameters or invalid addresses. If the maximum value for this field is reached, the count remains at the maximum value when additional errors are encountered and logged.
454-510	Reserved
511	Data structure checksum This is the two's complement of the sum of the first 511 bytes in the data structure. Each byte is added with unsigned arithmetic, and overflow is ignored.

(1) Error log data structure

An error log data structure is presented for each of the last five errors reported by the device. These error log data structure entries are viewed as a circular buffer. That is, the first error creates the first error log data structure; the second error, the second error log structure; etc. The sixth error creates an error log data structure that replaces the first error log data structure; the seventh error replaces the second error log structure, etc. The error log pointer indicates the most recent error log structure. If fewer than five errors have occurred, the unused error log structure entries are zero filled. The following table describes the content of a valid error log data structure.

Table 7.31 Error Log Data Structure

Byte	Description
n ~ n+11	First command data structure
n+12 ~ n+23	Second command data structure
n+24 ~ n+35	Third command data structure
n+36 ~ n+47	Fourth command data structure
n+48 ~ n+59	Fifth command data structure
n+60 ~ n+89	Error data structure

(2) Command data structure

The fifth command data structure contains the command or reset for which the error is being reported. The fourth command data structure contains the command or reset that preceded the command or reset for which the error is being reported, the third command data structure contains the command or reset preceding the one in the fourth command data structure, etc. If fewer than four commands and resets preceded the command or reset for which the error is being reported, the unused command data structures are zero filled.

If the command data structure represents a command or software reset, the content of the command data structure is as shown in following table. If the command data structure represents a hardware reset, the content of byte n is FFh, the content of bytes n+1 through n+7 are not valid, and the content of bytes n+8 through n+11 contains the timestamp.

Table 7.32 Command Data Structure

Byte	Description
n	Content of Device Control register when the Command register was written.
n+1	Content of Features register when the Command register was written.
n+2	Content of Sector Count register when the Command register was written.
n+3	Content of LBA Low (Sector Number) register when the Command register was written.
n+4	Content of LBA Mid (Cylinder Low) register when the Command register was written.
n+5	Content of LBA High (Cylinder High) register when the Command register was written.
n+6	Content of Device/Head register when the Command register was written.
n+7	Content written to the Command register.
n+8 ~ n+11	Timestamp This is the time since power-on in milliseconds when command acceptance occurred.

(3) Error data structure

The error data structure contains the error description of the command for which an error was reported as described in following.

Table 7.33 Error Data Structure

Byte	Description
n	Reserved
n+1	Content of the Error register after command completion occurred.
n+2	Content of the Sector Count Register after command completion occurred.
n+3	Content of the LBA Low (Sector Number) Register after command completion occurred.
n+4	Content of the LBA Mid (Cylinder Low) Register after command completion occurred.
n+5	Content of the LBA High (Cylinder High) Register after command completion occurred.
n+6	Content of the Device/Head register after command completion occurred.
n+7	Content written to the Status register after command completion occurred.
n+8 ~ n+25	Extended error information (Vendor Specific)
n+27	State This contains a value indicating the state of the device when command was written to the Command register or the reset occurred as described below. 01h: Sleep 02h: Standby 03h: Active/Idle with BSY cleared to zero 04h: Executing SMART off-line or self-test
n+28 ~ n+29	Life timestamp This contains the power-on lifetime of the device in hours when command completion occurred.

7.5.49.3. Comprehensive SMART Error Log [Log Sector Address = 02h]

The last 255 errors that device reported are gathered in comprehensive SMART error log. Only 28-bit error entries contain in Comprehensive SMART error log. Following table defines the format of each of the sectors that comprise the comprehensive SMART error log. The maximum size of the comprehensive SMART error log is 51 sectors. The comprehensive SMART error log data structures include UNC errors, IDNF errors for which the address requested was valid, servo errors, write fault errors, etc. Comprehensive SMART error log data structures do not include errors attributed to the receipt of faulty commands such as command codes not supported by the device or requests with invalid parameters or invalid addresses.

The error log is viewed as a circular buffer. When the last supported error log sector has been filled, the next error creates an error log data structure that replaces the first error log data structure in sector zero. The next error after that creates an error log data structure that replaces the second error log data structure in sector zero. The sixth error after the log has filled replaces the first error log data structure in sector one, and so on.

Unused error log data structures are filled with zeros.
The content of the error log data structure entries is defined in Table 7.31.

Table 7.34 Comprehensive SMART Error Log

Sector	Byte	Description
First Sector	0	SMART error log version The value of the SMART error log version is 01h.
	1	Error log index The error log index indicates the error log data structure representing the most recent error. Only values 1 through 255 are valid.
	2 - 91	First error log data structure
	92 - 181	Second error log data structure
	182 - 271	Third error log data structure
	272 - 361	Fourth error log data structure
	362 - 451	Fifth error log data structure
	452 - 453	Device error count This contains the total number of errors attributable to the device that have been reported by the device during the life of the device. If the maximum value for this field is reached, the count remains at the maximum value when additional errors are encountered and logged.
	454 - 510	Reserved
	511	Data structure checksum The data structure checksum is the two's complement of the sum of the first 511 bytes in the first sector.
Subsequent Sector N	0 - 2	Reserved
	2 - 91	(5n + 1) Error log data structure
	92 -181	(5n + 2) Error log data structure
	182 - 271	(5n + 3) Error log data structure
	272 - 361	(5n + 4) Error log data structure
	362 - 451	(5n + 5) Error log data structure
	452 - 510	Reserved
	511	Data structure checksum The data structure checksum is the two's complement of the sum of the first 511 bytes in the subsequent sector.

7.5.49.4. SMART Self-test Log [Log Sector Address = 06h]

The last twenty-first results of SMART short self-test routine, extended self-test routine and SMART selective self-test routine are gathered in SMART self-test log. Only 28-bit entries contain in the SMART self-test log. Following Table defines the 512 bytes that make up the SMART self-test log.

Table 7.35 SMART Self-test Log

Byte	Description
0 - 1	Self-test log data structure revision number The value of Self-test log data structure revision number is 0001h
2 - 25	1st descriptor entry
26 - 49	2nd descriptor entry
:	:
482 - 505	21st descriptor entry
506 - 507	Vendor Specific
508	Self Test index The self-test index points to the most recent entry. Initially, when the log is empty, the index is set to zero. It is set to one when the first entry is made, two for the second entry, etc., until the 22nd entry, when the index is reset to one.
509 - 510	Reserved
511	Data structure checksum

(1) Self-test log descriptor entry

This log is viewed as a circular buffer. The first entry begins at byte 2, the second entry begins at byte 26, and so on until the twenty-second entry, that replaces the first entry. Then, the twenty-third entry replaces the second entry, and so on. If fewer than 21 self-tests have been performed by the device, the unused descriptor entries are filled with zeros. The content of the self-test descriptor entry is shown in following table.

Table 7.36 Self-test log descriptor entry

Byte	Description
n	Content of the LBA Low (Sector Number) Register This contains the content of the LBA Low (Sector Number) Register when the Nth self-test subcommand was issued.
n+1	Content of the self-test execution status byte This contains the result of self-test routine when the Nth self-test was completed.
n+2 ~ n+3	Life timestamp This contains the Power-on lifetime of the device in hours when the Nth self-test subcommand was completed.
n+4	Content of the self-test failure checkpoint byte (Vendor specific) This contains additional information about the self-test routine that failed.
n+5 ~ n+8	Falling LBA The failing LBA is the LBA of the uncorrectable sector that caused the test to fail. If the device encountered more than one uncorrectable sector during the test, this field indicates the LBA of the first uncorrectable sector encountered. If the test passed or the test failed for some reason other than an uncorrectable sector, the value of this field is undefined.
n+9 ~ n+23	Vendor Specific

7.5.49.5. SMART Selective self-test Log [Log Sector Address = 09h]

The SMART Selective self-test log is a log that may be both written and read by the host. This log allows the host to select the parameters for the self-test and to monitor the progress of the self-test. Following table defines the content of the selective self-test log. The SMART Selective self-test log provides for the definition of up to five test spans. The starting LBA for each test span is the LBA of the first sector tested in the test span and the ending LBA for each test span is the last LBA tested in the test span. If the starting and ending LBA values for a test span are both zero, a test span is not defined and not tested. These values shall be written by the host. The host shall not write the SMART Selective self-test log while the execution of a selective self-test routine is in progress.

Table 7.37 SMART Selective Self-test Log

Byte	Description
0 - 1	Data structure revision number - This field shall be written as “01h” by the host.
2 - 9	Starting LBA for test span #1
10 - 17	Ending LBA for test span #1
:	:
66 - 73	Starting LBA for test span #5
74 - 81	Ending LBA for test span #5
82 - 337	Reserved - This bit shall be written as zeros by the host
338 - 491	Vendor specific - This bit shall be written as zeros by the host
492 - 499	Current LBA under test read As the self-test progresses, the device modifies this value to contain the beginning LBA of the 65,536 sector block currently being tested. When the self-test including the off-line scan between test spans has been completed, a zero value is placed in this field. This field shall be written with a value of zero by the host.
500 - 501	Current span under test read As the self-test progresses, the device modifies this value to contain the test span number of the current span being tested. If an off-line scan between test spans is selected, a value greater then five is placed in this field during the off-line scan. When the self-test including the off-line scan between test spans has been completed, a zero value is placed in this field. This field shall be written with a value of zero by the host.
502 - 503	Feature flags bit 15 - 5 Reserved - These bits shall be written as zeros by the host bit 4 Off-line scan active flag When set to one, off-line scan after selective test is active. This bit shall be written as zeros by the host and the device modifies them as the test progresses. bit 3 Off-line scan pending flag When set to one, off-line scan after selective test is pending. This bit shall be written as zeros by the host and the device modifies them as the test progresses. bit 2 Vendor specific - This bit shall be written as zeros by the host bit 1 Perform off-line read scan after selective self-test When set to one, perform off-line scan after selective test. This bit shall be written by the host and returned unmodified by the device bit 0 Vendor specific - This bit shall be written as zeros by the host
504 - 507	Vendor specific - This bit shall be written as zeros by the host
508 - 510	Selective self-test pending time This field is the time in minutes from power-on to the resumption of the off-line testing if the pending bit is set. At the expiration of this time, sets the active bit to one, and resumes the off-line scan that had begun before power-down.
511	Data structure checksum This field is the two's complement of the sum of the first 511 bytes in the sector .

7.5.50. SMART Return Status [B0h, Sub DAh]

Task File Registers	7	6	5	4	3	2	1	0
Command	B0h							
LBA High	C2h							
LBA Mid	4Fh							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	DAh							

The SMART RETURN STATUS command is used to communicate the reliability status of the device to the host at the host's request. Upon receipt of this command the device sets BSY, saves any updated attribute values to non-volatile memory, and compares the updated attribute values to the attribute thresholds.

If the device has not detected a threshold exceeded condition, the device sets the LBA Mid (Cylinder Low) Register to 4Fh and the LBA High (Cylinder High) Register to C2h. If the device has detected a threshold exceeded condition, the device sets the LBA Mid (Cylinder Low) Register to F4h and the LBA High (Cylinder High) Register to 2Ch. If SMART is disabled or if the values in the Features, LBA Mid (Cylinder Low), or LBA High (Cylinder High) registers are invalid, an Aborted command error is posted.

7.5.51. SMART Save Attribute Values [B0h, Sub D3h]

Task File Registers	7	6	5	4	3	2	1	0
Command	B0h							
LBA High	C2h							
LBA Mid	4Fh							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	D3h							

The SMART SAVE ATTRIBUTE VALUES command causes the device to immediately save any updated attribute values to the device's non-volatile memory regardless of the state of the attribute auto save timer. Upon receipt of this command from the host, the device sets BSY, writes any updated attribute values to non-volatile memory, clears BSY, and asserts INTRQ. If SMART is disabled or if the values in the Features, LBA Mid (Cylinder Low), or LBA High (Cylinder High) registers are invalid, an Aborted command error is posted.

7.5.52. SMART Write Log Sector [B0h, Sub D6h]

Task File Registers	7	6	5	4	3	2	1	0
Command	B0h							
LBA High	C2h							
LBA Mid	4Fh							
LBA Low	Log Address							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	Number of sector to be written							
Features	D6h							

The SMART WRITE LOG SECTOR Command writes an indicated number of 512 byte data sector to the indicated log sector. Host vendor specific logs are used by the host to store any data desired using the SMART Write LOG SECTOR command. LBA Low (Sector Number) Register indicated the log to be written as described in Table 7.11. If the host attempts to write to a read only log address, the device returns command aborted.

7.5.53. Standby [96h, E2h]

Task File Registers	7	6	5	4	3	2	1	0
Command	96h or E2h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	Standby Timer Value							
Features	XX							

The STANDBY command causes the device to enter the Standby mode. The Sector Count Register sets the standby timer value (Refer to Table 7.10). By the power on default, the Standby timer is disabled.

7.5.54. Standby Immediate [94h, E0h]

Task File Registers	7	6	5	4	3	2	1	0
Command	94h or E0h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	XX							

The STANDBY IMMEDIATE command causes the device to be spun down and enter the Standby Mode. The device returns an interrupt before it has complete transition to the Standby Mode.

7.5.55. Write Buffer [E8h]

Task File Registers	7	6	5	4	3	2	1	0
Command	E8h							
LBA High	XX							
LBA Mid	XX							
LBA Low	XX							
Device/Head	X	X	X	DRV	X	X	X	X
Sector Count	XX							
Features	XX							

The WRITE BUFFER command allows the host to write 512 bytes of data to the sector buffer of the device. When the WRITE BUFFER command and the READ BUFFER command are issued consecutively, the same data is read.

7.5.56. Write DMA [CAh, CBh]

Task File Registers	7	6	5	4	3	2	1	0
Command	CAh or CBh							
LBA High	L = 0: Cylinder number bit 15 - 8 L = 1: 28-bit LBA address bit 23 - 16							
LBA Mid	L = 0: Cylinder number bit 7 - 0 L = 1: 28-bit LBA address bit 15 - 8							
LBA Low	L = 0: Sector number L = 1: 28-bit LBA address bit 7 - 0							
Device/Head	X	L	X	DRV	L = 0: Head Number L = 1:28-bit LBA address bit 27-24			
Sector Count	Sector count							
Features	XX							

This command executes in a similar manner to the WRITE SECTORS command except for the followings:

- The host initializes a slave-DMA channel prior to issuing the command.
- Data transfers are qualified by DMARQ and are performed by the slave-DMA channel.
- The device issues only one interrupt per command to indicate that data transfer has terminated and status is valid.

If an error occurs, the write terminates at the sector where the error occurred. The command Block Registers contain the cylinder, head, and sector numbers or 28-bit LBA address where the error occurred.

7.5.57. Write DMA EXT [35h]

Task File Register		7	6	5	4	3	2	1	0
Command		35h							
Feature	Previous setting	XX							
	Current setting	XX							
LBA High	Previous setting	LBA bit 47 - 40							
	Current setting	LBA bit 23 - 16							
LBA Mid	Previous setting	LBA bit 39 - 32							
	Current setting	LBA bit 15 - 8							
LBA Low	Previous setting	LBA bit 31 - 24							
	Current setting	LBA bit 7 - 0							
Sector Count	Previous setting	Sector Count bit 15 - 8							
	Current setting	Sector Count bit 7 - 0							
Device		X	1	X	DEV	X	X	X	X

This command executes in a similar manner to the WRITE SECTORS EXT command except for the followings:

- The host initializes a slave-DMA channel prior to issuing the command.
- Data transfers are qualified by DMARQ and are performed by the slave-DMA channel.
- The device issues only one interrupt per command to indicate that data transfer has terminated and status is valid.

If an error occurs, the write terminates at the sector where the error occurred. The command Block Registers contain the 48-bit LBA address where the error occurred.

7.5.58. Write DMA FUA EXT [3Dh]

Task File Register		7	6	5	4	3	2	1	0
Command		3Dh							
Feature	Previous setting	XX							
	Current setting	XX							
LBA High	Previous setting	LBA bit 47 - 40							
	Current setting	LBA bit 23 - 16							
LBA Mid	Previous setting	LBA bit 39 - 32							
	Current setting	LBA bit 15 - 8							
LBA Low	Previous setting	LBA bit 31 - 24							
	Current setting	LBA bit 7 - 0							
Sector Count	Previous setting	Sector Count bit 15 - 8							
	Current setting	Sector Count bit 7 - 0							
Device		X	1	X	DEV	X	X	X	X

The WRITE DMA FUA EXT command provides the same function as the WRITE DMA EXT command except that regardless of whether write caching in the device is enabled or not, the user data is written to the media before ending status for the command is reported.

7.5.59. Write Log EXT [3Fh]

Task File Register		7	6	5	4	3	2	1	0
Command		3Fh							
Feature	Previous setting	XX							
	Current setting	XX							
LBA High	Previous setting	Reserved							
	Current setting	Reserved							
LBA Mid	Previous setting	Sector Offset bit 15 - 8							
	Current setting	Sector Offset bit 7 - 0							
LBA Low	Previous setting	Reserved							
	Current setting	Log Sector Address							
Sector Count	Previous setting	Sector Count bit 15 - 8							
	Current setting	Sector Count bit 7 - 0							
Device		X	X	X	DRV	X	X	X	X

The WRITE LOG EXT command writes a specified number of 512 byte data sectors to the specified log. If the feature set associated with the log specified in the LBA Low register is not supported or enabled, or if the values in the Features, Sector Count, LBA Mid, or LBA High registers are invalid, the device returns command aborted. If the host attempts to write to a read only (RO) log address, the device returns command aborted.

- Sector Count Register:
  Specifies the number of sectors that shall be written to the specified log. If the number is greater than the number indicated in the Log directory (which is available in Log number zero), the device returns command aborted. The log transferred to the device is stored by the device starting at the first sector in the specified log.

- LBA Low Register:
  Specifies the log to be written as described in Table 7.11. If the host attempts to write to a read only (RO) log address, the device returns command aborted.

- LBA Mid Register:
  Specifies the first sector of the log to be written.

7.5.60. Write Long [32h, 33h]

Task File Registers	7	6	5	4	3	2	1	0
Command	32h or 33h							
LBA High	L = 0: Cylinder number bit 15 - 8 L = 1: 28-bit LBA address bit 23 - 16							
LBA Mid	L = 0: Cylinder number bit 7 - 0 L = 1: 28-bit LBA address bit 15 - 8							
LBA Low	L = 0: Sector number L = 1: 28-bit LBA address bit 7 - 0							
Device/Head	X	L	X	DRV	L = 0: Head Number L = 1: 28-bit LBA address bit 27-24			
Sector Count	01h							
Features	XX							

The WRITE LONG command is similar to the WRITE SECTORS command, except that it writes the data and the ECC bytes directly from the host; the device does not generate the ECC bytes itself. Only single sector Write Long operations are supported. The transfer of the ECC bytes shall be 8-bits wide. The number of ECC bytes transferred will be 4 bytes (Default). If the ECC transfer length is changed by Features Register = 44h, 68 bytes of ECC will be transferred.

7.5.61. Write Multiple [C5h]

Task File Registers	7	6	5	4	3	2	1	0
Command	C5h							
LBA High	L = 0: Cylinder number bit 15 - 8 L = 1: 28-bit LBA address bit 23 - 16							
LBA Mid	L = 0: Cylinder number bit 7 - 0 L = 1: 28-bit LBA address bit 15 - 8							
LBA Low	L = 0: Sector number L = 1: 28-bit LBA address bit 7 - 0							
Device/Head	X	L	X	DRV	L = 0: Head Number L = 1: 28-bit LBA address bit 27-24			
Sector Count	Sector Count							
Features	XX							

The WRITE MULTIPLE command is similar to the WRITE SECTORS command, except interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by the SET MULTIPLE MODE command. The number of sectors defined by the SET MULTIPLE MODE command is transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The SET MULTIPLE MODE command, which must be executed prior to the WRITE MULTIPLE command, sets the block count of sectors to be transferred.

When the WRITE MULTIPLE command is issued, the Sector count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sector is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The Partial block transfer shall be for n sectors, where n = residue of {Sector Count / (Sector Count per Block)}

Disk errors encountered during WRITE MULTIPLE commands are posted after the attempted disk write of the block or partial block transferred. The write operation ends with the sector in error, regardless of the position in the block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of transfer of each block, except first block.

7.5.62. Write Multiple EXT [39h]

Task File Register		7	6	5	4	3	2	1	0
Command		39h							
Feature	Previous setting	XX							
	Current setting	XX							
LBA High	Previous setting	LBA bit 47 - 40							
	Current setting	LBA bit 23 - 16							
LBA Mid	Previous setting	LBA bit 39 - 32							
	Current setting	LBA bit 15 - 8							
LBA Low	Previous setting	LBA bit 31 - 24							
	Current setting	LBA bit 7 - 0							
Sector Count	Previous setting	Sector Count bit 15 - 8							
	Current setting	Sector Count bit 7 - 0							
Device		X	1	X	DEV	X	X	X	X

The WRITE MULTIPLE EXT command is similar to the WRITE SECTORS EXT command, except interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by the SET MULTIPLE MODE command. The number of sectors defined by the SET MULTIPLE MODE command is transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The SET MULTIPLE MODE command, which must be executed prior to the WRITE MULTIPLE EXT command, sets the block count of sectors to be transferred.

When the WRITE MULTIPLE EXT command is issued, the Sector count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sector is not

evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The Partial block transfer shall be for n sectors, where n = residue of {Sector Count / (Sector Count per Block)}

Disk errors encountered during WRITE MULTIPLE EXT commands are posted after the attempted disk write of the block or partial block transferred. The write operation ends with the sector in error, regardless of the position in the block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of transfer of each block, except first block.

7.5.63. Write Multiple FUA EXT [CEh]

Task File Register		7	6	5	4	3	2	1	0
Command		CEh							
Feature	Previous setting	XX							
	Current setting	XX							
LBA High	Previous setting	LBA bit 47 - 40							
	Current setting	LBA bit 23 - 16							
LBA Mid	Previous setting	LBA bit 39 - 32							
	Current setting	LBA bit 15 - 8							
LBA Low	Previous setting	LBA bit 31 - 24							
	Current setting	LBA bit 7 - 0							
Sector Count	Previous setting	Sector Count bit 15 - 8							
	Current setting	Sector Count bit 7 - 0							
Device		X	1	X	DEV	X	X	X	X

The WRITE MULTIPLE FUA EXT command provides the same function as the WRITE MULTIPLE EXT command except that regardless of whether write caching in the device is enabled or not, the user data is written to the media before ending status for the command is reported.

7.5.64. Write Sectors [30h, 31h]

Task File Registers	7	6	5	4	3	2	1	0
Command	30h or 31h							
LBA High	L = 0: Cylinder number bit 15 - 8 L = 1: 28-bit LBA address bit 23 - 16							
LBA Mid	L = 0: Cylinder number bit 7 - 0 L = 1: 28-bit LBA address bit 15 - 8							
LBA Low	L = 0: Sector number L = 1: 28-bit LBA address bit 7 - 0							
Device/Head	X	L	X	DRV	L = 0: Head Number L = 1: 28-bit LBA address bit 27-24			
Sector Count	Sector Count							
Features	XX							

The WRITE SECTORS command transfers one or more sectors from the host to the device. The data is then written to the media, beginning at the specified in the LBA High (Cylinder High), LBA Mid (Cylinder Low) and LBA Low (Sector Number) Registers.

At command completion, the Command Block Registers contain the cylinder, head, and sector numbers or LBA address of the last sector written. If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head, and sector numbers or LBA address of the sector where the error occurred.

7.5.65. Write Sectors EXT [34h]

Task File Register		7	6	5	4	3	2	1	0
Command		34h							
Feature	Previous setting	XX							
	Current setting	XX							
LBA High	Previous setting	LBA bit 47 - 40							
	Current setting	LBA bit 23 - 16							
LBA Mid	Previous setting	LBA bit 39 - 32							
	Current setting	LBA bit 15 - 8							
LBA Low	Previous setting	LBA bit 31 - 24							
	Current setting	LBA bit 7 - 0							
Sector Count	Previous setting	Sector Count bit 15 - 8							
	Current setting	Sector Count bit 7 - 0							
Device		X	1	X	DEV	X	X	X	X

The WRITE SECTORS EXT command transfers one or more sectors from the host to the device. The data is then written to the media, beginning at the specified in the LBA High, LBA Mid and LBA Low Registers.

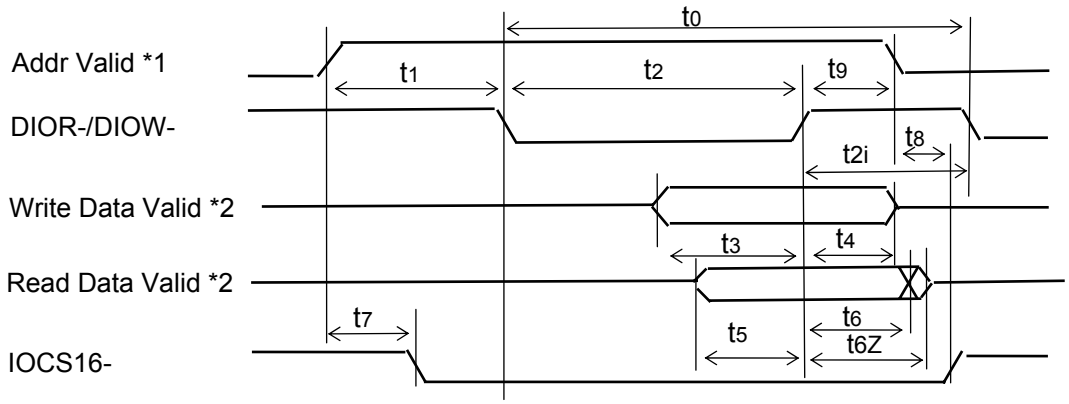
At command completion, the Command Block Registers contain 48-bit LBA address of the last sector written. If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The command Block Registers contain 48-bit LBA address of the sector where the error occurred.

8.0 Interface Signal Timing

8.1. Data Transfer Timing

Figures 8-1, 8-2, and 8-3 show the timing for asserting interface signals for transferring 16-bit and 8-bit data.

Figure 8.1 PIO Data Transfer Timing (Mode 4)

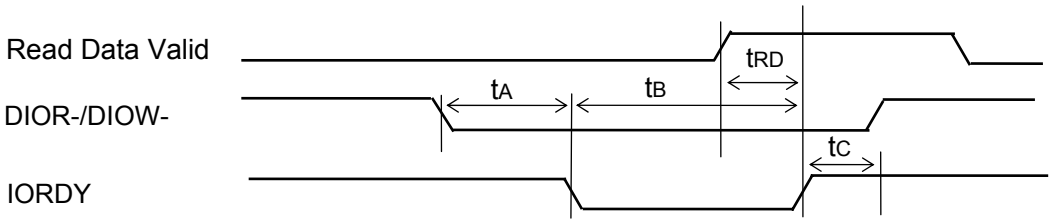


*1 Device Address consists of signals CS0-, CS1-, and DA2-0

*2 Data consists of DD0-15(16 bit) or DD0-7(8 bit)

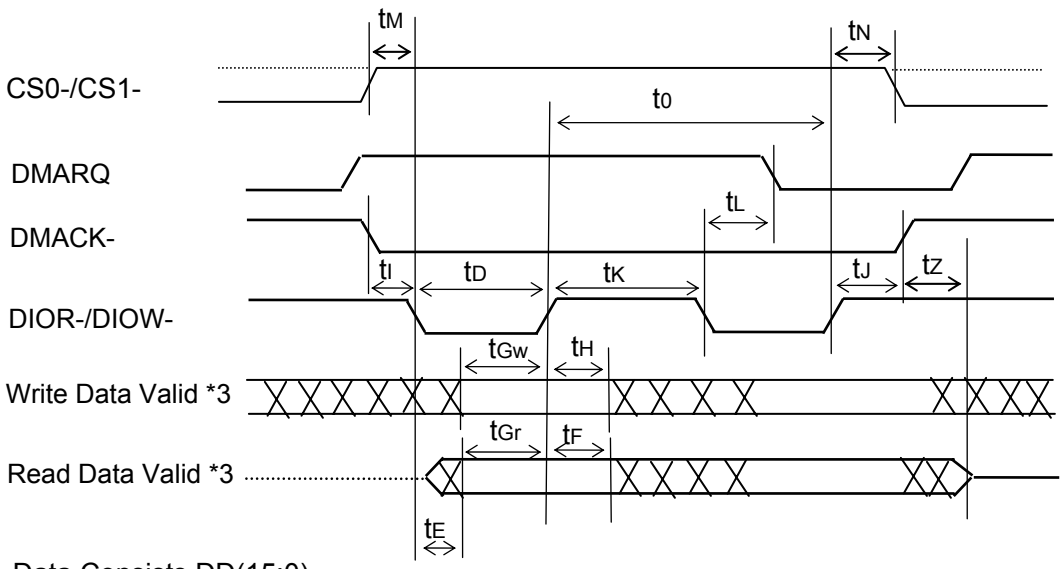
SYMBOL	Description	MIN(ns)	MAX(ns)
t_0	Cycle Time	120	
t_1	Address Valid to DIOR-/DIOW- Setup	25	
t_2	DIOR-/DIOW- Pulse Width	70	
t_{2i}	DIOR-/DIOW- Recovery	25	
t_3	DIOW- Data Setup	20	
t_4	DIOW- Data Hold	10	
t_5	DIOR- Data Setup	20	
t_6	DIOR- Data Hold	5	
t_{6Z}	DIOR- Data tristate		30
t_7	Addr Valid To IOCS16- Assertion(MAX)		40
t_8	Addr Valid To IOCS16- Negation (MAX)		30
t_9	DIOR-/DIOW- to Address Valid Hold	10	

Figure 8.2 IORDY Timing



SYMBOL	Description	MIN(ns)	MAX(ns)
t_A	IORDY Setup Time		35
t_B	IORDY Pulse Width		1250
t_{RD}	Read Data Valid to IORDY active	0	
tc	IORDY assertion to release		5

Figure 8.3 Multi-word DMA Data Transfer Timing (Mode 2)

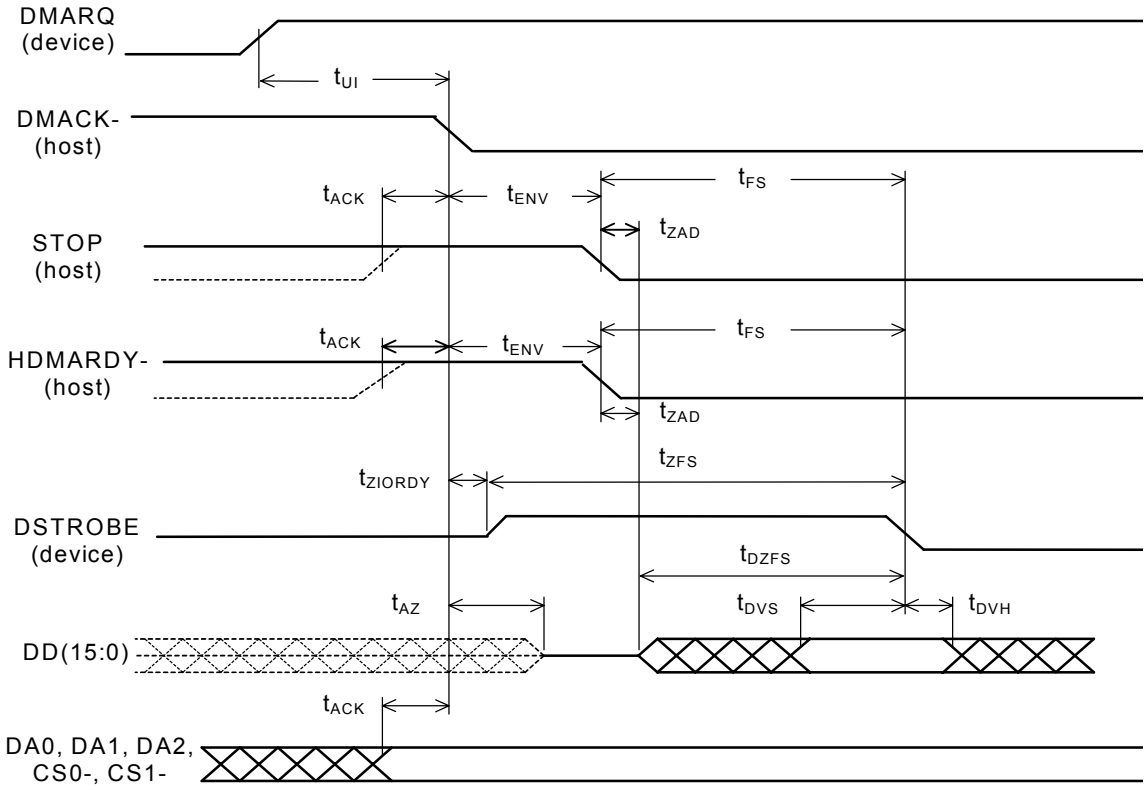


*3 Data Consists DD(15:0)

SYMBOL	Description	MIN(ns)	MAX(ns)
t_0	Cycle Time	120	
t_D	DIOR- /DIOW- Pulse Width	70	
t_E	DIOR- Data Access		50
t_F	DIOR- Data Hold	5	
t_{Gr}	DIOR- Data Setup	20	
t_{Gw}	DIOW- Data Setup	20	
t_H	DIOW- Data Hold	10	
t_I	DMACK to DIOR- / DIOW- Setup	0	
t_J	DIOR- / DIOW- to DMACK Hold	5	
t_K	DIOR- / DIOW- Negated Pulse Width	25	
t_L	DIOR- / DIOW- to DMARQ Delay		35
t_M	CS(1:0) valid to DIOR-/DIOW-	25	
t_N	CS(1:0) hold	10	
t_Z	DMACK- to tristate		25

8.2. Ultra DMA Data Transfer Timing

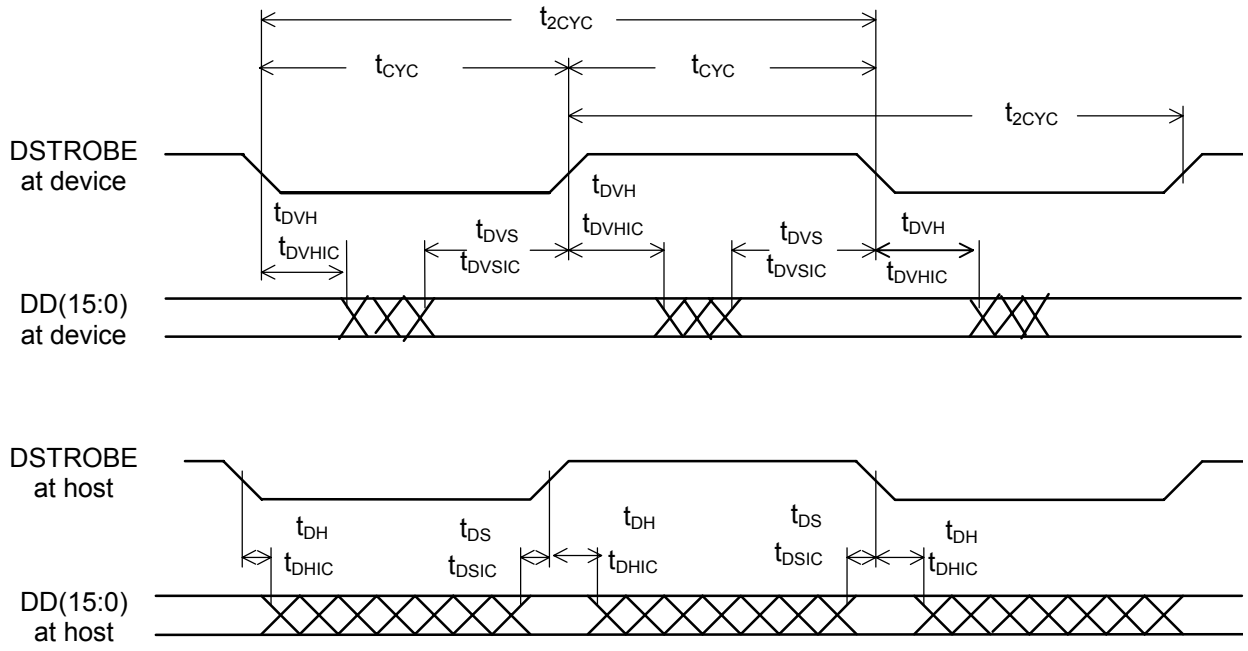
Figure 8.4 Initiating an Ultra DMA Read



Note: The definitions for the STOP, HDMARDY and DSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

	Mode 0(ns)		Mode 1(ns)		Mode 2(ns)		Mode3(ns)		Mode4(ns)		Mode5(ns)		Description
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{DVS}	70		48		31		20		6.7		4.8		Data valid setup time at sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		4.8		Data valid hold time at sender
t_{FS}		230		200		170		130		120		90	First strobe
t_{UI}	0		0		0		0		0		0		Unlimited interlock
t_{AZ}		10		10		10		10		10		10	Maximum time allowed for output drivers to release
t_{ZAD}	0		0		0		0		0		0		Maximum delay time for output drivers turning on
t_{ENV}	20	70	20	70	20	70	20	55	20	55	20	50	Envelope time
t_{ZIORDY}	0		0		0		0		0		0		Minimum time waiting before driving IORDY
t_{ZFS}	0		0		0		0		0		35		Time from STROBE output released-to-driving until the first transition of critical timing
t_{DZFS}	70		48		31		20		6.7		25		Time from data output released-to-driving until the first transition of critical timing
t_{ACK}	20		20		20		20		20		20		Setup and hold times before assertion and negation of DMACK_

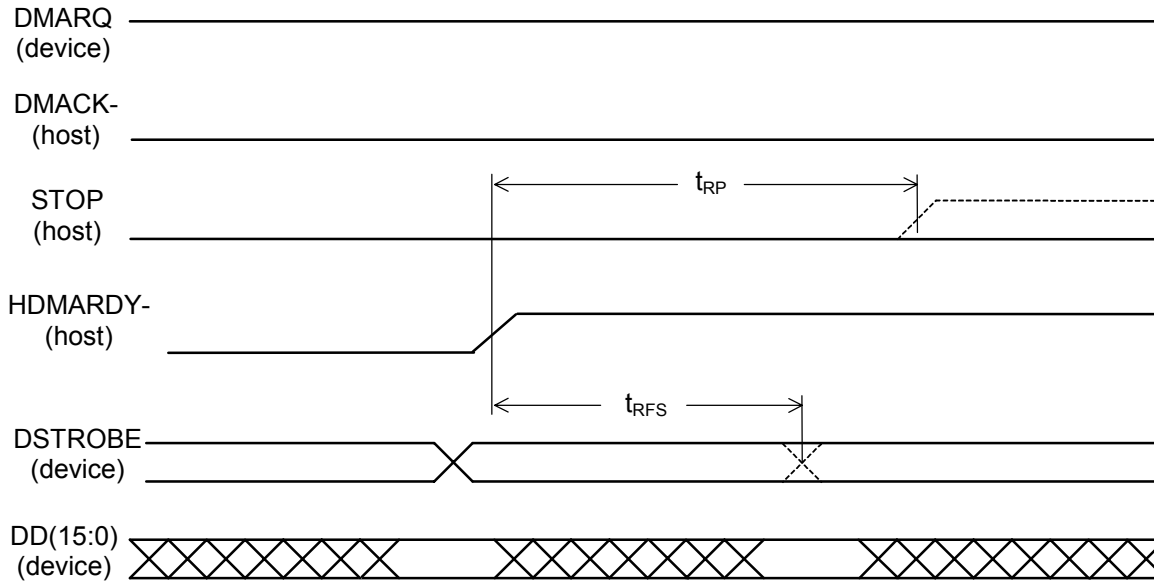
Figure 8.5 Sustained Ultra DMA Read Data



Note: DD(15:0) and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

	Mode 0(ns)		Mode 1(ns)		Mode 2(ns)		Mode3(ns)		Mode4(ns)		Mode5(ns)		Description
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CYC}	112		73		54		39		25		16.8		Cycle time allowing for asymmetry and clock variation
$t2_{CYC}$	230		153		115		86		57		38		Two cycle time allowing for clock variation
t_{DS}	15		10		7		7		5		4		Data setup time at recipient
t_{DH}	5		5		5		5		5		4.6		Data hold time at recipient
t_{DVS}	70		48		31		20		6.7		4.8		Data valid setup time at sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		4.8		Data valid hold time at sender
t_{DSIC}	14.7		9.7		6.8		6.8		4.8		2.3		Recipient IC data setup time
t_{DHIC}	4.8		4.8		4.8		4.8		4.8		2.8		Recipient IC data hold time
t_{DVSIC}	72.9		50.9		33.9		22.6		9.5		6.0		Sender IC data valid setup time
t_{DVHIC}	9.0		9.0		9.0		9.0		9.0		6.0		Sender IC data valid hold time

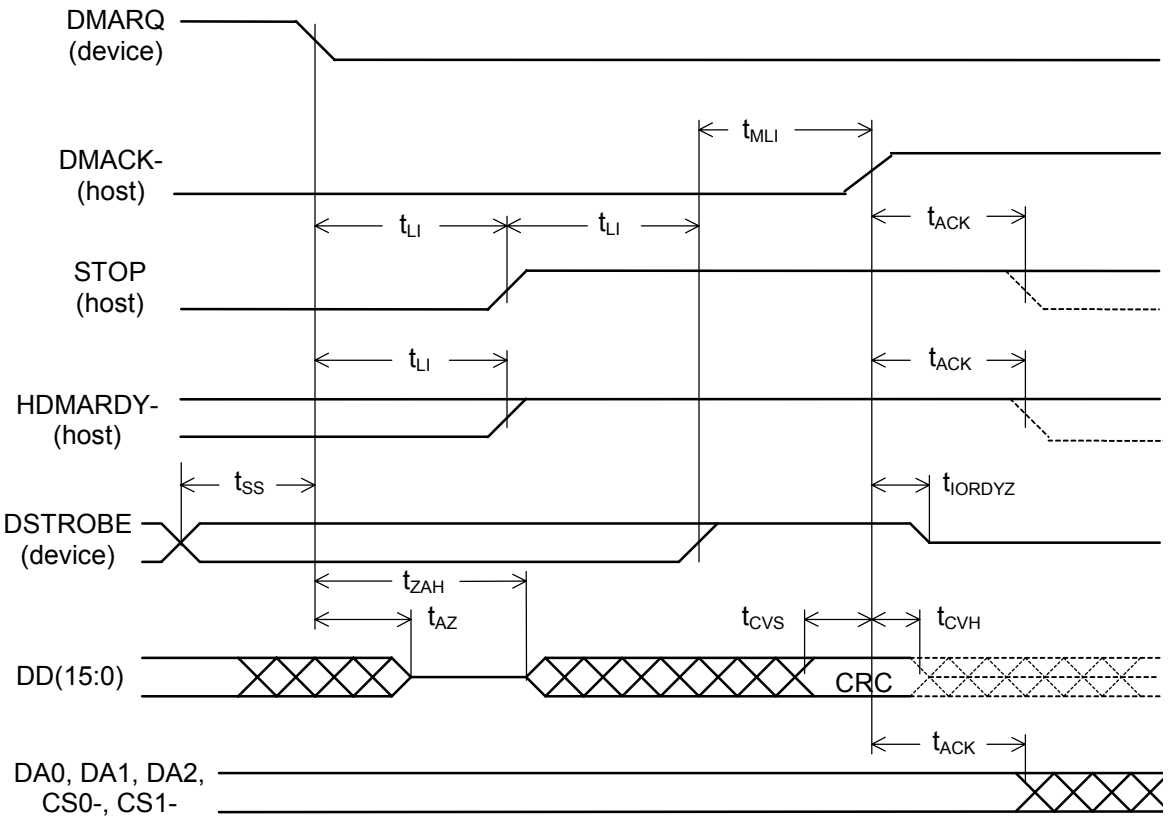
Figure 8.6 Host pausing an Ultra DMA Read



Note: The host asserts STOP to request termination of the Ultra DMA burst no sooner than t_{RP} after HDMARDY- is negated.

	Mode 0(ns)		Mode 1(ns)		Mode 2(ns)		Mode3(ns)		Mode4(ns)		Mode5(ns)		Description
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RFS}		75		70		60		60		60		50	Ready-to-final STROBE time
t_{RP}	160		125		100		100		100		85		Ready-to-pause time

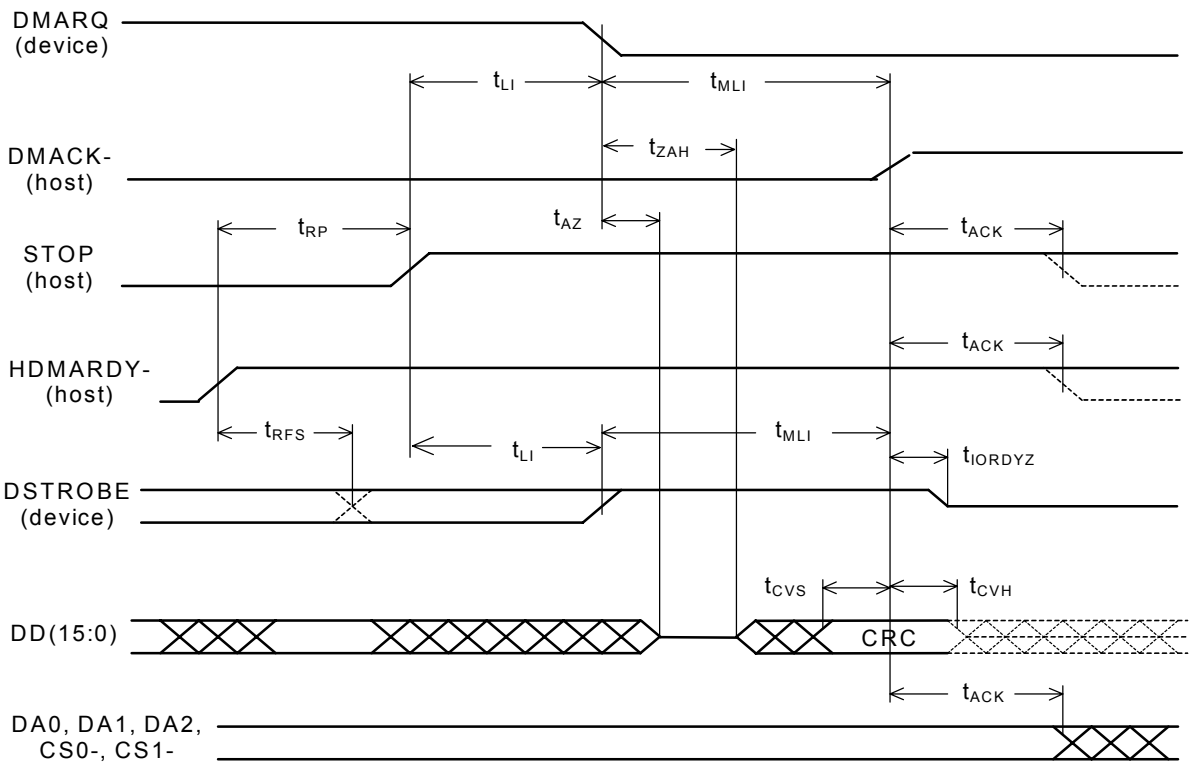
Figure 8.7 Device termination an Ultra DMA Read



Note: The definitions for the STOP, HDMARDY and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

	Mode 0(ns)		Mode 1(ns)		Mode 2(ns)		Mode3(ns)		Mode4(ns)		Mode5(ns)		Description
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CVS}	70		48		31		20		6.7		10		CRC word valid setup time at sender
t_{CVH}	6.2		6.2		6.2		6.2		6.2		10		CRC word valid hold time at sender
t_{LI}	0	150	0	150	0	150	0	100	0	100	0	75	Limited interlock time
t_{MLI}	20		20		20		20		20		20		Interlock time with minimum
t_{AZ}		10		10		10		10		10		10	Maximum time allowed for output drivers to release
t_{ZAH}	20		20		20		20		20		20		Minimum delay time for output drivers turning on
t_{IORDYZ}		20		20		20		20		20		20	Maximum time before releasing IORDY
t_{ACK}	20		20		20		20		20		20		Setup and hold times before assertion and negation of DMACK_
t_{SS}	50		50		50		50		50		50		Time from STROBE edge to negation of DMARQ or assertion of STOP

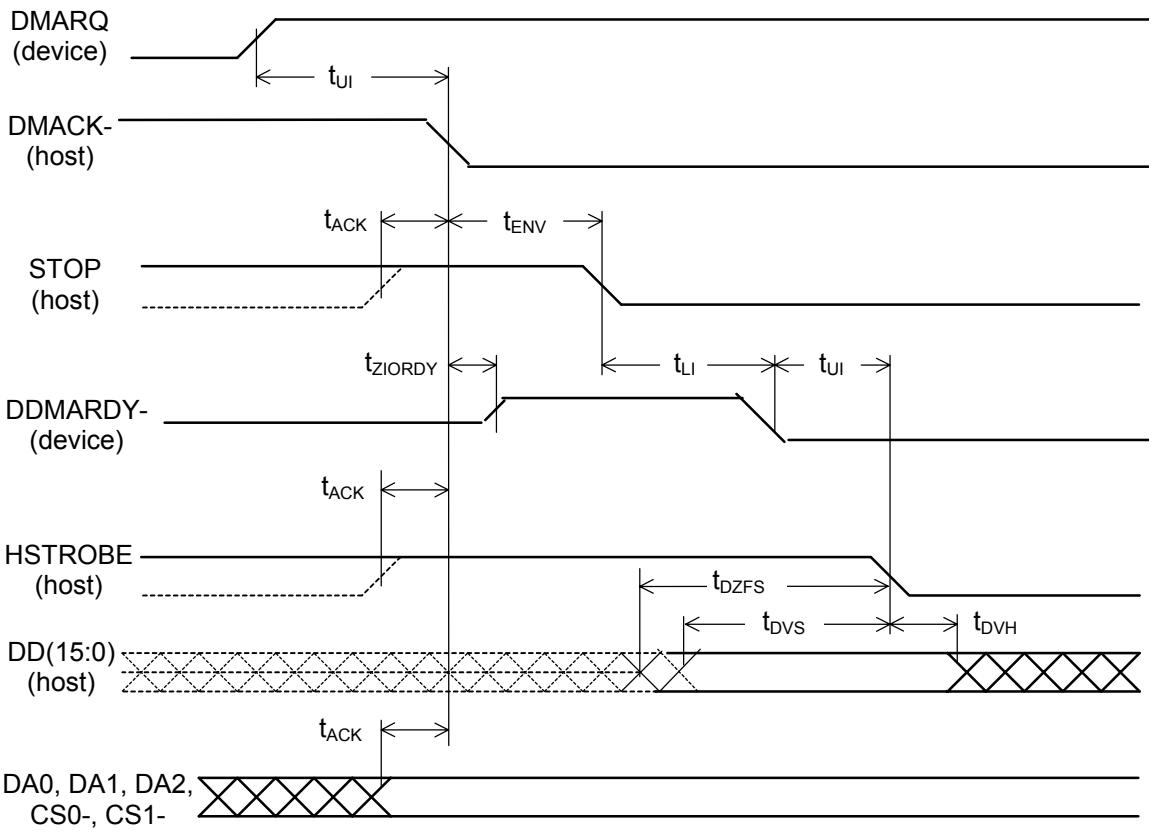
Figure 8.8 Host terminating an Ultra DMA Read



Note: The definitions for the STOP, HDMARDY and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

	Mode 0(ns)		Mode 1(ns)		Mode 2(ns)		Mode3(ns)		Mode4(ns)		Mode5(ns)		Description
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CVS}	70		48		31		20		6.7		10		CRC word valid setup time at sender
t_{CVH}	6.2		6.2		6.2		6.2		6.2		10		CRC word valid hold time at sender
t_{LI}	0	150	0	150	0	150	0	100	0	100	0	75	Limited interlock time
t_{MLI}	20		20		20		20		20		20		Interlock time with minimum
t_{AZ}		10		10		10		10		10		10	Maximum time allowed for output drivers to release
t_{ZAH}	20		20		20		20		20		20		Minimum delay time for output drivers turning on
t_{RFS}		75		70		60		60		60		50	Ready-to-final-STROBE time
t_{RP}	160		125		100		100		100		85		Ready-to-pause time
t_{IORDYZ}		20		20		20		20		20		20	Maximum time before releasing IORDY
t_{ACK}	20		20		20		20		20		20		Setup and hold times before assertion and negation of DMACK_

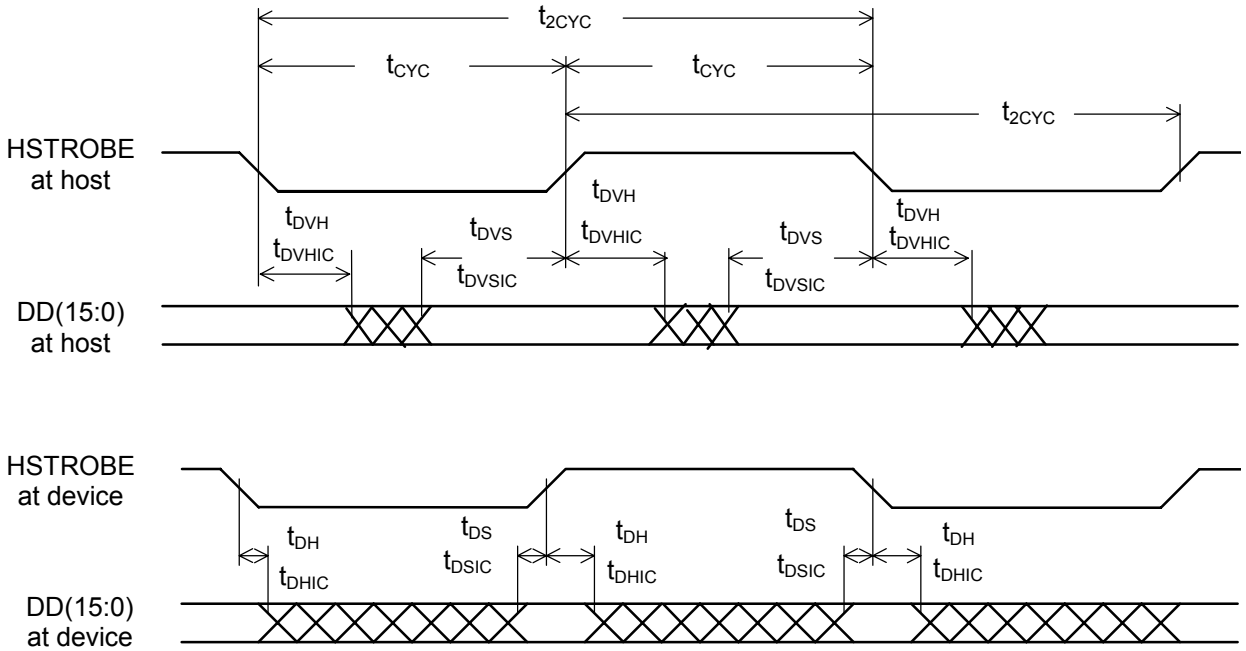
Figure 8.9 Initiating an Ultra DMA Write



Note: The definitions for the STOP, DDMARDY and HSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

	Mode 0(ns)		Mode 1(ns)		Mode 2(ns)		Mode3(ns)		Mode4(ns)		Mode5(ns)		Description
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{DVS}	70		48		31		20		6.7		4.8		Data valid setup time at sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		4.8		Data valid hold time at sender
t_{LI}	0	150	0	150	0	150	0	100	0	100	0	75	Limited interlock time
t_{UI}	0		0		0		0		0		0		Unlimited interlock
t_{ENV}	20	70	20	70	20	70	20	55	20	55	20	50	Envelope time
t_{ZIORDY}	0		0		0		0		0		0		Minimum time before driving IORDY
t_{ACK}	20		20		20		20		20		20		Setup and hold times before assertion and negation of DMACK_
t_{DZFS}	70		48		31		20		6.7		25		Time from data output released-to-driving until the first transition of critical timing

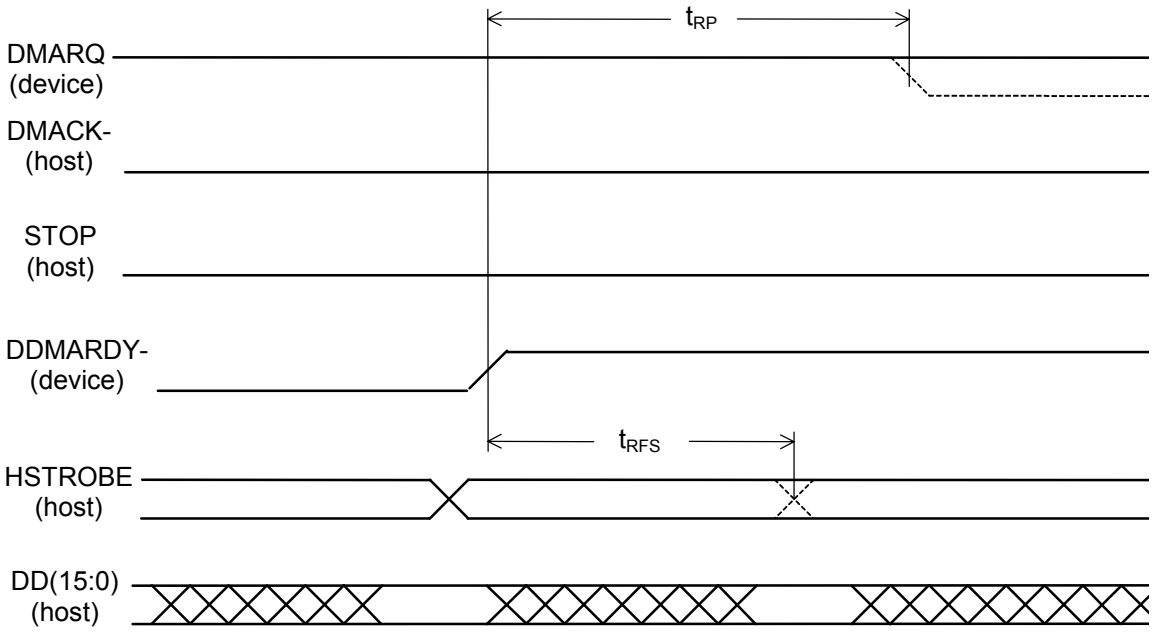
Figure 8.10 Sustained Ultra DMA Write Data



Note: DD(15:0) and HSTROBE signals are shown at both the device and the host to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host.

	Mode 0(ns)		Mode 1(ns)		Mode 2(ns)		Mode 3(ns)		Mode 4(ns)		Mode5(ns)		Description
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CYC}	112		73		54		39		25		16.8		Cycle time allowing for asymmetry and clock variation
$t2_{CYC}$	230		153		115		86		57		38		Two cycle time allowing for clock variation
t_{DS}	15		10		7		7		5		4		Data setup time at recipient
t_{DH}	5		5		5		5		5		4.6		Data hold time at recipient
t_{DVS}	70		48		31		20		6.7		4.8		Data valid setup time at sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		4.8		Data valid hold time at sender
t_{DSIC}	14.7		9.7		6.8		6.8		4.8		2.3		Recipient IC data setup time
t_{DHIC}	4.8		4.8		4.8		4.8		4.8		2.8		Recipient IC data hold time
t_{DVSIC}	72.9		50.9		33.9		22.6		9.5		6.0		Sender IC data valid setup time
t_{DVHIC}	9		9		9		9		9		6		Sender IC data valid hold time

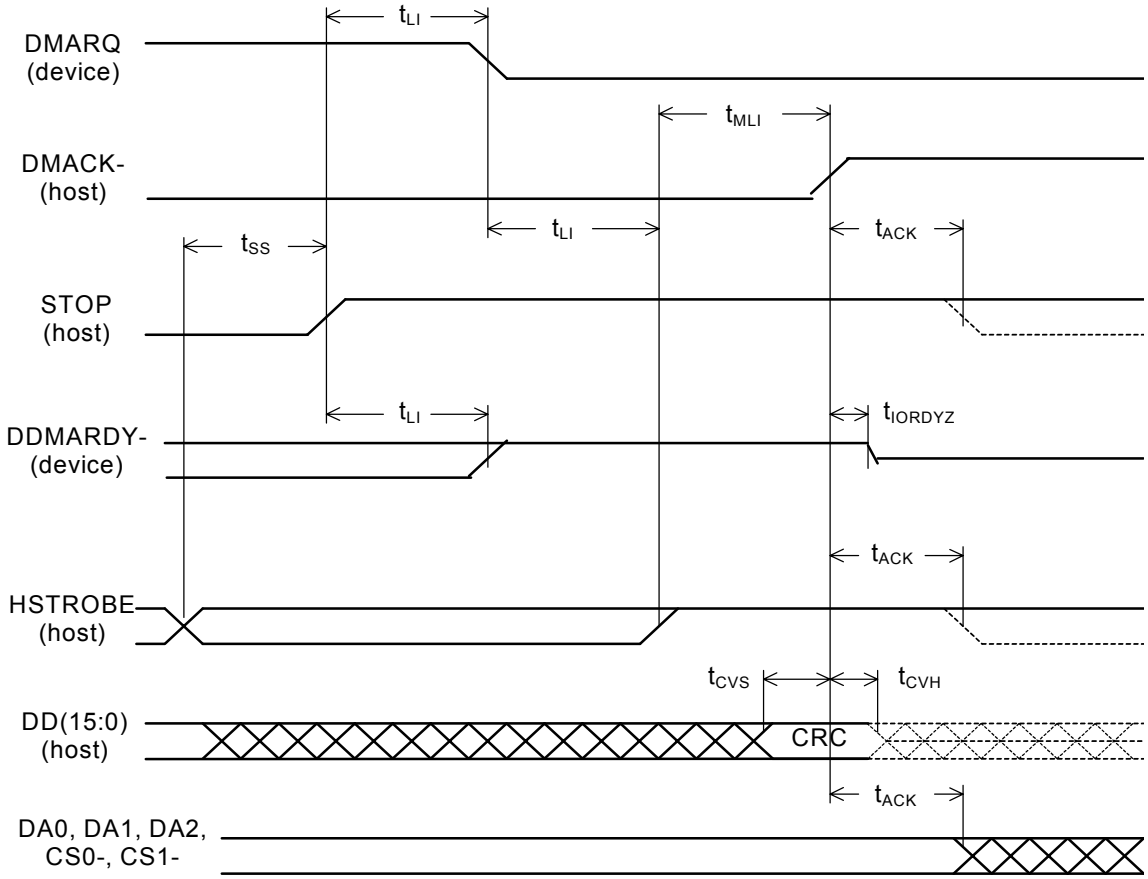
Figure 8.11 Device pausing an Ultra DMA Write



Note: The device negates DMARQ to request termination of the Ultra DMA burst no sooner than t_{RP} after DDMARDY- is negated.

	Mode 0(ns)		Mode 1(ns)		Mode 2(ns)		Mode 3(ns)		Mode 4(ns)		Mde5(ns)		Description
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RFS}		75		70		60		60		60		50	Ready-to-final STROBE time
t_{RP}	160		125		100		100		100		85		Ready-to-pause time

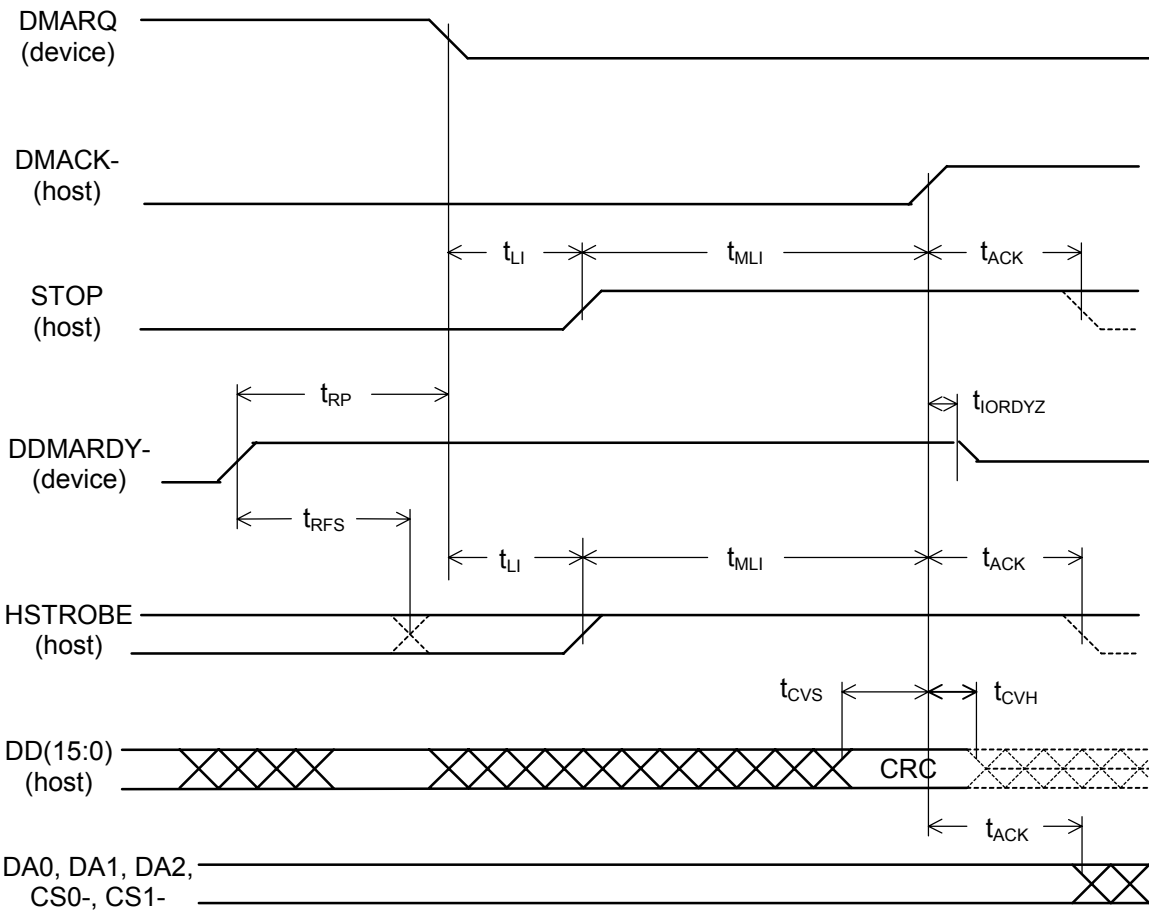
Figure 8.12 Host terminating an Ultra DMA Write



Note: The definitions for the STOP, DDMARDY and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

	Mode 0(ns)		Mode 1(ns)		Mode 2(ns)		Mode 3(ns)		Mode 4(ns)		Mode5(ns)		Description
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CVS}	70		48		31		20		6.7		10		CRC word valid setup time at sender
t_{CVH}	6.2		6.2		6.2		6.2		6.2		10		CRC word valid hold time at sender
t_{LI}	0	150	0	150	0	150	0	100	0	100	0	75	Limited interlock time
t_{MLI}	20		20		20		20		20		20		Interlock time with minimum
t_{AZ}		10		10		10		10		10		10	Maximum time allowed for output drivers to release
t_{IORDYZ}		20		20		20		20		20		20	Maximum time before releasing IORDY
t_{ACK}	20		20		20		20		20		20		Setup and hold times for DMACK_
t_{SS}	50		50		50		50		50		50		Time from STROBE edge to negation of DMARQ or assertion of STOP

Figure 8.13 Device terminating an Ultra DMA Write

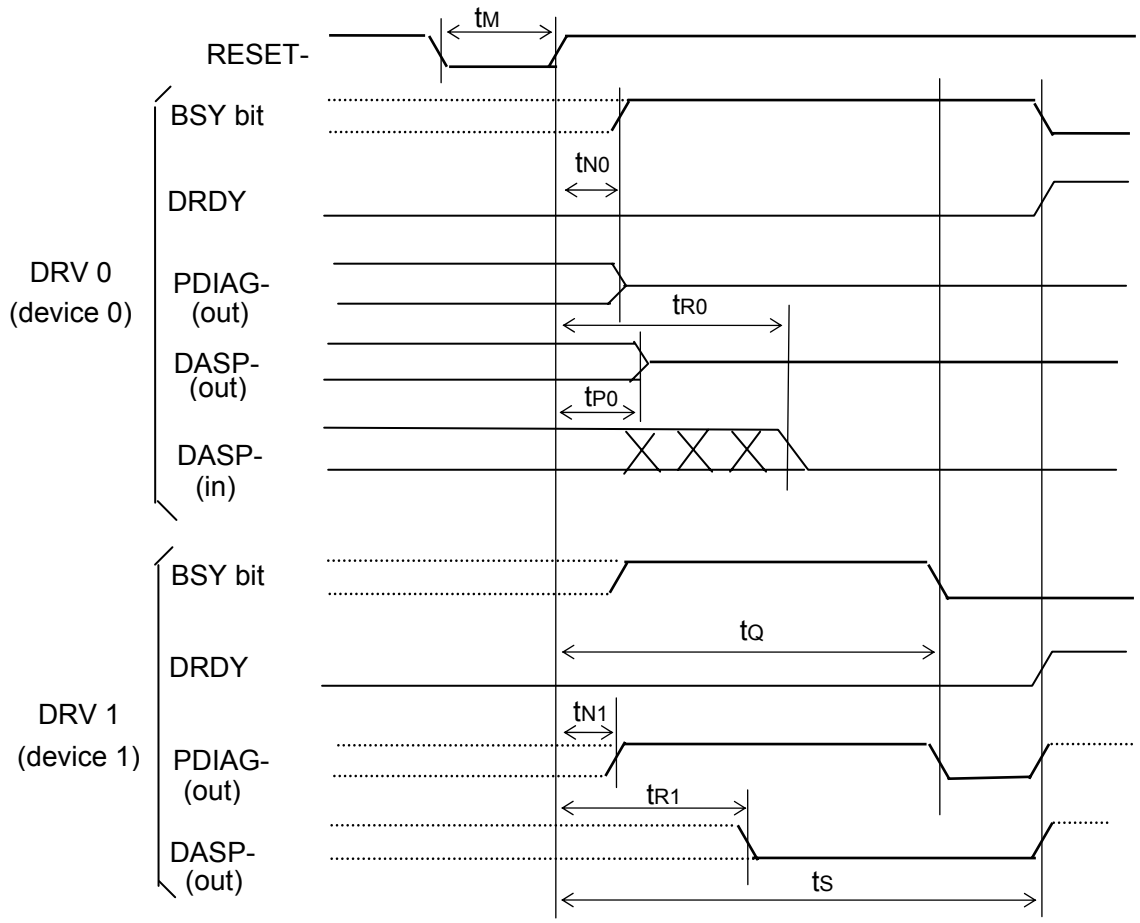


Note: The definitions for the STOP, DDMARDY and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

	Mode 0(ns)		Mode 1(ns)		Mode 2(ns)		Mode 3(ns)		Mode 4(ns)		Mode5(ns)		Description
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CVS}	70		48		31		20		6.7		10		CRC word valid setup time at sender
t_{CVH}	6.2		6.2		6.2		6.2		6.2		10		CRC word valid hold time at sender
t_{LI}	0	150	0	150	0	150	0	100	0	100	0	75	Limited interlock time
t_{MLI}	20		20		20		20		20		20		Interlock time with minimum
t_{RFS}		75		70		60		60		60		50	Ready-to-final-STROBE time
t_{RP}	160		125		100		100		100		85		Ready-to-pause time
t_{IORDYZ}		20		20		20		20		20		20	Maximum time before releasing IORDY
t_{ACK}	20		20		20		20		20		20		Setup and hold times for DMACK_

8.3. Power On and Hardware Reset Timing

Figure 8.14 Power on and Hardware Reset Timing



SYMBOL	Description	MIN	MAX	Units
t_M	RESET- Pulse Width	25		μs
t_{N0}	DRV 0 RESET negation to BSY bit set to one, release PDIAG-		400	ns
t_{P0}	DRV 0 release DASP-		1	ms
t_{R0}	DRV 0 sample of DASP-	1	450	ms
t_S	DRV 0 sample of PDIAG-	1ms	31s	-
t_{R1}	DRV 1 assert DASP-		400	ms
t_{N1}	DRV 1 negate PDIAG- if asserted		1	ms
t_Q	DRV 1 assert PDIAG-		30	sec

< Glossary >

ATA	AT Attachment
ABRT	Aborted Command
AMNF	AM Not Found
APM	Advanced Power Management
BIOS	Basic Input-Output System
BPI	Bit Per Inch
BSY	Busy
CDR	Constant Density Recording
CHS	Cylinder Head Sector
CORR	Corrected Data
CRC	Cyclic Redundancy Check
CSS	Contact Start/Stop
CYL	Cylinder
DMA	Direct Memory Accessing
DRV	Drive
DRDY	Drive Ready
DRQ	Data Request
DSC	Drive Seek Complete
DWF	Drive Write Fault
ECC	Error Checking and Correction
ERR	Error
GND	Ground
GB	1000,000,000 bytes
HD	Head
HDA	Head/Disk Assembly
HDD	Hard Disk Drive
I/O	Input/Output
ICRC	Interface CRC Error
IDE	Intelligent Device Electronics
IDNF	ID Not Found
IDX	Index
MB	1000,000 bytes
ME^{2}PRML	Modified, Extended, Extended Partial Response Maximum Likelihood
PCBA	Printed Circuit Board Assembly
PIO	Programmed Input-output
p-p	peak to peak
RPM	Rotation Per Minute
SC	Sector Count Register
sec	second
SMART	Self-monitoring, Analysis and Reporting Technology
SPT	Sector Per Track
SRST	Software Reset
TK0NF	Track 0 Not Found
TPI	Track Per Inch
Typ.	Typical
UNC	Uncorrectable ECC error

<Reference>

Factory Packaging

The structure of the factory packaging is described in this reference.

(1) Packaging Components

No.	Name	Materials	Quantity
1	Package box	Card box	1
2	HDD Cushion	Card Board	1
3	Upper Cushion	Card Board	1
4	Side Cushion	. Card Board	4
5	Desiccant	Silica gel	50
6	Vinyl Package	ESD protective bags	50

(2) Standard Identification Label

The label is indicated on the exterior of the package. The following items will be based on user request.

(a) HDD type
(b) HDD serial number
(c) Package serial number
(d) Quantity